

BLF8G10LS-160V

Power LDMOS transistor

Rev. 2 — 24 October 2012

Product data sheet

1. Product profile

1.1 General description

160 W LDMOS power transistor with improved video bandwidth for base station applications at frequencies from 925 MHz to 960 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in a common source class-AB production test circuit.

Test signal	f (MHz)	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	925 to 960	1100	30	35	19.9	30	-38 ^[1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier. Carrier spacing 5 MHz.

1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Decoupling leads to enable improved video bandwidth (60 MHz typical)
- Designed for broadband operation (925 MHz to 960 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 925 MHz to 960 MHz frequency range



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		<p>aaa-003619</p>
2	gate		
3	source		
4	decoupling lead		
5	decoupling lead		
6	n.c.		
7	n.c.		

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BLF8G10LS-160V	-	earless flanged ceramic package; 6 leads	SOT1244B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$; $P_L = 35\text{ W}$; $V_{DS} = 30\text{ V}$; $I_{Dq} = 1100\text{ mA}$	0.5	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.2\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 220\text{ mA}$	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	39.0	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 7.7\text{ A}$	-	14.9	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 7.7\text{ A}$	-	85	151	$\text{m}\Omega$

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR = 7.5 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; $f_1 = 925\text{ MHz}; f_2 = 930\text{ MHz}; f_3 = 955\text{ MHz}; f_4 = 960\text{ MHz}$; RF performance at $V_{DS} = 30\text{ V}; I_{Dq} = 1100\text{ mA}; T_{case} = 25\text{ }^\circ\text{C}$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 35\text{ W}$	18.4	19.9	-	dB
RL_{in}	input return loss	$P_{L(AV)} = 35\text{ W}$	-	-15	-10	dB
η_D	drain efficiency	$P_{L(AV)} = 35\text{ W}$	27	30	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 35\text{ W}$	-	-38	-32.5	dBc

7. Test information

7.1 Ruggedness in class-AB operation

BLF8G10LS-160V is capable of withstanding a load mismatch corresponding to $V_{SWR} = 10 : 1$ through all phases under the following conditions: $V_{DS} = 30\text{ V}; I_{Dq} = 1100\text{ mA}; P_L = 160\text{ W (CW)}; f = 925\text{ MHz to } 960\text{ MHz}$.

7.2 Impedance information

Table 8. Typical impedance information

$I_{Dq} = 1100\text{ mA}$; main transistor $V_{DS} = 30\text{ V}$.

Z_S and Z_L defined in [Figure 1](#).

f (MHz)	Z_S (Ω)	Z_L (Ω)
925	4.5 – j4.1	1.2 – j2.4
942	5.9 – j4.0	1.2 – j2.3
960	6.2 – j4.7	1.2 – j2.5

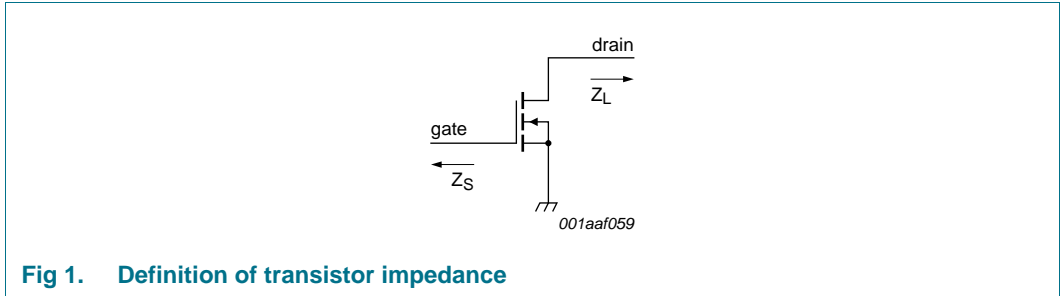


Fig 1. Definition of transistor impedance

7.3 VBW in class-AB operation

The BLF8G10LS-160V shows 60 MHz (typical) video band-width in class-AB test circuit in 900 MHz band at $V_{DS} = 30\text{ V}$ and $I_{Dq} = 1.1\text{ A}$.

7.4 Circuit

The diagram shows a top-down view of a PCB layout. A central area represents the transistor. Various components are placed around it: capacitors C1, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18; and resistors R1 and R2. Two large circular components, C12 and C13, are located on the right side. The reference number 'aaa-004169' is at the bottom right.

Printed-Circuit Board (PCB): Rogers RO4350; $\epsilon_r = 3.5\text{ F/m}$; thickness = 0.762 mm; thickness copper plating = 35 μm .

The vias can be used as a reference to place components.

The above layout shows the test circuit used to measure the devices in production. A more appropriate application demonstration for specific customer needs can be provided.

See [Table 9](#) for list of components.

Fig 2. Component layout

Table 9. List of components

See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C3	multilayer ceramic chip capacitor	11 pF	ATC 800B
C4, C5	multilayer ceramic chip capacitor	36 pF	ATC 800B
C6, C7	multilayer ceramic chip capacitor	6.8 pF	ATC 800B
C8, C9, C10, C11	multilayer ceramic chip capacitor	10 μF	Murata
C12, C13	electrolytic capacitor	470 μF , 63 V	

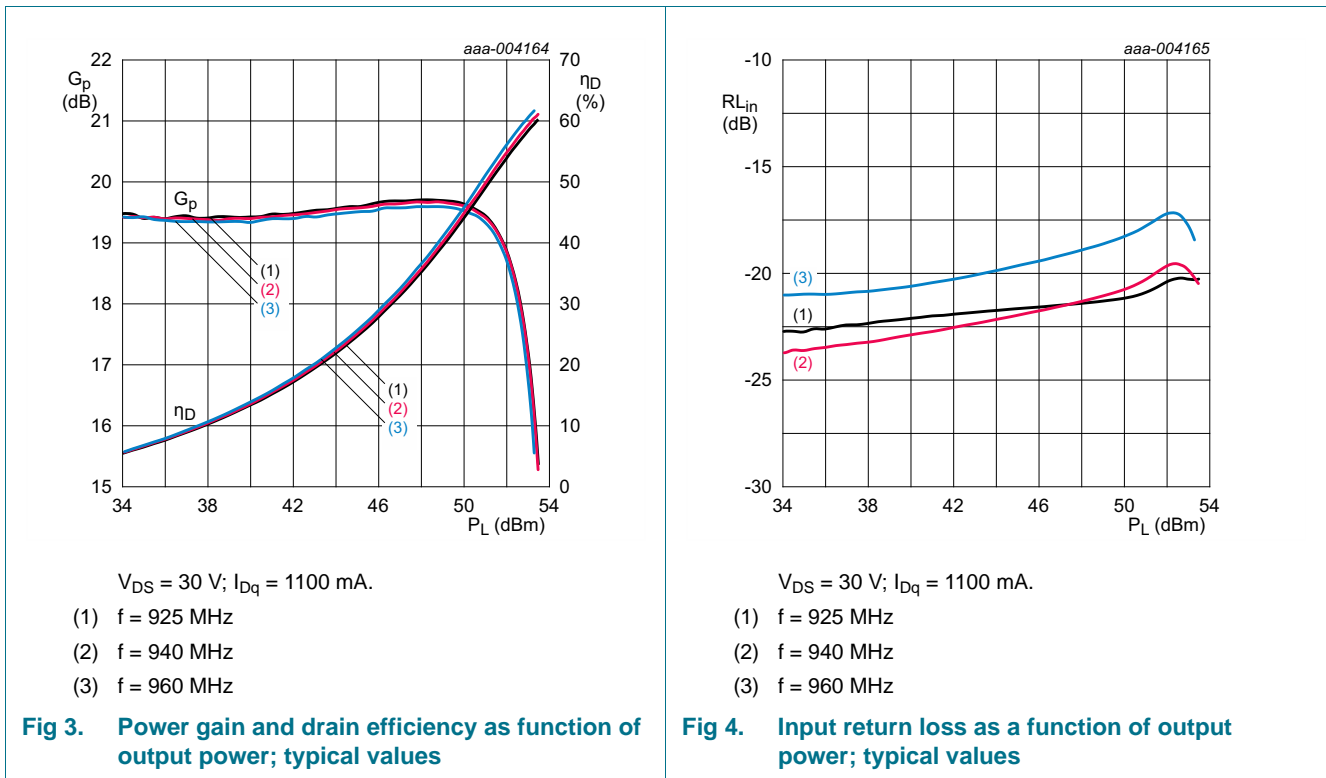
Table 9. List of components
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C14, C15	multilayer ceramic chip capacitor	4.7 μ F	[1] Murata
C18	multilayer ceramic chip capacitor	1 μ F	Murata
R1, R2	resistor	2.0 Ω	

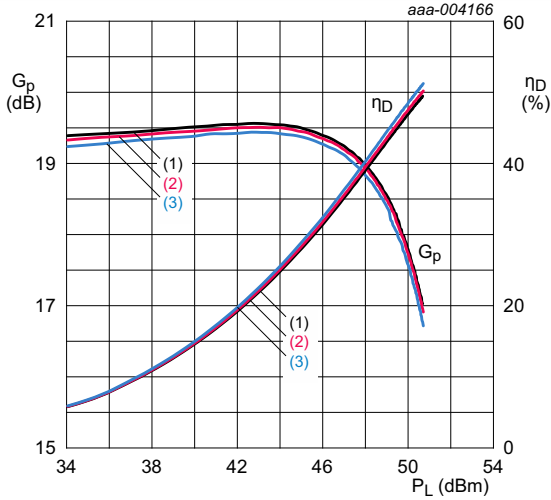
[1] Video decoupling capacitors are not used in production test circuit.

7.5 Graphical data

7.5.1 CW pulse

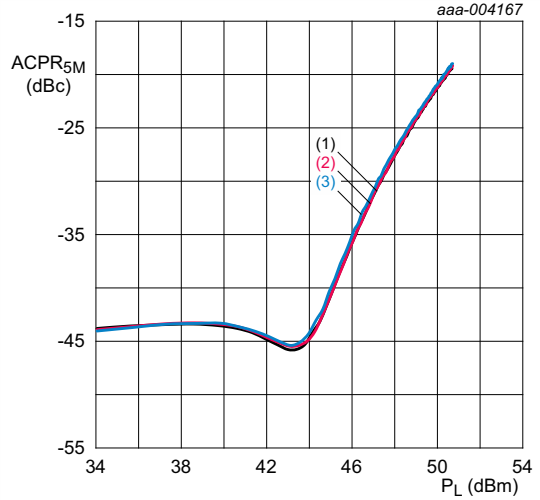


7.5.2 2-Carrier W-CDMA



$V_{DS} = 30\text{ V}; I_{Dq} = 1100\text{ mA}$.
 (1) $f = 925\text{ MHz}$
 (2) $f = 940\text{ MHz}$
 (3) $f = 960\text{ MHz}$

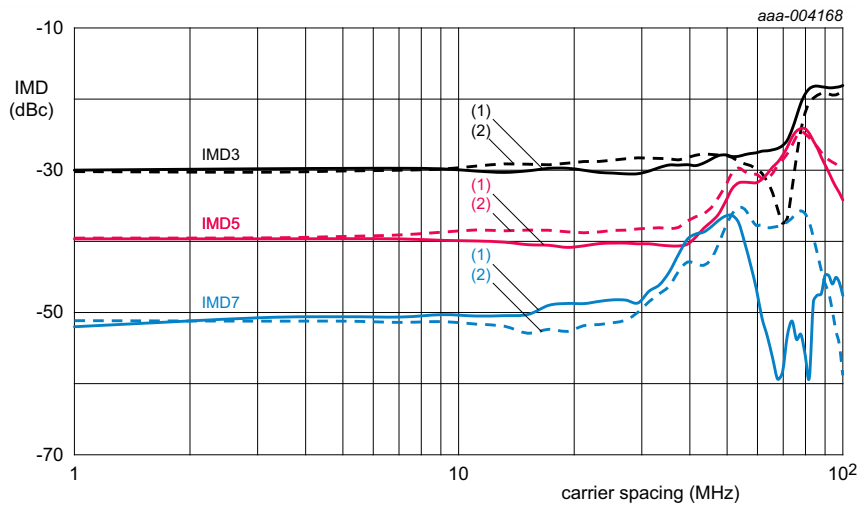
Fig 5. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 30\text{ V}; I_{Dq} = 1100\text{ mA}$.
 (1) $f = 925\text{ MHz}$
 (2) $f = 940\text{ MHz}$
 (3) $f = 960\text{ MHz}$

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

7.5.3 2-Tone VBW



$V_{DS} = 30\text{ V}; I_{Dq} = 1100\text{ mA}; f = 942\text{ MHz}$.
 (1) IMD low
 (2) IMD high

Fig 7. VBW capability in class-AB test circuit

8. Package outline

Earless flanged ceramic package; 6 leads

SOT1244B

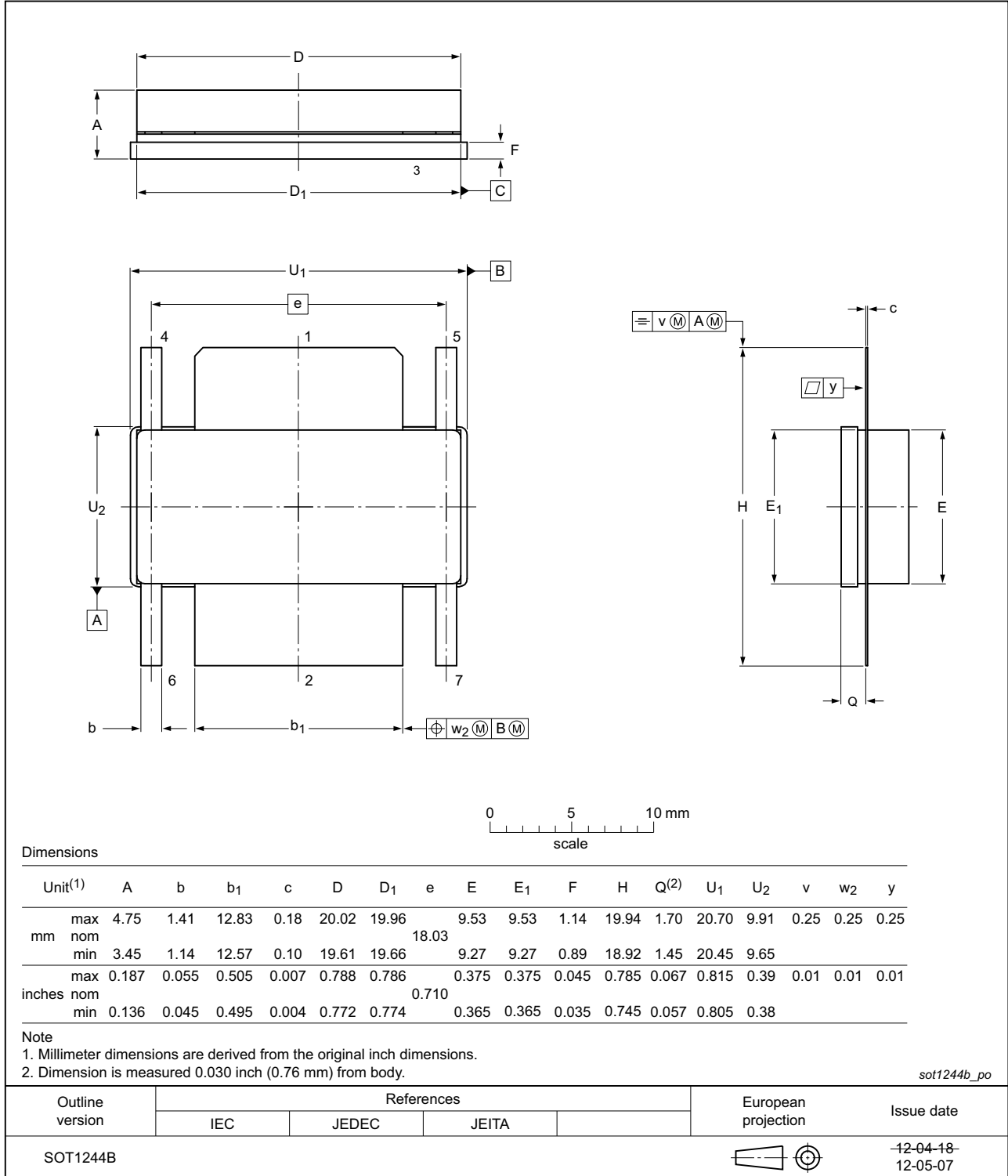


Fig 8. Package outline SOT1244B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PAR	Peak-to-Average Ratio
VSWR	Voltage Standing Wave Ratio
VBW	Video BandWidth
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G10LS-160V v.2	20121024	Product data sheet	-	BLF8G10LS-160V v.2
Modifications:				
<ul style="list-style-type: none"> The status of this document has been changed to Product data sheet Table 1 on page 1: changed several values. Table 7 on page 3: changed several values. Table 7 on page 3: moved table to Section 6 on page 3. Moved graphical data to Section 7.5 on page 5. 				
BLF8G10LS-160V v.1	20120713	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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