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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR



2SK3113

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3113 is N-channel DMOS FET device that features a low gate charge and excellent switching characteristic, and designed for high voltage applications such as switching power supply, AC adapter.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3113	TO-251 (MP-3)
2SK3113-Z	TO-252 (MP-3Z)

FEATURES

Low on-state resistance

 $R_{DS(on)} = 4.4 \Omega MAX. (V_{GS} = 10 V, I_{D} = 1.0 A)$

Low gate charge

 $Q_G = 9 \text{ nC TYP.}$ ($V_{DD} = 450 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 2.0 \text{ A}$)

- Gate voltage rating ±30 V
- Avalanche capability ratings

(TO-251)

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (VGS = 0 V)	VDSS	600	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±30	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±2.0	Α
Drain Current (pulse) Note1	D(pulse)	±8.0	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	20	W
Total Power Dissipation (T _A = 25°C) Note2	P _{T2}	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note3	las	2.0	Α
Single Avalanche Energy Note3	Eas	2.7	mJ



(TO-252)



Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Mounted on glass epoxy board of 40 mm \times 40 mm \times 1.6 mm

3. Starting T_{ch} = 25°C, V_{DD} = 150 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V

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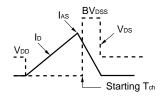


ELECTRICAL CHARACTERISTICS (TA = 25°C)

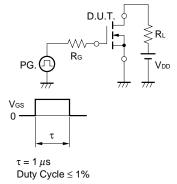
	•	-				
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	Ipss	Vps = 600 V, Vgs = 0 V			100	μА
Gate Leakage Current	lgss	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$			±10	μА
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.5		3.5	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 1.0 A	0.5			S
Drain to Source On-state Resistance	RDS(on)	Vgs = 10 V, ID = 1.0 A		3.3	4.4	Ω
Input Capacitance	Ciss	V _{DS} = 10 V		290		pF
Output Capacitance	Coss	Vgs = 0 V		60		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		5		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 150 V, I _D = 1.0 A		7		ns
Rise Time	tr	Vgs = 10 V		2		ns
Turn-off Delay Time	t _{d(off)}	$R_G = 10 \Omega$, $R_L = 10 \Omega$		22		ns
Fall Time	tr			9		ns
Total Gate Charge	QG	V _{DD} = 450 V		9		nC
Gate to Source Charge	Qgs	Vgs = 10 V		2.4		nC
Gate to Drain Charge	Q _{GD}	I _D = 2.0 A		2		nC
Body Diode Forward Voltage	V _F (S-D)	IF = 2.0 A, VGS = 0 V		0.9		V
Reverse Recovery Time	trr	IF = 2.0 A, VGS = 0 V		0.9		μS
Reverse Recovery Charge	Qrr	di/dt = 50 A/μs		2.0		μC

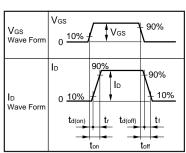
TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c} \text{D.U.T.} \\ \text{PG.} \\ \text{PG.} \\ \end{array} \begin{array}{c} \text{Rg} = 25 \ \Omega \\ \text{$>$} 50 \ \Omega \end{array} \begin{array}{c} \text{\downarrow} \\ \text{\downarrow} \\ \text{\downarrow} \end{array} \begin{array}{c} \text{\downarrow} \\ \text{\downarrow} \\ \text{\downarrow} \end{array} \begin{array}{c} \text{\downarrow} \\ \text{\downarrow} \\ \text{\downarrow} \end{array}$

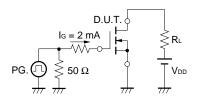


TEST CIRCUIT 2 SWITCHING TIME

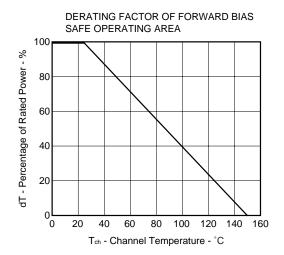


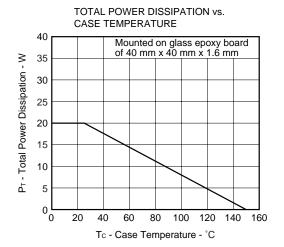


TEST CIRCUIT 3 GATE CHARGE

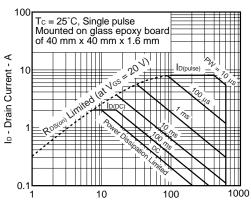


TYPICAL CHARACTERISTICS (TA = 25°C)



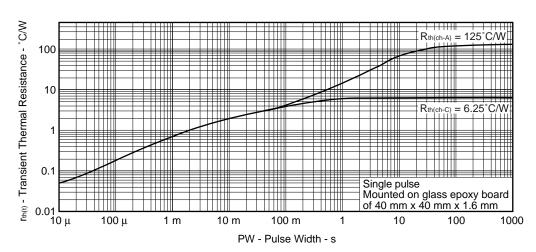


FORWARD BIAS SAFE OPERATING AREA

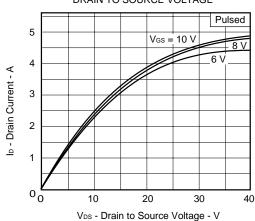


$V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

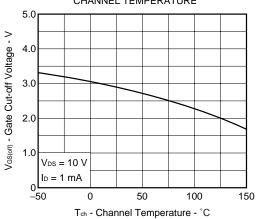
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



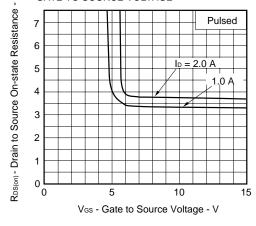
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



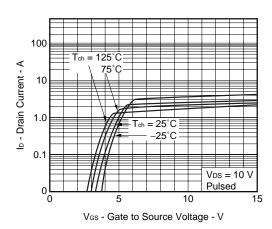
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



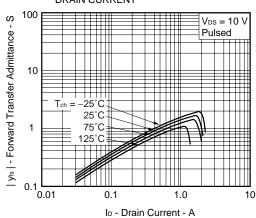
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



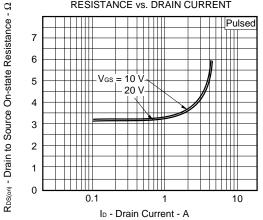
FORWARD TRANSFER CHARACTERISTICS

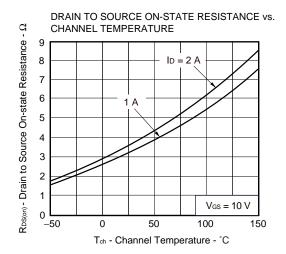


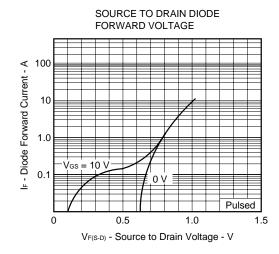
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

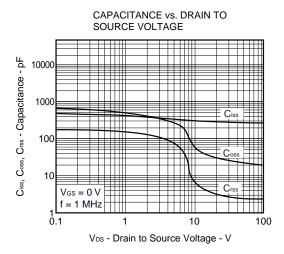


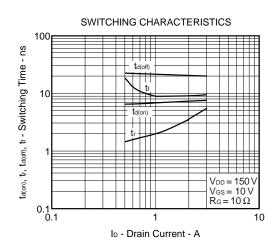
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

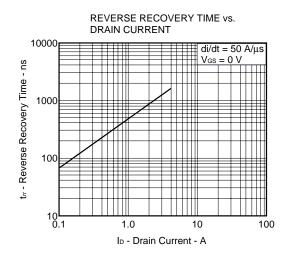


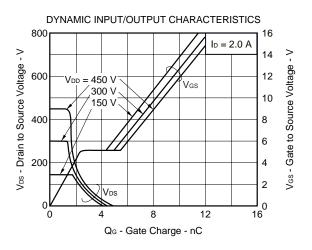


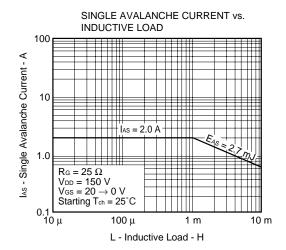


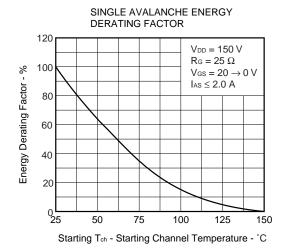








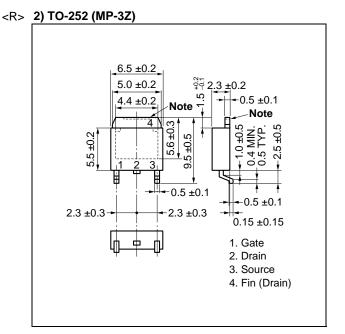






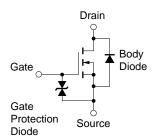
PACKAGE DRAWINGS (Unit: mm)

1) TO-251 (MP-3) 40.7 6.5 ± 0.2 1.5 5.0 ±0.2 0.5 ±0.1 1.6 ±0.2 5.5 13.7 7.0 MIN 1.1 ±0 0.5 +0.2 0.5 +0.2 1. Gate 2. Drain 3. Source 4. Fin (Drain)



Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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