S3086

Device Specification

Continuous Rate Clock Recovery Unit

FEATURES

- SiGe BiCMOS technology
- Complies with Bellcore and ITU-T specifications for jitter tolerance, jitter transfer and jitter generation
- On-chip high-frequency PLL with loop filter for clock recovery
- Programmable signal detect input active High or active Low (LVTTL and LVPECL Input)
- Supports clock recovery from 30 Mbps to 2.7 Gbps with no gaps
- Capable of working at OC-48 with Forward Error Correction (FEC), OC-48, FireWire, HDTV, GE, FC, OC-12, DTV, ESCON, OC-3, FDDI, FE, OC-1 and DS-3 rates
- Selectable optional reference clock (19.44/155.52 MHz for SONET rates or user defined for non-SONET rates)
- Loss-of-Lock Indication
- Low jitter serial interface
- +3.3 V single power supply
- Compact 48-pin TQFP/TEP package
- Typical power 825 mW (Serial Clock Enabled)
- Typical power 700 mW (Serial Clock Disabled)

APPLICATIONS

- SONET/SDH/ATM/OC-3/OC-12/OC-48
- Fibre Channel
- Gigabit Ethernet/Fast Ethernet
- High Definition Television/Digital Television (HDTV/DTV)
- FireWire
- Fibre Distributed Data Interface (FDDI)
- Enterprise Systems Connection (ESCON)
- DS-3

GENERAL DESCRIPTION

The Continuous Rate Clock Recovery Unit (CRU) is a variable rate clock recovery interface device. The device is suitable for use in applications such as SONET/SDH, Fibre Channel, Fast Ethernet, HDTV, ESCON, Gigabit Ethernet, and DS-3. The chip performs all necessary clock recovery functions in conformance with the Bellcore 253, IEEE 802.3, and SMPTE 292/184 transmission standards.

The function of the S3086 continuous rate clock recovery unit is to derive high-speed timing signals for all rates from 30 Mbps to 2.7 Gbps. The S3086 is implemented using AMCC's proven Phase Lock Loop (PLL) technology. Figure 1 shows a typical network application for the S3086.

The S3086 receives a scrambled NRZ signal from 30 Mbps to 2.7 Gbps and recovers the clock from the data. The chip may output a differential bit clock with retimed data. An external oscillator may be used for continuous down-stream clocking in SONET applications.

The S3086 utilizes an on-chip PLL which consists of a phase detector, a loop filter, and a Voltage Controlled Oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage. A block diagram is shown in Figure 2.

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Figure 1. S3086 Typical Application (Not meant to be used as a reference design)

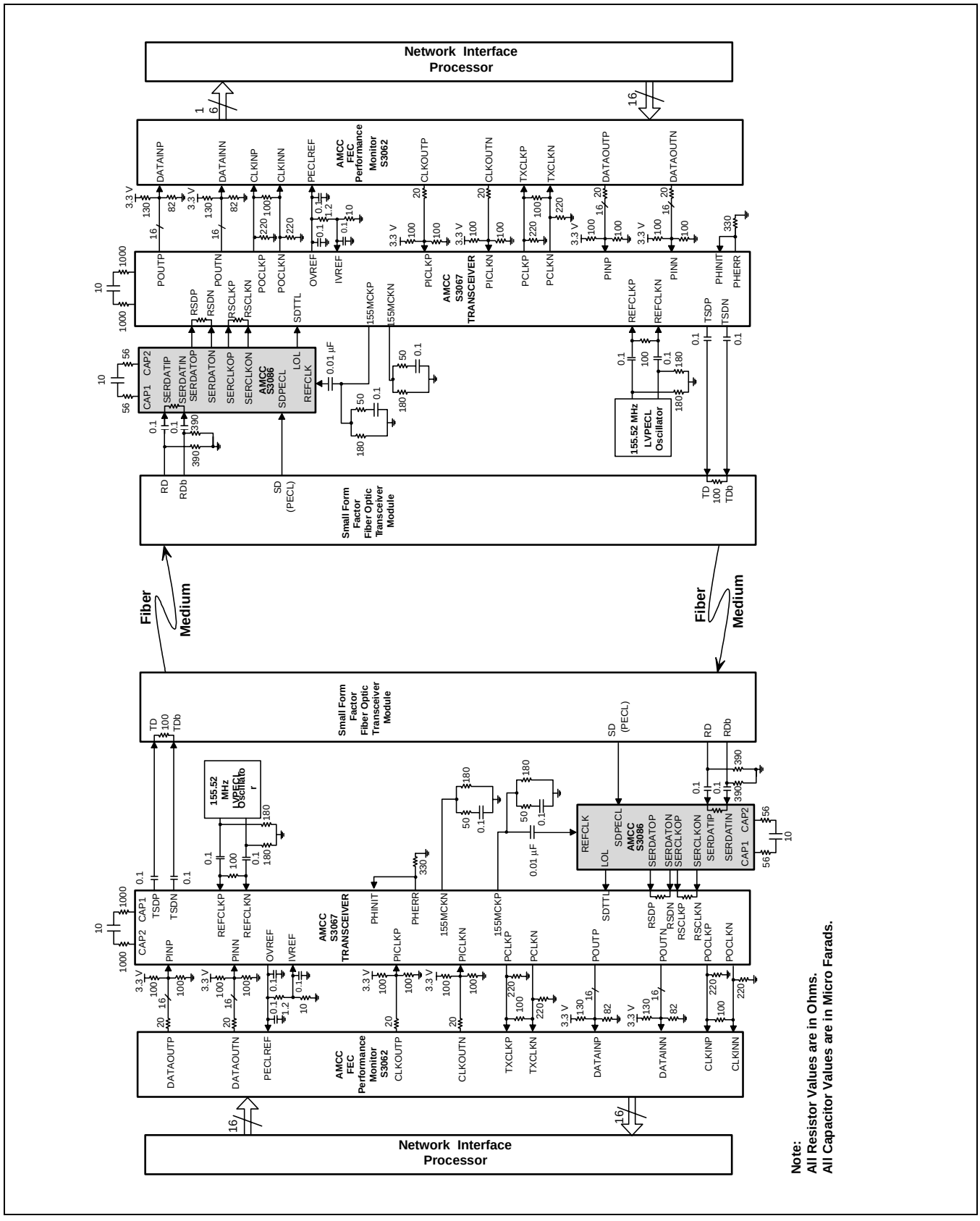


Figure 2. S3086 Functional Block Diagram

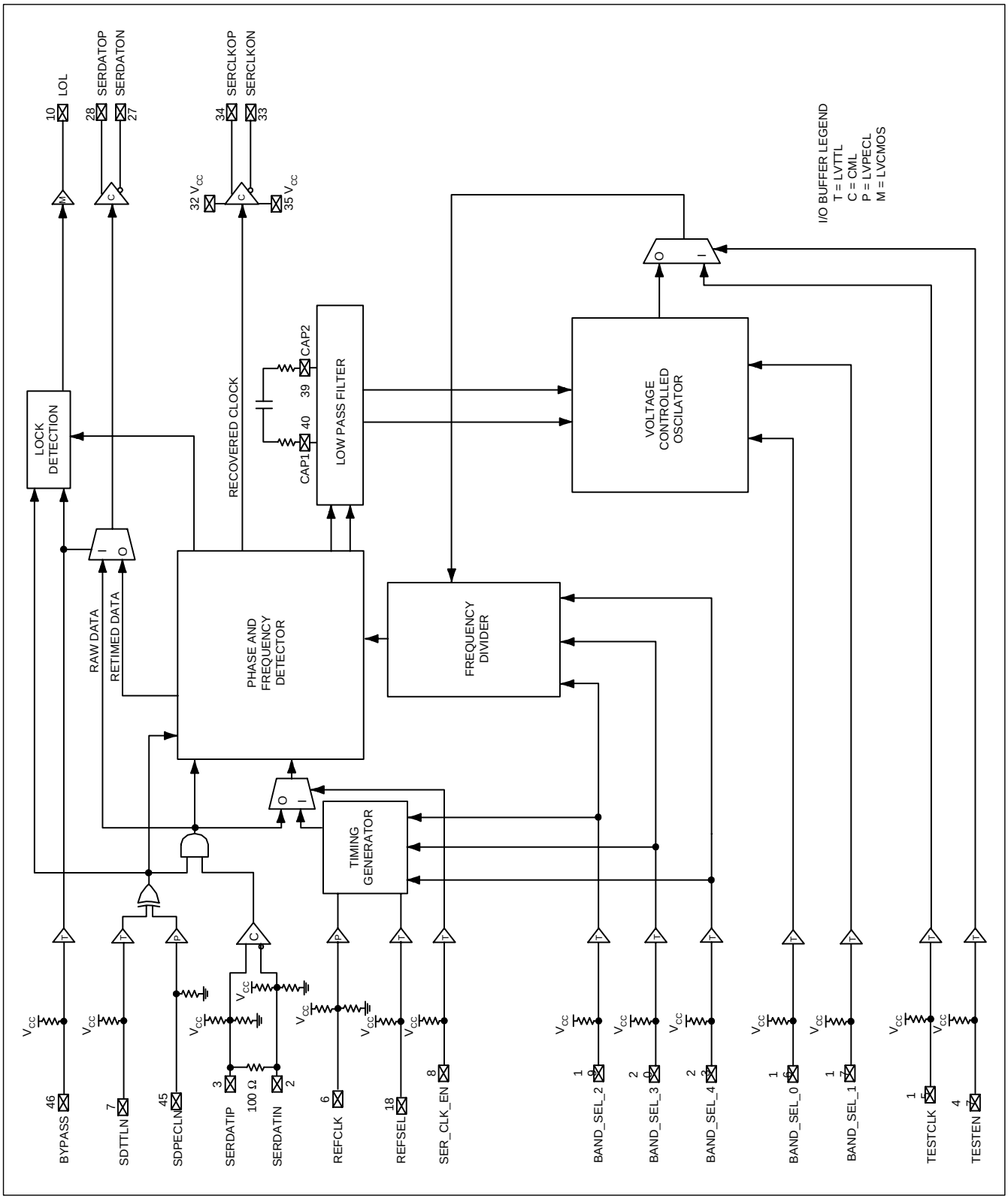


Table 1. Suggested Interface Devices

AMCC S2080	34 X 34 Crosspoint Switch
AMCC S2090	68 X 69 Crosspoint Switch
AMCC S2509	4-Bit LVDS 2.5 Gbps SERDES
AMCC S3055	OC-48 Transceiver
AMCC S3057	OC-48 Transceiver
AMCC S3059	OC-48 Transceiver
AMCC S3067	OC-48 Transceiver
AMCC S7022	Quad VCSEL Driver
AMCC S7025	Quad Transimpedance Amplifier

S3086 PIN DESCRIPTION

Serial Data In (SERDATIP/N)

These pins are the differential Current Mode Logic (CML) serial data inputs. They receive inputs from an optics module or other upstream logic devices. The incoming data rate can be within the range of 30 Mbps to 2.7 Gbps. The S3086 extracts the clock from the SERDATIP/N inputs and provides a retimed clock (SERCLKOP/N). These pins are internally biased and terminated 100 Ω line-to-line. See Figure 20 for CML input buffer structure.

Serial Data Out (SERDATOP/N)

This signal is the retimed version of the incoming data stream (SERDATIP/N) updated on the falling edge of serial clock output (SERCLKOP/N). This signal is typically passed to a deserialization device to be converted to parallel data or may be transmitted across a serial backplane. This is a CML output, internally terminated with 50 Ω to V_{CC}. See Figure 19 for CML output buffer structure.

Serial Clock Out (SERCLKOP/N)

This is the serial data recovered clock. It is phase aligned with the serial output data. This signal is used to synchronize data transfers with downstream logic devices or may remain unused as in the case of serial backplane transmission or repeater/retiming applications. This is a CML output, internally terminated with 50 Ω to VCC. This clock may be powered down by connecting pins 32 and 35 to GND. These pins are the VCC supply for the serial clock output buffer. This will result in a 125 mW (TYP) power saving.

Signal Detect (SDPECLN/SDTTLN)

Two types of signal detect inputs are provided, LVPECL and LVTTL. The LVPECL input should be driven by optical transceivers with LVPECL signal detect outputs, and the LVTTL input should be driven by optical transceivers with a LVTTL signal detect output. The LVTTL input is internally pulled-up and the LVPECL input is internally pulled-down. These inputs may be used with optics modules that are either active Low or active High for signal detection.

For an optics module with a LVPECL output, connect that LVPECL output to the S3086 SDPECLN input (Pin 45), and configure SDTTLN as shown in Table 2.

For an optics module with an LVTTL output, connect that LVTTL output to the S3086 SDTTLN input (Pin 7), and configure SDPECLN as shown in Table 3. See Figures 16 and 18 for LVPECL and LVTTL input buffer structure.

Table 2. SDTTLN Configuration when driving SDPECLN Input with a Signal Detect Source

	Optics Signal Detect Active High (Low value indicates loss of light)	**Optics Signal Detect Active Low (High value indicates loss of light)**
SDTTLN Input	Connect to GND	No Connect

Table 3. SDPECLN Configuration when driving SDTTLN Input with a Signal Detect Source

	Optics Signal Detect Active High (Low value indicates loss of light)	**Optics Signal Detect Active Low (High value indicates loss of light)**
SDPECLN Input	No Connect	Pull-up V_{CC} [1]

1. Connect to V_{CC} through a 1 kΩ pull-up resistor.

Loss of Lock (LOL)

LOL is an active low LVCMOS output that may be used to determine the validity of the serial input data. The following requirements (also referred to as REFCLK Mode) must be met for LOL to be a valid alarm:

- SER_CLK_EN input must be active (SER_CLK_EN = 1)
- Valid REFCLK must be present (consult Table 16 for REFCLK requirements)

If the LOL requirements above are met, an active LOL alarm will indicate that the incoming data stream has failed the PLL frequency test (consult Table 16 for the typical frequency difference values at which the PLL goes in and out of lock) and the incoming data will be considered invalid. This will force the PLL to lock to the incoming REFCLK, maintaining down stream clocking out of the SERCLKOP/N output but the serial output data (SERDATOP/N) will continue to pass the incoming data through the device. If all of the LOL requirements above are met and LOL is inactive, the incoming data stream will have passed the PLL frequency test and the incoming data will be considered valid. Clocking will also be extracted from the incoming data stream, not the REFCLK.

If any of the LOL requirements listed above are not met (also referred to as Non REFCLK Mode) the LOL alarm output is considered invalid and should not be used. Non REFCLK Mode should not be used for SONET/SDH clock recovery/extraction applications because the down stream clocking will not be maintained in the absence of valid data.

Reference Clock (REFCLK)

This LVPECL 19.44 MHz/155.52 MHz user-defined frequency input is used to establish the initial operating frequency of the clock recovery PLL. It is also used as a standby clock in the absence of data. This is an LVPECL input and is internally biased. If downstream clocking is not required, a REFCLK input is not needed. If unused, this input should be pulled Low through a 1 kΩ resistor. In the REFCLK mode, the REFCLK frequency must stay with in the selected band. If the REFCLK frequency goes outside the selected band due to spurious emissions etc., the external FET circuit shown in Figure 30 must be used. See AMCC application note *S3086 Design Recommendations (AN1239)* for details. For required REFCLK frequencies, see Table 6. **This input must be AC coupled (0.01 µF)**.

Frequency Band Select (BAND_SEL [4:0])

The BAND_SEL pins are LVTTL inputs that program the expected incoming data rate (Consult Table 6 for Band Select settings) of the S3086. These input pins may be configured statically before boot-up or dynamically after boot-up. If these pins are to be configured dynamically, several restrictions apply to guarantee the proper operation of the device.

- These select lines may only be changed at a rate greater than $1/T_{LOCK}$. Consult Table 16 for T_{LOCK} requirements.
- Signal Detect (SD) should be set inactive (loss of light condition present) prior to changing the frequency bands. This can be accomplished by programing the SD input inactive if SD is being driven from an FPGA or similar digital logic device. If SD is being driven directly from an optics device, the unused SD input may be reconfigured to create a loss of light condition even when the optics are indicating light is present or not present. Consult tables 2 and 3 for SD configuration settings. SD may be returned to the active setting 1250 ms after BAND_SEL has been programed to the proper value.
- If operating in Non Refclk Mode (REFCLK input disabled by tying REFCLK input low and/or SER_CLK_EN=0) a gate is required across CAP1/2 as shown in Figure 30. This will discharge the filter capacitors when changing frequency bands. Consult Figure 30 and application note *S3086 Design Recommendations (AN1239)* for recommendations and the desired application circuit.

The Frequency Band Select pins are internally pulled high and will default to 1.986-2.700 Gbps (OC-48 + FEC) operation when not connected. NOTE: If operating the S3086 while the REFCLK input is not disabled (REFCLK inputs are not tied low), frequency excursions on the REFCLK input must stay with-in the selected frequency band for proper device operation.

For any deviation from these recommended guidelines the external FET circuit shown in Figure 30 may be required. Consult AMCC application note *S3086 Design Recommendations (AN1239)* for details.

Serial Clock Output Enable (SER_CLK_EN)

This LVTTL input is active High and is used to select between the two modes of operation. When inactive and valid serial data is no longer present, or signal detect is inactive, the serial clock output will not be maintained. Conversely, when active, the SER_CLK_EN will be maintained under the same conditions since the PLL will lock to the reference clock to maintain the serial clock output. If SER_CLK_EN is High, a reference clock must be provided (19.44 MHz or 155.52 MHz for SONET traffic or user defined for non-SONET traffic). This input is internally pulled High. See Table 4.

Table 4. Serial Clock Output Enable

SER_CLK_EN	REFCLK Mode
0	NO REFCLK Required
1	REFCLK Required

Bypass (BYPASS)

This LVTTL input is active High. When active, this input is used to bypass the PLL, which allows transmission of data without clock recovery. This should be used if data rates less than 30 Mbps are transmitted but may also be used for data rates up to and including 2.7 Gbps. In BYPASS mode LOL is always active. This input is internally pulled High.

Reference Select (REFSEL)

This LVTTL input determines whether the REFCLK input frequency is used as is or as a divide-by-8 version when used internally. This input is internally pulled High. For SONET rates, REFSEL = 1 requires a 155.52 MHz REFCLK. For REFSEL = 0, a 19.44 MHz REFCLK is required. See Table 5.

Table 5. Reference Select

REFSEL	Reference Frequency
0	REFCLK Input
1	REFCLK Input ÷ 8

Loop Filter (CAP1, CAP2)

The external loop filter capacitor and resistors are connected to these pins. These devices should be surrounded by a non-contiguous ground shield.

During layout, care should be taken to:

- Minimize trace lengths from the CAP1 and CAP2 pins to off-chip passives, to keep parasitic inductances low and coupling of external noise sources to a minimum.
- Keep traces approximately balanced and symmetrical.

Such practices help ensure predictable PLL responses to data rate changes and minimize random jitter.

Resistor and capacitor values should be as shown in Figure 30.

Factory Test (TESTEN, TESTCLK)

These LVTTL pins are for test factory purposes only. For normal operation, connect to GND. These pins are internally pulled High.

S3086 FUNCTIONAL DESCRIPTION

Clock Recovery

The Phase and Frequency Detector, as shown in the block diagram of Figure 2, generates a clock that is at the same frequency as the incoming data bit rate at the serial data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost. This only occurs when the serial clock output is enabled, SER_CLK_EN = 1.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance that exceeds the minimum tolerance proposed for SONET equipment by the Bellcore TA-NWT-000253 standard, shown in Figure 4.

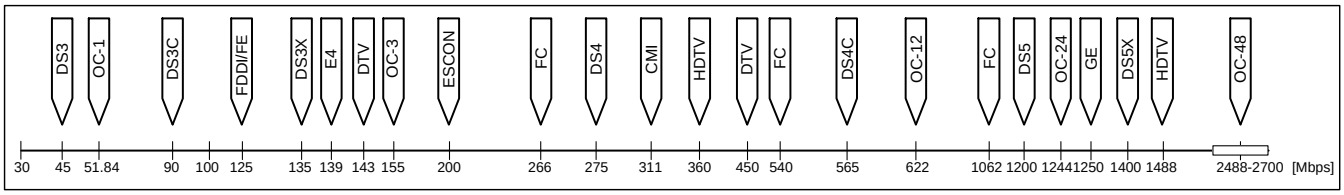
The S3086 PLL must have either a PRBS data or REFCLK to start up. The S3086 will not lock to the square data when SER_CLK_EN is low.

Loss of Lock

If SER_CLK_EN is active, the S3086 enables a lock detect circuit, which monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, the PLL will be forced to lock to the local reference clock, and the Loss-of-Lock (LOL) output will be asserted. This will maintain the correct frequency of the recovered clock output under loss-of-signal or loss-of-lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by more than that stated in Table 16, the PLL will be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within that stated in Table 16, the PLL will be declared in lock and the lock detect output will be de-asserted. The assertion of SDPECLN or SDTTLN will also cause an out-of-lock condition.

During continuous loss of valid data conditions, the LOL output will continuously pulse. When the PLL is locked to the REFCLK input, the LOL output will be de-asserted. Once locked to the REFCLK input, the PLL will poll the input data path for valid data. When none is found, the LOL output will then be re-asserted. This cycle will continue until valid data is found.

Figure 3. Rate Select



Note: The S3086 device has been characterized with standard SONET data patterns and PRBS patterns up to 2^{31}-1. Also, the device has only been tested for SONET, Gigabit Ethernet, Fibre Channel and HDTV Jitter Characteristics.

Table 6. Band Select

BAND_ SEL_4	BAND_ SEL_3	BAND_ SEL_2	BAND_ SEL_1	BAND_ SEL_0	DATA RATE BAND (Mbps)	REQUIRED REFCLK FREQUENCY	
						REFSEL = 0	REFSEL = 1
0	0	0	0	0	Undefined	Undefined	Undefined
0	0	0	0	1	Undefined	Undefined	Undefined
0	0	0	1	0	30 - 33	Data Rate ÷ 2	Data Rate x 4
0	0	0	1	1	31 - 45	Data Rate ÷ 2	Data Rate x 4
0	0	1	0	0	44 - 50	Data Rate ÷ 4	Data Rate x 2
0	0	1	0	1	46 - 52	Data Rate ÷ 4	Data Rate x 2
0	0	1	1	0	50 - 66	Data Rate ÷ 4	Data Rate x 2
0	0	1	1	1	62 - 90	Data Rate ÷ 4	Data Rate x 2
0	1	0	0	0	88 - 100	Data Rate ÷ 8	Data Rate
0	1	0	0	1	92 - 104	Data Rate ÷ 8	Data Rate
0	1	0	1	0	100 - 133	Data Rate ÷ 8	Data Rate
0	1	0	1	1	124 - 181	Data Rate ÷ 8	Data Rate
0	1	1	0	0	177 - 200	Data Rate ÷ 16	Data Rate ÷ 2
0	1	1	0	1	184 - 209	Data Rate ÷ 16	Data Rate ÷ 2
0	1	1	1	0	201 - 266	Data Rate ÷ 16	Data Rate ÷ 2
0	1	1	1	1	248 - 362	Data Rate ÷ 16	Data Rate ÷ 2
1	0	0	0	0	354 - 400	Data Rate ÷ 32	Data Rate ÷ 4
1	0	0	0	1	369 - 419	Data Rate ÷ 32	Data Rate ÷ 4
1	0	0	1	0	402 - 533	Data Rate ÷ 32	Data Rate ÷ 4
1	0	0	1	1	496 - 724	Data Rate ÷ 32	Data Rate ÷ 4
1	0	1	0	0	709 - 801	Data Rate ÷ 64	Data Rate ÷ 8
1	0	1	0	1	738 - 839	Data Rate ÷ 64	Data Rate ÷ 8
1	0	1	1	0	804 -1066	Data Rate ÷ 64	Data Rate ÷ 8
1	0	1	1	1	993 - 1448	Data Rate ÷ 64	Data Rate ÷ 8
1	1	X	0	0	1419 - 1603	Data Rate ÷ 128	Data Rate ÷ 16
1	1	X	0	1	1477 - 1679	Data Rate ÷ 128	Data Rate ÷ 16
1	1	X	1	0	1608 - 2132	Data Rate ÷ 128	Data Rate ÷ 16
1	1	X	1	1	1986 - 2700	Data Rate ÷ 128	Data Rate ÷ 16

X = don’t care.

SONET JITTER CHARACTERISTICS

Performance

The S3086 PLL complies with the jitter specifications proposed for SONET/SDH equipment defined by the Bellcore Specifications: GR-253-CORE, Issue 2C, February 1999 and ITU-T Recommendations: G.958 document when used as specified.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance limits are shown in Figure 4. S3086 jitter tolerance performance is shown in Table 7.

Jitter Transfer

The jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. SONET jitter transfer requirements are shown in Figure 5. The measurement condition is that input sinusoidal jitter be applied up to the mask level in Figure 4. S3086 jitter transfer performance is shown Table 8.

Jitter Generation

The jitter of the serial clock and serial data outputs shall not exceed the value specified in Table 9 when a serial data input with no jitter is presented to the serial data inputs.

Table 7. SONET Jitter Tolerance Performance

Parameter	Min	Typ	Max	Units	Conditions
OC-48/STS-48		0.5		UI (p-p)	1 MHz < f < 20 MHz Data Pattern = 2^7-1 PRBS
OC-12/STS-12		0.6		UI (p-p)	250 kHz < f < 5 MHz Data Pattern = 2^7-1 PRBS
OC-3/STS-3		0.8		UI (p-p)	65 kHz < f < 1 MHz Data Pattern = 2^7-1 PRBS

Table 8. SONET Jitter Transfer Performance

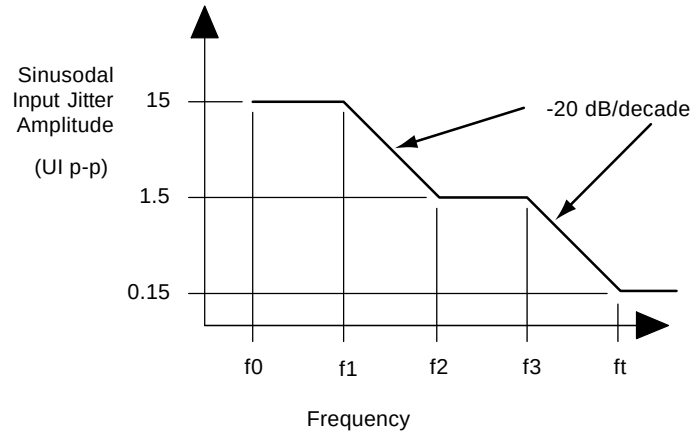
Parameter	Min	Typ	Max	Units	Conditions
OC-48/STS-48			0.1	dB	fc = 2000 kHz
OC-12/STS-12			0.1	dB	fc = 500 kHz
OC-3/STS-3			0.1	dB	fc = 130 kHz

Table 9. SONET Jitter Generation Performance

Parameter	Min	Typ	Max	Units	Conditions
OC-48			0.006	UI (rms)	Data Output Jitter with VCO locked to SERDATIP/N.
OC-12			0.005[1]	UI (rms)	Data Output Jitter with VCO locked to SERDATIP/N.
OC-3			0.005[1]	UI (rms)	Data Output Jitter with VCO locked to SERDATIP/N.

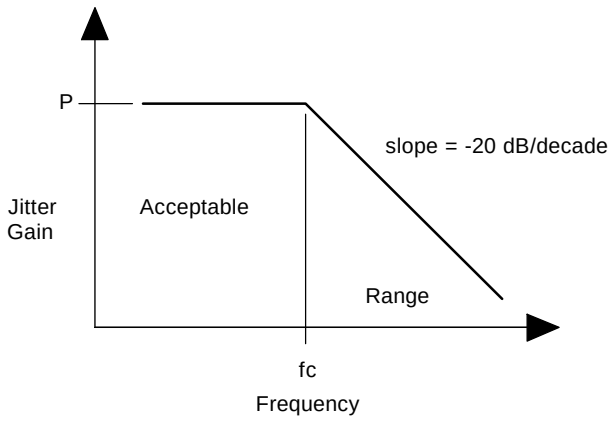
1. Quantity extrapolated from higher rates.

Figure 4. SONET Input Jitter Tolerance Mask Specification



OC/STN Level	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)
48	10	600	6000	100	1000
12	10	30	300	25	250
3	10	30	300	6.5	65

Figure 5. SONET Jitter Transfer Specification



OC/STN Level[1,2]	fc (kHz)	P (dB)
48	2000	0.1
12	500	0.1
3	130	0.1

1. Bellcore Specifications: GR-253-CORE, Issue 2C, February 1999.
2. ITU-T Recommendations: G.958.

FIBRE CHANNEL JITTER CHARACTERISTICS

Performance

The S3086 complies with the jitter specifications proposed for Fibre Channel equipment recommended in "Fibre Channel – Methodologies for Jitter Specification," (FC-MJS, Rev 10).

Input Jitter Tolerance

Input Jitter Tolerance is defined as the ability of the circuit to correctly recover an incoming data stream despite the jitter present. See Figure 6 for the *Fibre Channel Jitter Tolerance Sinusoidal Component Mask*. It is characterized by the amount of jitter required to produce a specified bit error rate. The reference point for jitter tolerance is always at the component receiver node (see Figure 7). The tolerance depends upon the frequency content of the jitter. Table 10 shows the jitter tolerance components.

Figure 6. Fibre Channel Jitter Tolerance Sinusoidal Component Mask

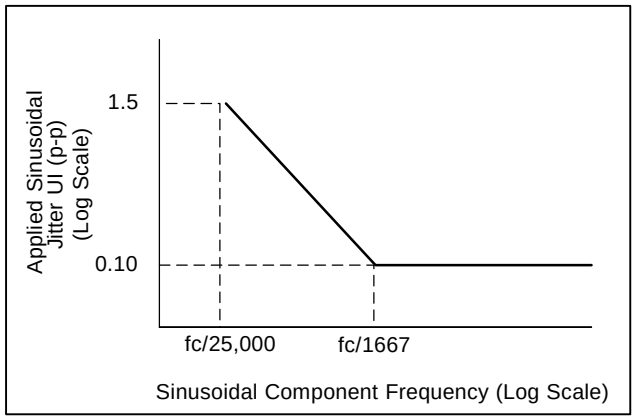
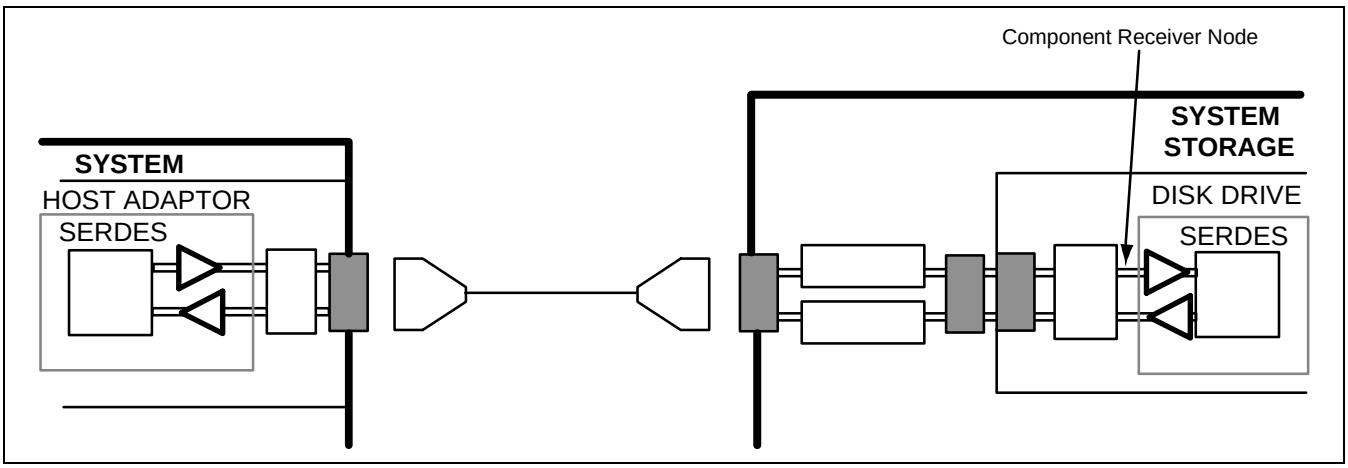


Table 10. Fibre Channel Input Jitter Tolerance Component Specification

Component	UI (p-p)
Sinusoidal Applied Jitter Swept from fc/25,000 to 5 MHz (Example: fc = 1.0625 Gbps; 42.5 kHz to 5 MHz)	See Figure 6.
Nonsinusoidal Deterministic Jitter fc/1667 to fc/2 Majority of Jitter at fc/2 (Example: fc = 1.0625 Gbps; 637 kHz to 531 MHz)	0.38
Random Jitter Bandwidth includes fc/1667 to fc/2 (Example: fc = 1.0625 Gbps; 637 kHz to 531 MHz)	0.22
Sinusoidal > 637 kHz	0.70

Figure 7. Fibre Channel System Node Definition



GIGABIT ETHERNET JITTER CHARACTERISTICS

Performance

The S3086 complies with the jitter specifications proposed for Gigabit Ethernet equipment as defined by the IEEE 802.3z/D4.2 (March 17, 1998) specification.

Input Jitter Tolerance

Input Jitter Tolerance is defined as the ability of the circuit to correctly recover an incoming data stream despite the jitter. It is characterized by the amount of jitter required to produce a specified bit error rate. The reference point for jitter tolerance is always the TP4 point. (See Figure 8.) The tolerance depends upon the frequency content of the jitter. The numbers shown in Table 11 represent high frequency jitter (above 637 kHz) and do not include low frequency jitter or wander.

Jitter Generation

The jitter of the serial data outputs shall not exceed the value specified in Table 12 when serial data with no jitter is presented to the serial data inputs.

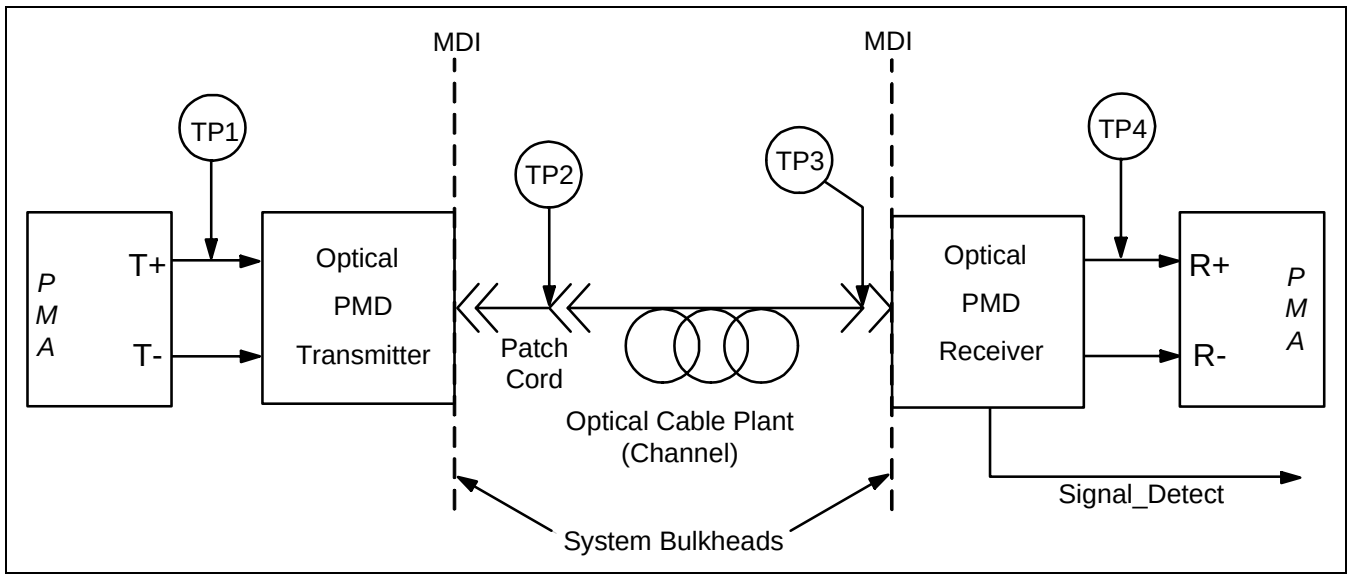
Table 11. Gigabit Ethernet Input Jitter Tolerance Specification

Compliance Point	Total Jitter		Deterministic Jitter	
TP4	UI	psec	UI	psec
	0.749	599	0.462	370

Table 12. Gigabit Ethernet Output Jitter Generation Specification

Compliance Point	Total Jitter		Deterministic Jitter	
TP1	UI	psec	UI	psec
	0.24	192	0.10	80

Figure 8. Gigabit Ethernet System Node Definition



HDTV JITTER CHARACTERISTICS

Performance

The S3086 complies with the jitter specifications proposed for High Definition Serial Digital Interface (HD-SDI) systems as defined by SMPTE 292M-1998 and SMPTE RP184-1996. Jitter is measured with reference to Figure 10 shown below. The required Bit Error Rate (BER) for spec compliance is 1E-14 (using 2^7-1 PRBS).

Jitter Transfer

The jitter transfer function is defined as the ratio on the output signal (Point 3, Figure 9) to the jitter applied on the input (Point 2, Figure 9) versus frequency. HDTV jitter transfer requirements are shown in Figure 10. The measurement condition is that input sinusoidal jitter, up to the mask level in Figure 11, is applied.

Intrinsic Jitter

Intrinsic jitter has two components, alignment and timing jitter, and is measured from point 2 to point 3 on Figure 9. Alignment jitter is the variation in position of a signal's transitions relative to that of the clock that is extracted from that signal. The bandwidth of the clock extraction process determines the low frequency limit for alignment jitter. Timing jitter is the variation in position of a signal's transitions occurring at a rate greater than a specified frequency. Variations below this specified frequency are termed "wander" and are not considered. Figure 12 shows the jitter input mask, and Figure 13 shows the HDTV output timing jitter requirement. Figure 14 shows the alignment jitter input mask and Figure 15 shows the HDTV output alignment jitter requirement.

Figure 9. HDTV Jitter Measurement Points

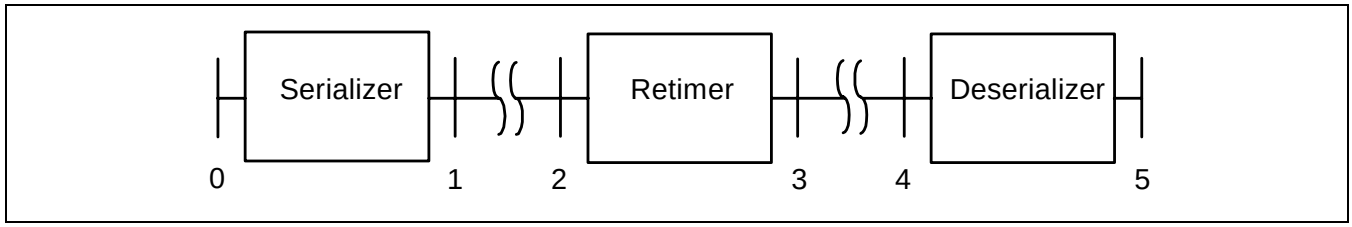


Figure 10. HDTV Jitter Transfer Specification

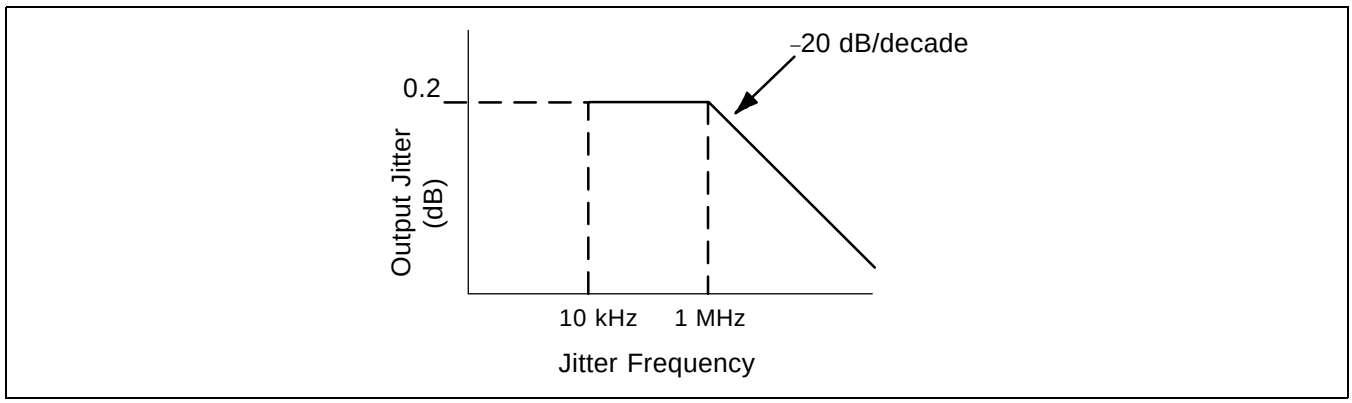


Figure 11. HDTV Input Jitter Tolerance Mask

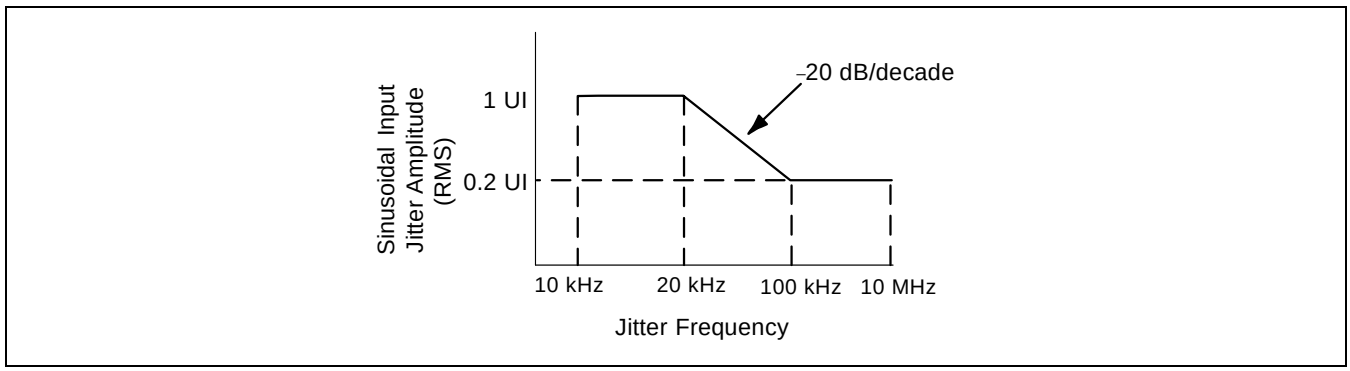


Figure 12. HDTV Timing Jitter Input Mask Specification

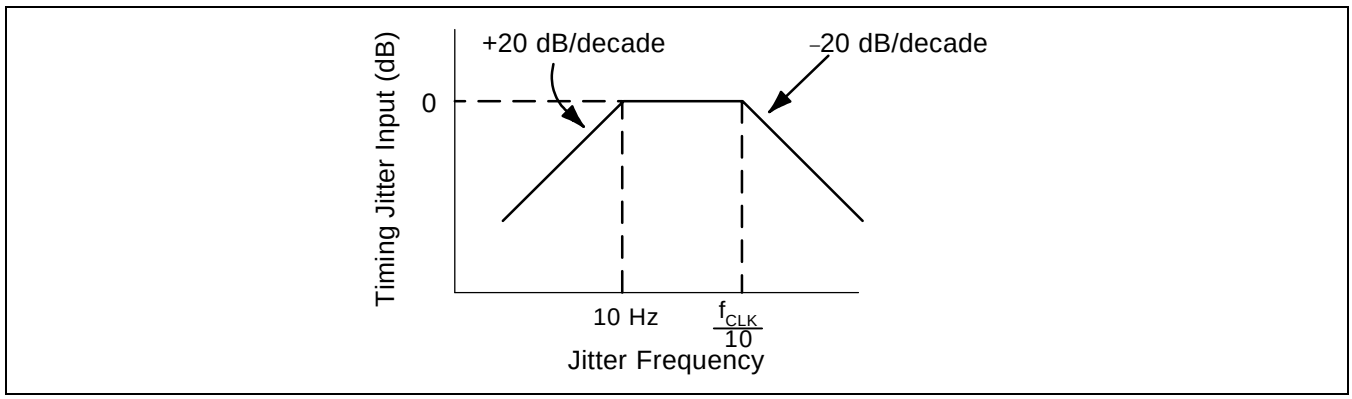


Figure 13. HDTV Output Timing Jitter Specification

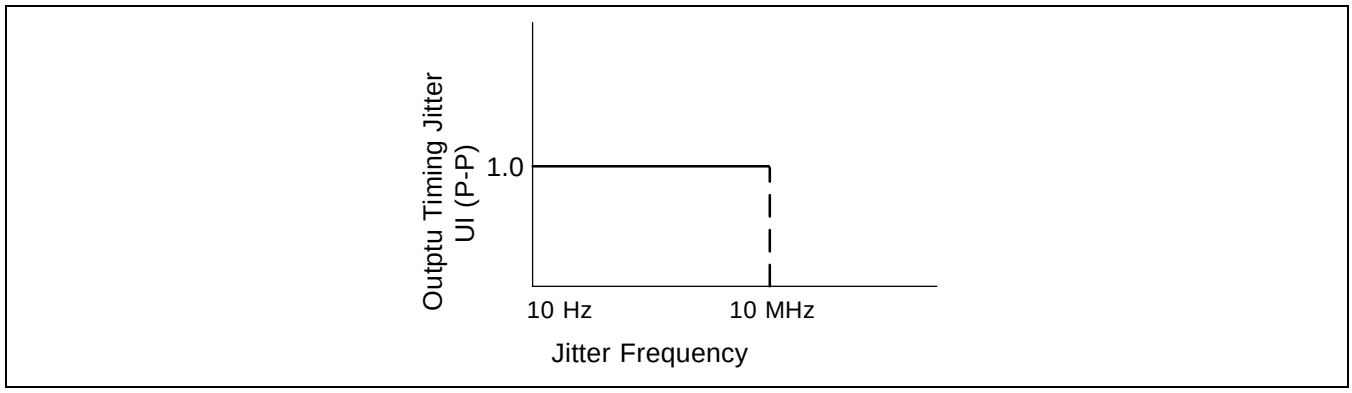


Figure 14. HDTV Alignment Jitter Input Mask Specification

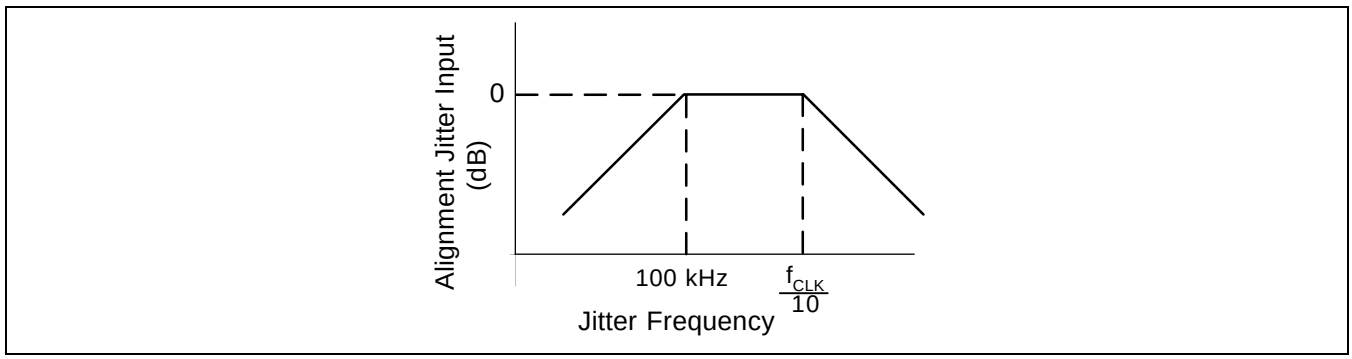
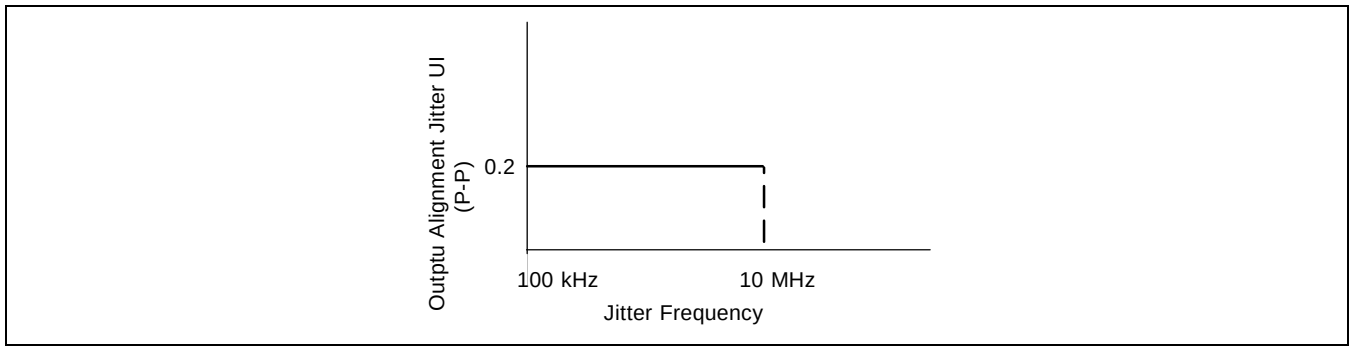


Figure 15. HDTV Output Alignment Jitter Specification



GENERIC PROTOCOL JITTER PEAKING CHARACTERISTICS

Jitter Peaking

Jitter peaking for a given transition density will be specified for those data rates or protocols for which jitter transfer has not been specified. Table 13 below lists the data rates as well as the minimum transition density (unchanging bit times) for which the jitter transfer is 2 dB or less. Changing the external loop filter resistor and capacitor values will bring the transition density to 50% with < 2dB peaking for data rates less than 93 Mbps.

Table 13. Minimum Transition Density for Jitter Transfer Peaking With STS-48 External R and C

Data Rate Band (Mbps)	Minimum Transition Density for which Jitter Gain < 2 dB (Bit Time)	Data Rate Band (Mbps)	Minimum Transition Density for which Jitter Gain < 2 dB (Bit Time)
30 - 33	80%	248 - 362	50%
31 - 45	80%	354 - 400	50%
44 - 50	70%	369 - 419	50%
46 - 52	70%	402 - 533	50%
50 - 66	70%	496 - 724	50%
62 - 90	70%	709 - 801	50%
88 - 100	70%	738 - 839	50%
92 - 104	70%	804 -1066	50%
100 - 133	50%	993 - 1448	50%
124 - 181	50%	1419 - 1603	50%
177 - 200	50%	1477 - 1679	50%
184 - 209	50%	1608 - 2132	50%
201 -266	50%	1986 - 2700	50%

Note: The loop filters in Figure 30 have been optimized for STS-48/24/12/3 operation. Refer to the PLL calculator CALC1207 for the approximate loop jitter value for the other rates. The user may have to further optimize the loop filters values depending upon the specific application. Peaking can be minimized and the transition density can be reduced to 50% (for data rates less than 93 Mbps) with an optimized loop jitter value for each rate.

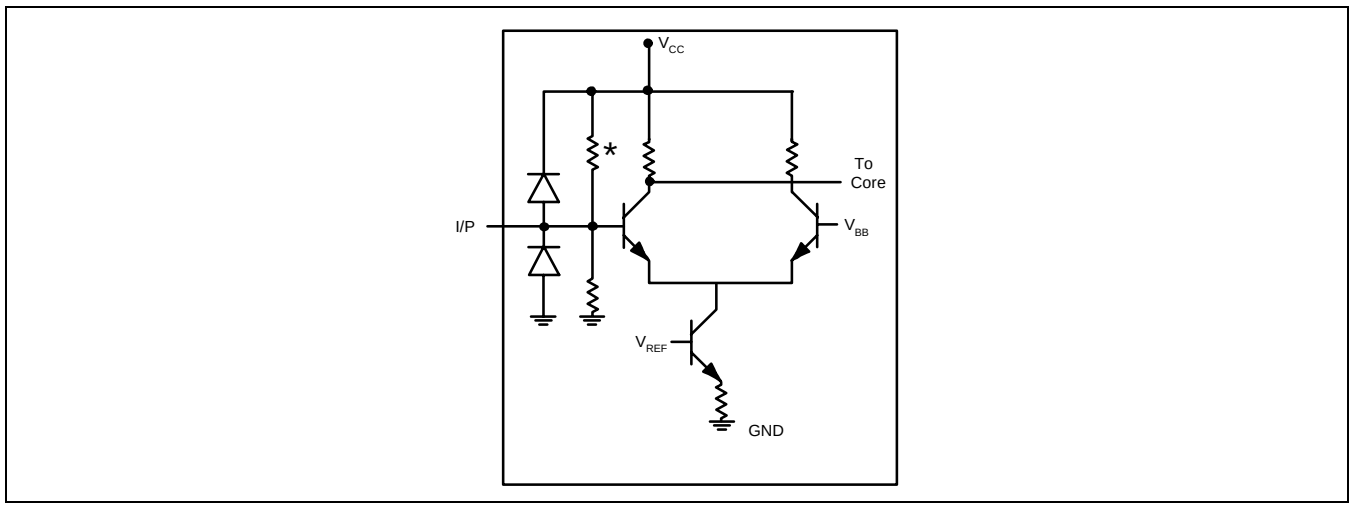
Table 14. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
SERDATIP SERDATIN	Diff. CML	I	3 2	**Serial Data In.** The embedded clock is recovered from the transitions on these inputs. Internally biased and terminated.
BYPASS	LVTTL	I	46	**Bypass.** Active High. This input, when active, is used to bypass the PLL. It allows transmission of data without clock recovery. Typically used for data rates less than 30 Mbps but may also be used for data rates up to and including 2.7 Gbps. This input is internally pulled High.
SDPECLN	Single-Ended LVPECL	I	45	**Signal Detect.** A single-ended 10K PECL input to be driven by the external optical receiver module to indicate a loss of received optical power. This input may be utilized by an optics module with either an active Low for loss of light or active High for loss of light. For an active High optics module, SDTTLN must remain unconnected. For an active Low optics module, the SDTTLN input must be connected to GND. The optics module LVPECL signal detect output may be directly connected to the S3086 SDPECLN input. This input is internally pulled Low. When a loss-of-light condition occurs the internal PLL will be forced to lock to the REFCLK input signal if SER_CLK_EN is asserted High. Internally biased.
SDTTLN	LVTTL	I	7	**Signal Detect.** A Single-Ended LVTTL input to be driven by the external optical receiver module to indicate a loss of received optical power. This input may be utilized by an optics module with either an active Low for loss of light or active High for loss of light. For an active Low optics module, SDPECLN must remain unconnected. For an active High optics module, the SDPECLN input must be pulled High through a 1 kΩ resistor. The optics module LVTTL signal detect output may be directly connected to the S3086 SDTTLN input. This input is internally pulled High. When a loss-of-light condition occurs, the internal PLL will be forced to lock to the REFCLK input signal if SER_CLK_EN is asserted High.
REFCLK	Single-Ended LVPECL	I	6	**Reference Clock.** This input is used to establish the initial operating frequency of the clock recovery PLL and is also used as a standby clock in the absence of data during reset or when SDTTLN or SDPECLN is asserted during loss of light conditions. Internally biased. This input must be AC coupled (0.01 µF).
CAP1 CAP2	Analog	I	40 39	**Loop Filter.** The PLL external loop filter capacitor and resistors are connected to these pins (See Figure 30.) This circuitry should be surrounded by a non-contiguous ground shield.
TESTCLK	LVTTL	I	15	**Test Clock.** Test input signal used for production test. Connect to GND for normal operation. This input in internally pulled High.
TESTEN	LVTTL	I	47	**Test Enable.** Active High. Test input signal used for production test. Connect to GND for normal operation. This input is internally pulled High.
REFSEL	LVTTL	I	18	**Reference Select.** Selects the Reference Frequency input division utilized internally. 0: Internal Reference = REFCLK, 1: Internal Reference = REFCLK/8. For SONET rates REFSEL = 1 requires a 155.52 MHz REFCLK and REFSEL = 0 requires a 19.44 MHz REFCLK. This input is internally pulled High.
BAND_SEL_0 BAND_SEL_1 BAND_SEL_2 BAND_SEL_3 BAND_SEL_4	LVTTL	I	16 17 19 20 23	**Band Select.** Selects the operating band. (See Table 6.) These are internally pulled High.

Table 14. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
SER_CLK_EN	LVTTL	I	8	**Serial Clock Enable.** Active High. This input is used to select between the two modes of operation. When inactive, the serial clock output is not maintained if serial data is no longer present or signal detect has been asserted. When active, the serial clock output will be maintained if serial data is no longer present or signal detect has been asserted. If SER_CLK_EN is High, a reference clock must be provided (19.44 MHz or 155.52 MHz for SONET traffic or user defined for non-SONET traffic). When the PLL is locked to the REFCLK, the serial data inputs will be polled for data activity. If no activity is found, the PLL will remain locked to the REFCLK input. This input is internally pulled High.
SERDATOP SERDATON	Diff. CML	O	28 27	**Serial Data Out.** This signal is the delayed version of the incoming data stream (SERDATIP/N) updated on the falling edge of Serial Clock Out (SERCLKOP/N).
SERCLKOP SERCLKON	Diff. CML	O	34 33	**Serial Clock Out.** This signal is phase aligned with Serial Data Out (SERDATOP/N). This output may be disabled by connecting pins 32 and 35 to GND.
LOL	LVCMOS	O	10	**Loss of Lock.** Active Low. Clock recovery indicator. This signal is inactive when the internal clock recovery has locked onto the incoming data stream. LOL is an asynchronous output.
AVCC	+3.3 V	PWR	37, 42	**Analog power supply.** ± 5% tolerance.
AGND	GND	PWR	38, 41, 43	Ground.
VCC	+3.3 V	PWR	1, 5, 9, 21, 24, 26, 29, 32, 35, 48	**Digital Power Supply.** ± 5% tolerance.
GND	GND	PWR	4, 11, 12, 13, 14, 22, 25, 30, 31, 36, 44	Ground.

Figure 16. LVPECL Input Buffer



* Not present at SDPECLN input.

Figure 17. LVCMOS Output Buffer

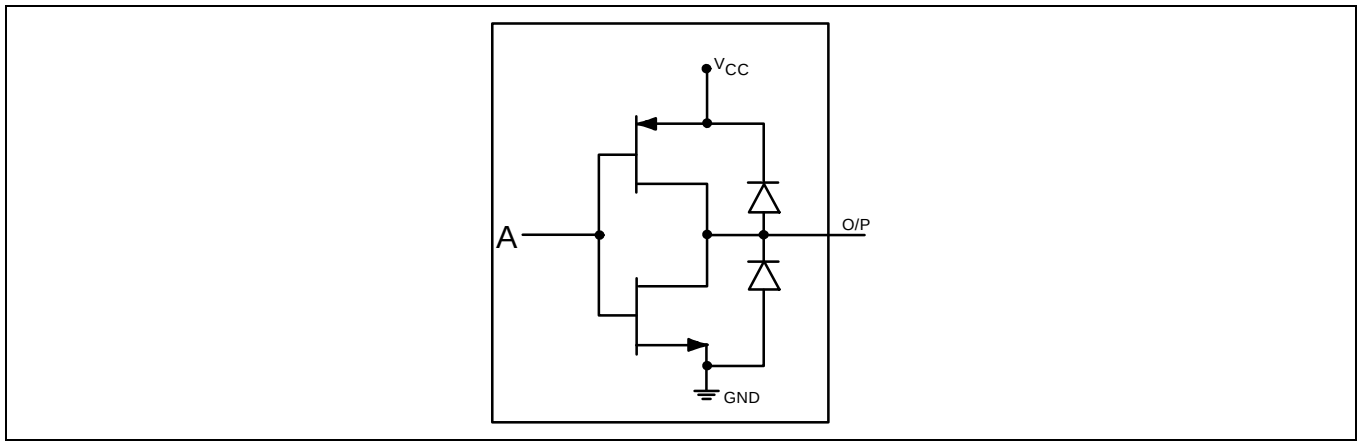


Figure 18. LVTTL Input Buffer

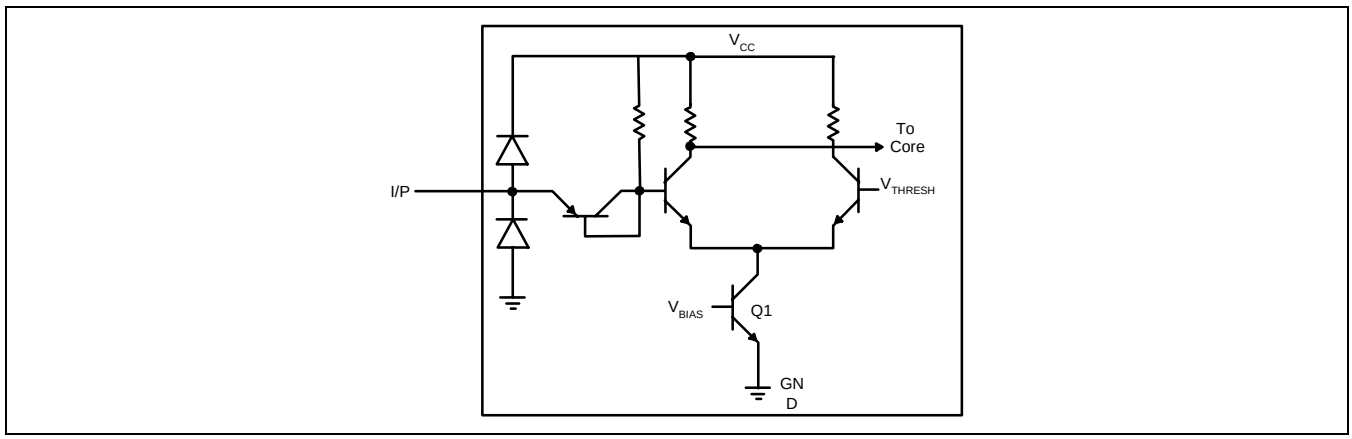


Figure 19. CML Output Buffer

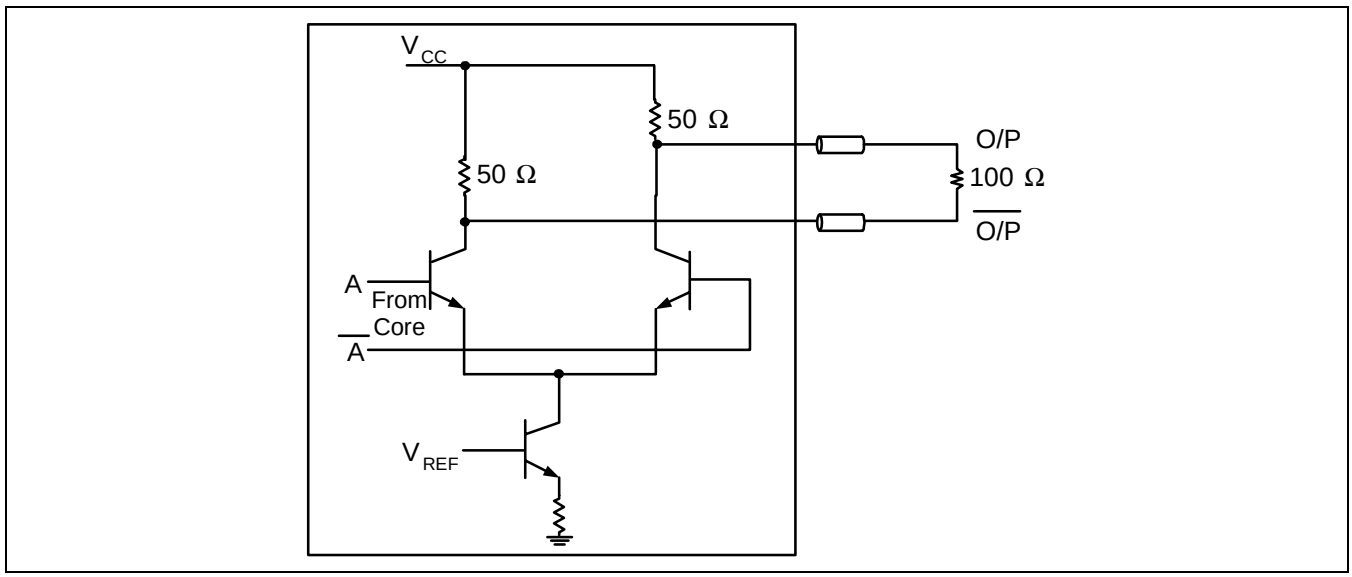


Figure 20. CML Input Buffer

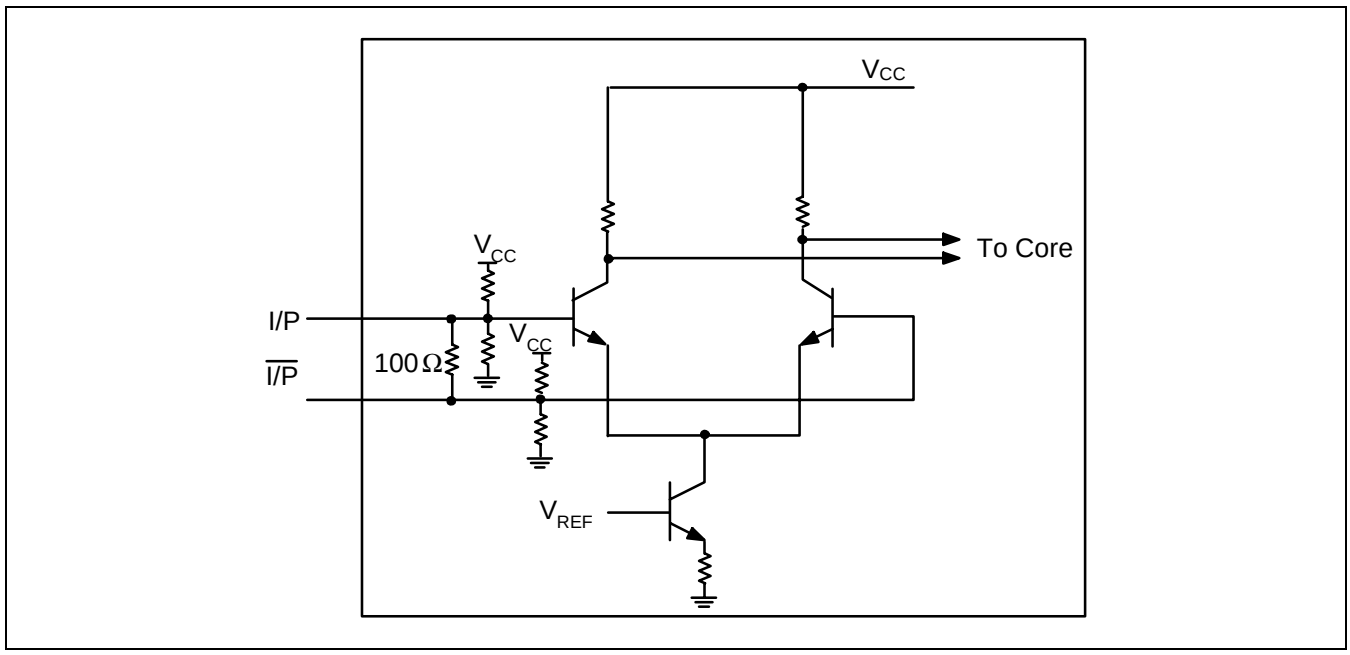


Figure 21. S3086 48-Pin TQFP/TEP Pinout

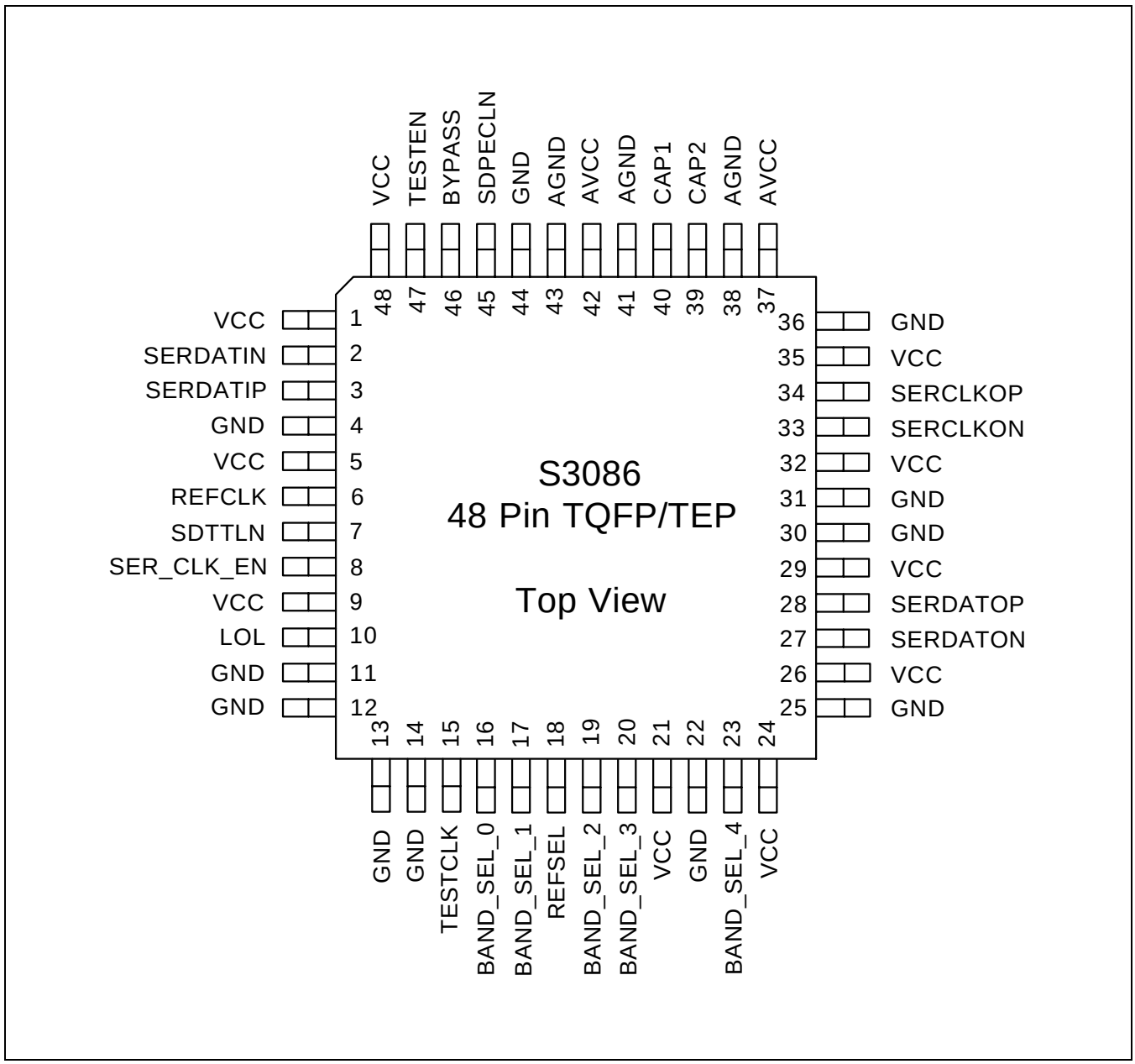
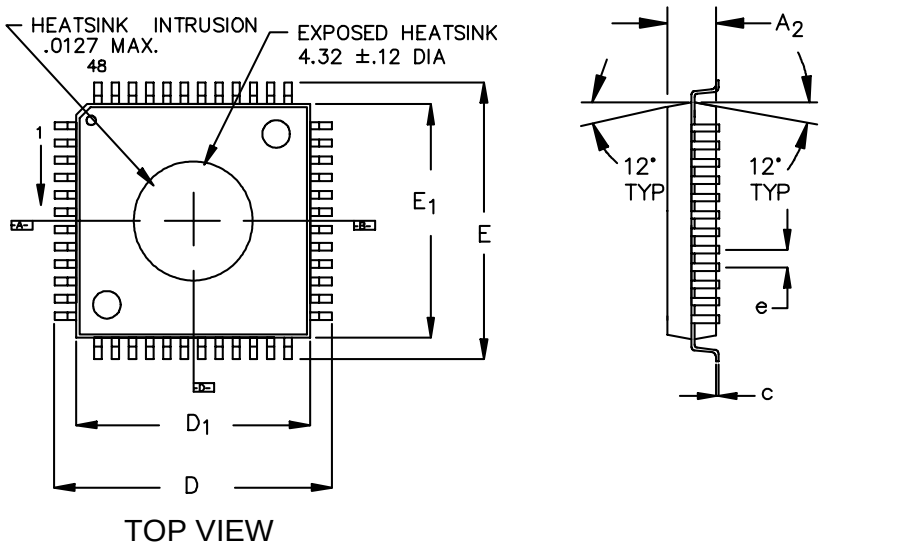
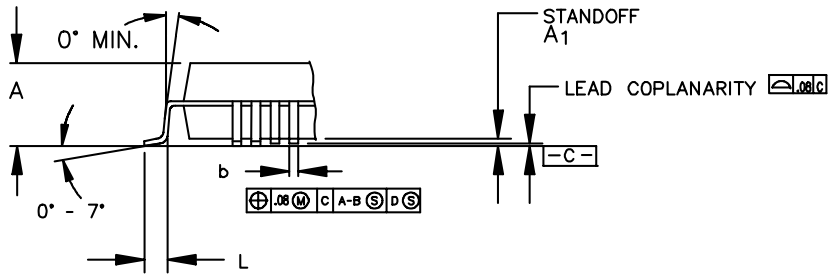


Figure 22. 48-Pin TQFP/TEP Package





DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.05	1.35	8.80	6.90	8.80	6.90	0.75	0.50 BSC.	0.17	
NOM			1.40	9.00	7.00	9.00	7.00	0.60		0.22	1.27
MAX	1.60	0.15	1.45	9.20	7.10	9.20	7.10	0.50		0.27	

Note: Exposed heatsink can be connected directly to ground.

Table 15. Thermal Management

Device	Package Max Power	θja	θjc	θjb
S3086	800 mW - 85°C Ambient	50°C/W	6.8°C/W	28.9°C/W
	1100 mW - 70°C Ambient			

Table 16. Performance Specifications

Parameter	Min	Typ	Max	Units	Conditions
Output Clock Rate	30		2700	MHz	
Reference Clock Frequency Tolerance	-100		+100	ppm	REFCLK input requirement to meet SONET specifications is ±20 ppm.
Frequency Difference at which all PLL goes into lock		±488		ppm	
Frequency Difference at which all PLL comes out of lock		±488		ppm	
Phase Acquisition Lock Time (T_{LOCK})		700	1250	ms	Minimum transition density of 20% PRBS or with REFCLK if square data. Guaranteed but not tested. With device already powered up and valid REFCLK.
Reference Clock Input Duty Cycle	40		60	% of UI	
Reference Clock Rise and Fall Times 155.52 MHz 19.44 MHz			 1.5 12.0	ns	20% to 80% of amplitude.
155.52 MHz REFCLK Phase Noise requirement to meet SONET spec on SERCLKO.			-102	dBc/Hz	@ 10 kHz offset from carrier.
19.44 MHz REFCLK Phase Noise requirement to meet SONET spec on SERCLKO.			-120	dBc/Hz	@ 10 kHz offset from carrier.
CML Output Rise and Fall Times		60	100	ps	20% to 80%, 100 Ω load line to line.
Setup Time (t_{SU})	142			ps	See Figure 23.
Hold Time (t_H)	167			ps	See Figure 23.
Power Supply Noise Rejection (PSNR)			50	mV	12 kHz to 20 MHz Bandwidth

Note: The performance specifications have been characterized for SONET STS-48 rates only.

Table 17. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Junction temperature under bias			125	°C
Ambient Temperature Under Bias[1]	-40		+70	°C
Ambient Temperature Under Bias with Heatsink and 150 LFPM Airflow[1,2]	-40		+85	°C
Voltage on V_{CC} with respect to GND	3.135	3.3	3.465	V
Voltage on any CML Input Pin	0		V_{CC}	
Voltage on any LVTTL Input Pin	0		V_{CC}	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
Digital I_{CC} Supply Current[3]		125	155.5	mA
Analog I_{CC} Supply Current[3]		125	155.5	mA

1. Excluding cold start conditions.
2. Use Thermal extrusion #11087.
3. Outputs open and serial clock enabled.

Table 18. Absolute Maximum Ratings

The following are the absolute maximum stress ratings for the S3086 device. Stresses beyond those listed may cause permanent damage to the device. Absolute maximum ratings are stress ratings only, and operation of the device at the maximums stated or any other conditions beyond those indicated in the “Recommended Operating Conditions” of the document are not inferred. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		+150	°C
Voltage on V_{CC} with respect to GND	-0.5		3.465	V
Voltage on any CML Input Pin	-0.5		V_{CC} +0.5	V
Voltage on any LVTTL Input Pin	-0.5		V_{CC} +0.5	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
LVCMOS Output Source Current			1	mA
LVCMOS Output Sink Current			1	mA
LVTTL Output Sink Current			8	mA
LVTTL Output Source Current			8	mA
LVPECL Output Sink Current			15	mA
LVPECL Output Source Current			15	mA
Power Dissipation[1]		825	1077	mW
Power Dissipation[2]		700	927	mW

1. With serial clock enabled and powered.
2. With serial clock disabled.

Electrostatic Discharge (ESD) Rating:
All pins are rated at 1500 V. (human body model)

Figure 23. Typical Waveform

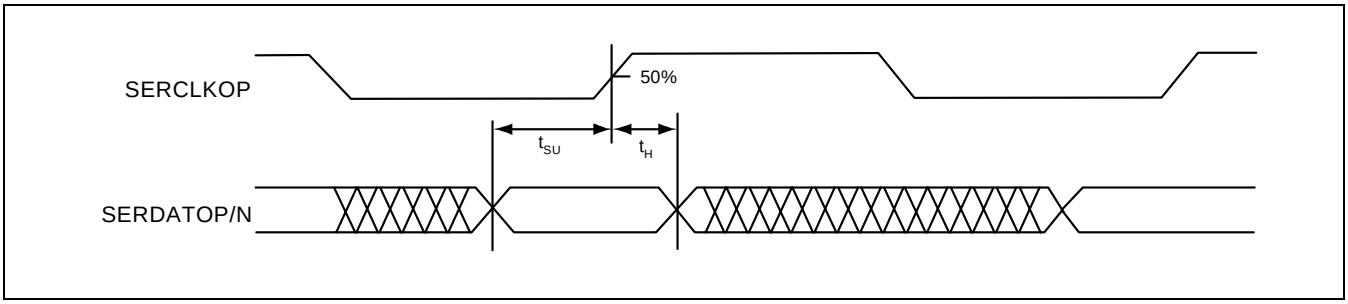


Table 19. CML Input DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	CML Input Low Voltage	V_{CC} -2.0			V	
V_{IH}	CML Input High Voltage			V_{CC} -0.2	V	
V_{IDIFF}	Differential Input Voltage Swing	100		1900	mV	See Figure 24.
$V_{ISINGLE}$	Single-ended Input Voltage Swing	50		950	mV	See Figure 24.
R_{IDIFF}	Differential Input Resistance	80	100	120	Ω	

Table 20. CML Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
$V_{OL(DATA)}$	Output Low Voltage	V_{CC} -1.0		V_{CC} -0.65	V	100 Ω line-to-line.
$V_{OH(DATA}$	Output High Voltage	V_{CC} -0.35		V_{CC} -0.2	V	100 Ω line-to-line.
$V_{ODIFF(DATA)}$	Serial Output Differential Voltage Swing (V+ to V-)	800		1600	mV	100 Ω line-to-line. See Figure 24.
$V_{OSINGLE(DATA)}$	Serial Output Single-ended Voltage Swing (V+ or V- to GND)	400		800	mV	100 Ω line-to-line. See Figure 24.
$R_{ODIFF(DATA)}$	Differential Output Resistance	80	100	120	Ω	
$V_{OL(CLOCK)}$	Output Low Voltage	V_{CC} -1.5		V_{CC} -0.85	V	100 Ω line-to-line.
$V_{OH(CLOCK)}$	Output High Voltage	V_{CC} -0.50		V_{CC} -0.25	V	100 Ω line-to-line.
$V_{ODIFF(CLOCK)}$	Serial Output Differential Voltage Swing (V+ to V-)	800		1800	mV	100 Ω line-to-line. See Figure 24.
$V_{OSINGLE(CLOCK)}$	Serial Output Single-ended Voltage Swing (V+ or V- to GND)	400		900	mV	100 Ω line-to-line. See Figure 24.
$R_{ODIFF(CLOCK)}$	Differential Output Resistance	80	100	120	Ω	

Table 21. LVTTL Input DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	2.0		3.465	V	LVTTL V_{CC} = Max
V_{IL}	Input Low Voltage	0		0.8	V	LVTTL V_{CC} = Max
I_{IH}	Input High Current			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current	-500			µA	V_{IN} = 0.5 V

Note: All parameters are specified with respect to the source termination and ground with LVTTL = Max. = 3.465 V.

Table 22. LVCMOS Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -0.03 mA
V_{OL}	Output Low Voltage			0.5	V	I_{OL} = 1 mA

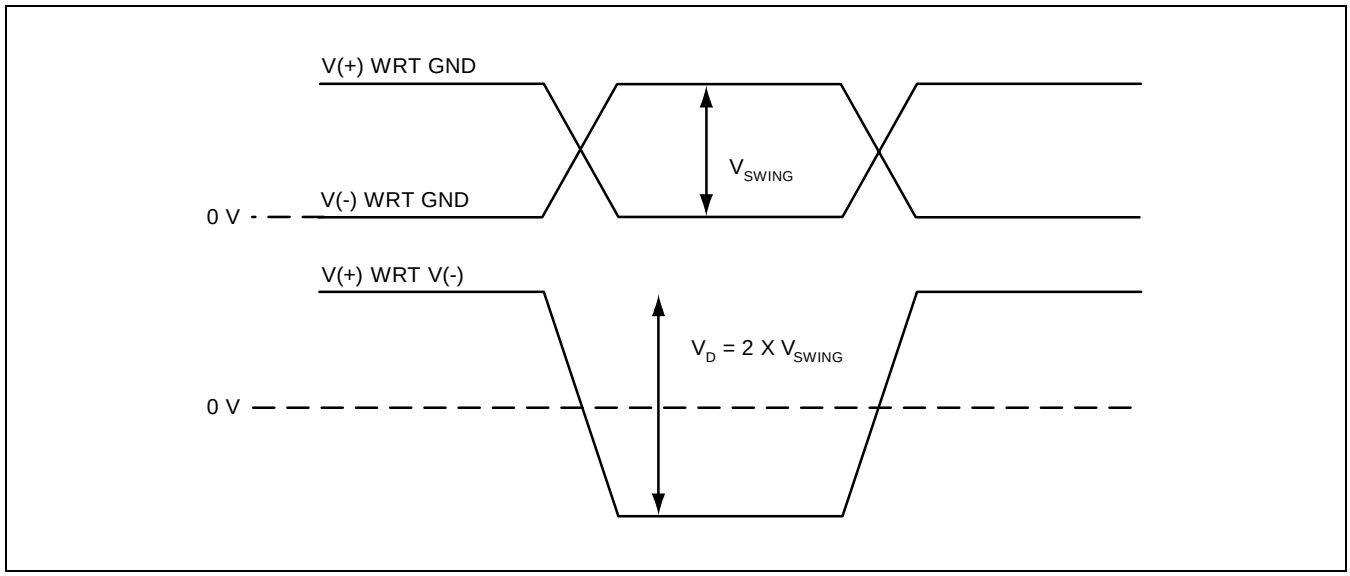
Table 23. Single Ended LVPECL Input DC Characteristics (SDPECLN Only)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage	V_{CC} -2.0		V_{CC} -1.4	V	
V_{IH}	Input High Voltage	V_{CC} -1.2		V_{CC} -0.5	V	
I_{IL}	Input Low Current	-100		0	µA	V_{CC} -2.0 V
I_{IH}	Input High Current	50		350	µA	V_{CC} -0.5 V

Table 24. Single Ended LVPECL Input DC Characteristics (REFCLK Only)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage	V_{CC} -2.0		V_{CC} -1.4	V	
V_{IH}	Input High Voltage	V_{CC} -1.2		V_{CC}	V	
V_{IB}	Internal Bias Voltage Range	V_{CC} -0.95		V_{CC} -0.45	V	
I_{IL}	Input Low Current	-220		-50	µA	V_{CC} -2.0 V
I_{IH}	Input High Current	-20		50	µA	V_{CC} -0.5 V

Figure 24. Differential Voltage Measurement



Note: WRT = With Respect to.

Figure 25. +5 V Differential PECL Driver to S3086 Differential CML Input AC Coupled Termination

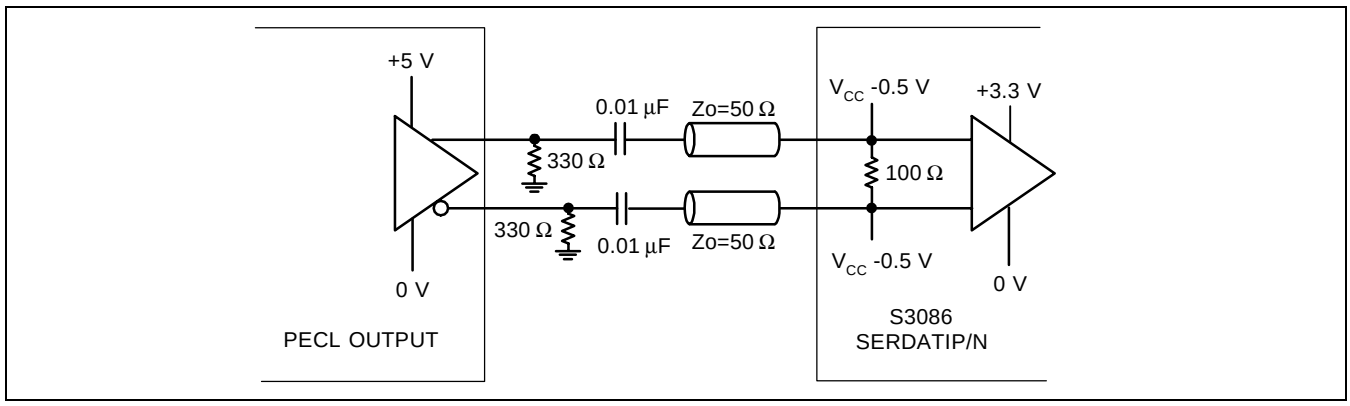


Figure 26. S3086 Differential CML Output to S3057/S3067 CML Input Terminations

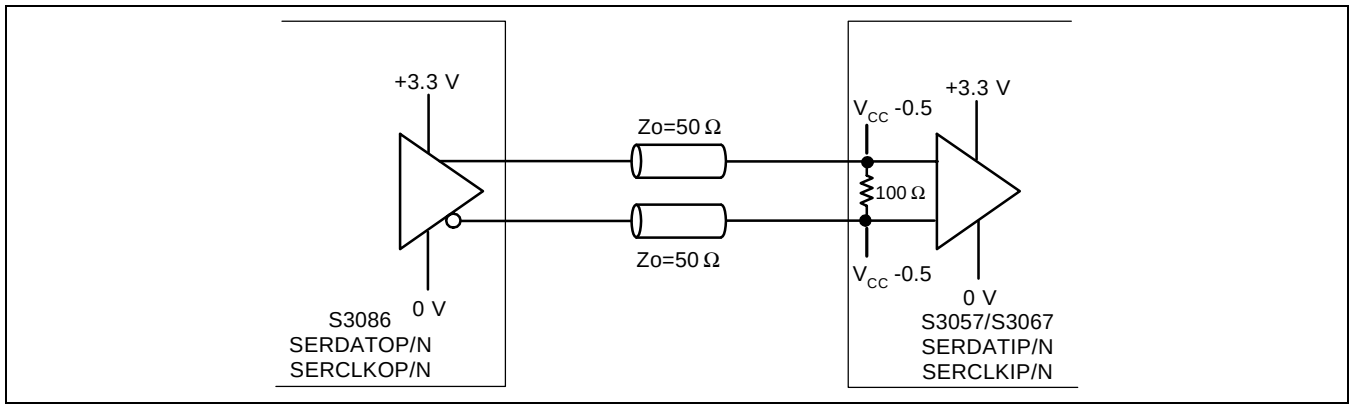


Figure 27. S3086 Differential CML Output to LVDS Input Termination

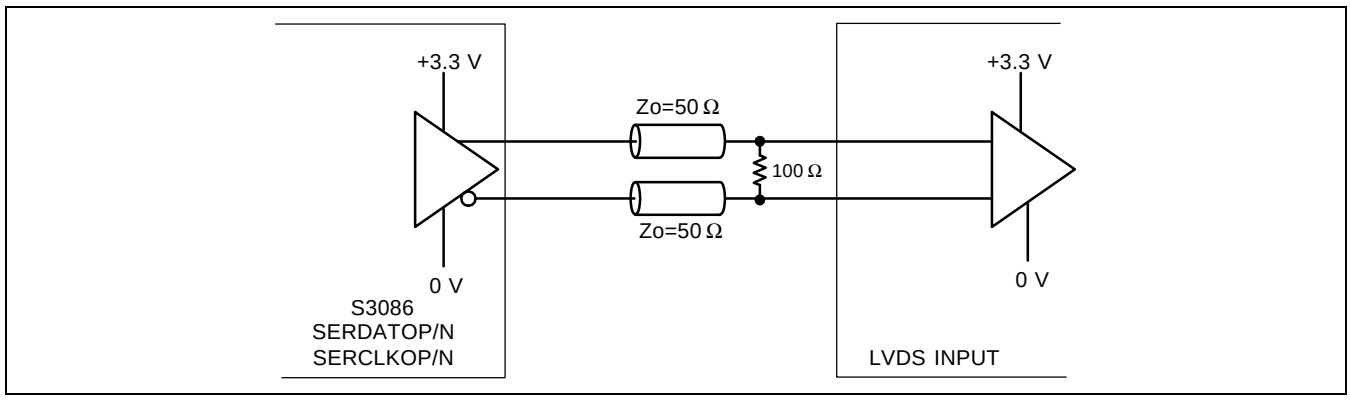


Figure 28. LVDS Output to S3086 Differential CML Input AC Coupled Termination

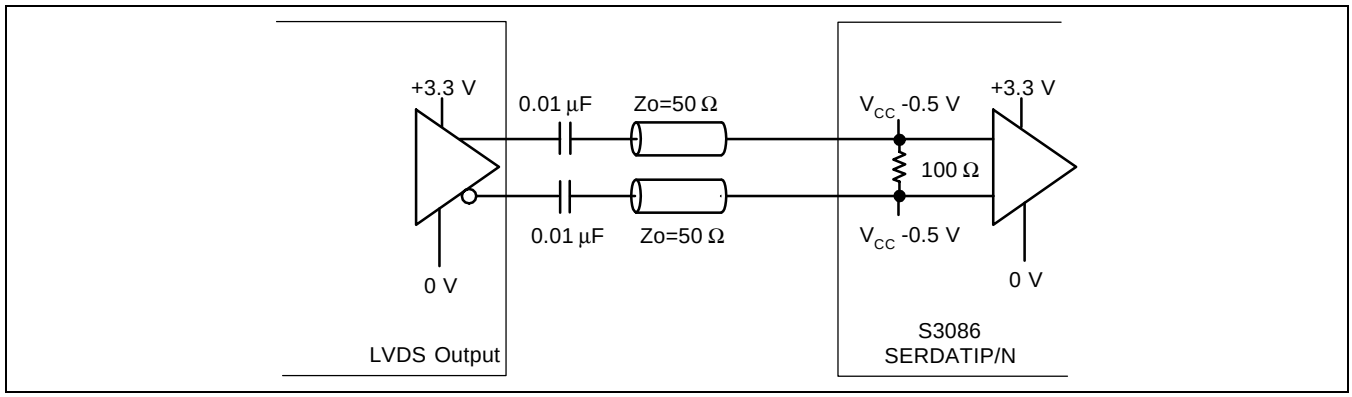


Figure 29. +3.3 V Differential LVPECL Driver to S3086 Reference Clock Input AC Coupled Termination

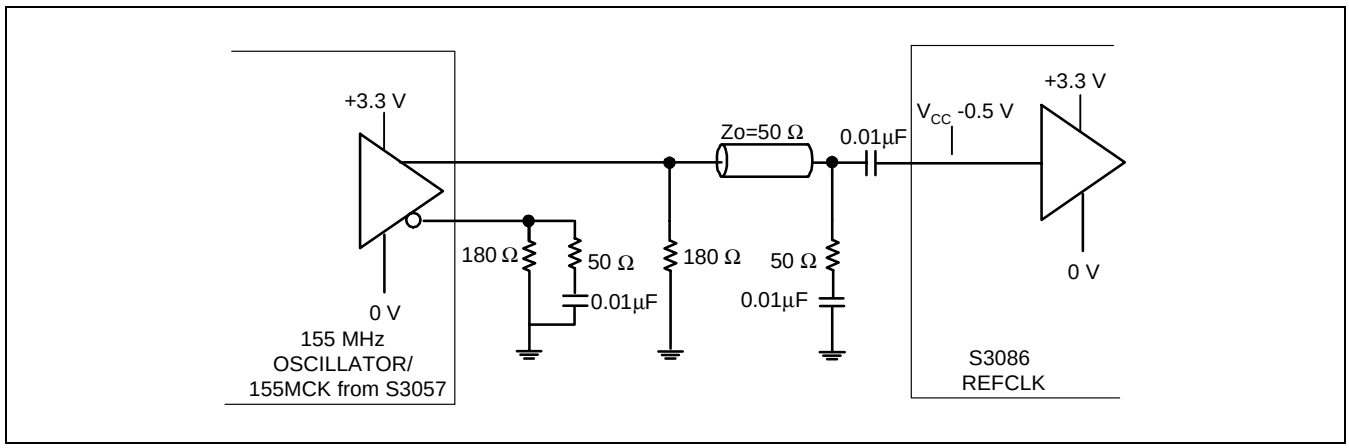
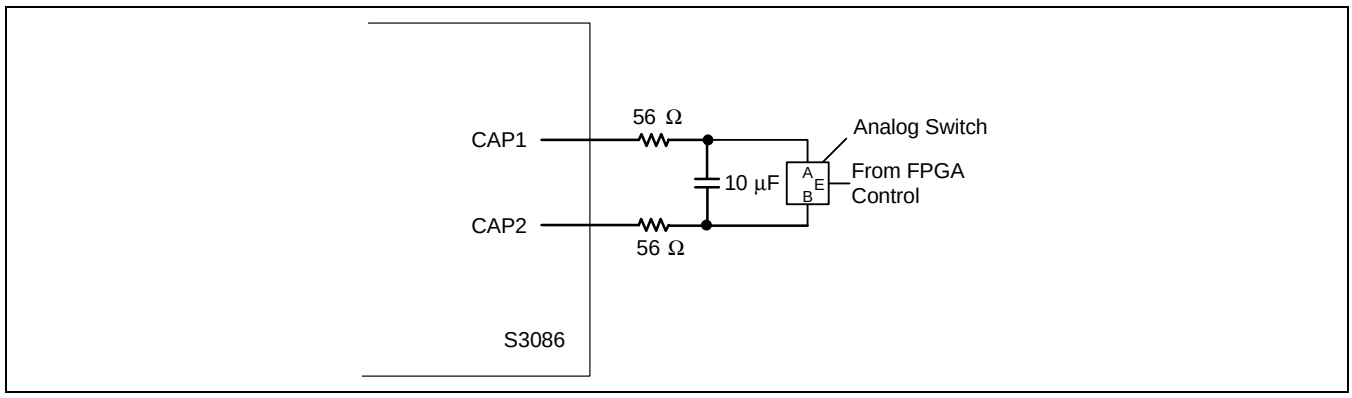


*Figure 30. Loop Filter Capacitor Connections**



* Loop filters optimized for STS-3/12/48 operation.

* Refer to the PLL calculator CALC1207 for the optimal loop jitter value for other rates.

* The analog switch is required to change bands when using the S3086 device in non-REFCLK mode. An ideal switch should be CMOS compatible, ultra high-speed, single pole/1-bit bus switch. The ON resistance of the switch should be low, so that the input can be connected to the output with minimal propagation delay. The switch enable (E) can be controlled from an FPGA before changing the data rate. When E is High, the switch is ON, and the capacitor is discharged, thus enabling the S3086 device to configure to the new incoming rate.When E is Low, the switch is open and a high-impedance state exists between the parts A and B. AMCC has demonstrated capability with FAIRCHILD SEMICONDUCTOR® NC75266.FSA66 and PHILLIPS SEMICONDUCTOR® 74LVC1G66 analog switches. The user may want to further investigate for their specific application requirements.

DOCUMENT REVISION HISTORY

Revision	Date	Description
A	2/19/03	- Pg 1, Features updated with new Serial Clock Disabled typical power (to 700 mW from 425 mW) - Pg 5, Figure 1, AC coupling caps added to S3086 REFCLK inputs - Pg 6, Figure 2, pull-up added to REFCLK input - Pg 7, Paragraph 3, typical power saving updated (to 125 mW from 150 mW) - Pg 7, Paragraph 4, wording altered for clarity of Signal Detect function - Pg 7, Tables 2 and 3, wording altered for clarity of Signal Detect function - Pg 7, Table 3, note altered to specify a 1kΩ pull-up - Pg 8, Paragraph 1-3, LOL definition rewritten for clarity of function - Pg 8, Paragraph 4, REFCLK definition rewritten for clarity of function and pull-up changed to 1kΩ from10kΩ - Pg 8, Paragraph 4-9, BAND_SEL definition rewritten for clarity of function - Pg 10, Figure 3, note added to clarify what rates have been tested - Pg 11, Table 6, don't cares added to table for clarity - Pg 19, Table 13, note added to describe how to optimize loop filter values for better transition density response - Pg 20, Table 14, Signal Detect pull-up changed from 10kΩ to 1kΩ - Pg 21, Table 14, Serial Clock Enable description fix - input changed to output - Pg 22, Figure 16, note added to resistor - Pg 22, Figure 18, pull-up added - Pg 23, Figure 20, output moved below resistor for clarity - Pg 25, Table 15, theta JC/JB values added, 70°C max package power added, and note added stating exposed heatsink may be attached directly to ground - Pg 26, Table 16, phase acquisition values changed/added (to 700/1250 ms typ/max from 120 ms typ) - Pg 26, Table 16, note added indicating the only data rate that the product was characterized under - Pg 26, Table 16, Serial Clock Output Frequency Tolerance removed from table - Pg 27, Table 17, Added Junction Temperature Information - Pg 27, Table 18, power dissipation was changed for serial clock disabled mode (to 700/927 mW typ/max from 425/677 mW typ/max) - Pg 31, Figure 29, drawing modified to add clarity to the location of the termination and their configuration - Pg 32, Figure 30, figure altered to add analog switch for CAP1/2 discharging - Pg 32, Figure 30, notes added to indicate operation covered by recommended values, note on how to derive other loop filter values, note on how/when to implement analog switch

Ordering Information

Prefix	Device	Package	Revision
S – Integrated Circuit	3086	TT – 48 Pin TQFP/TEP	11

X	XXXX	XX	XX
Prefix	Device	Package	Revision

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