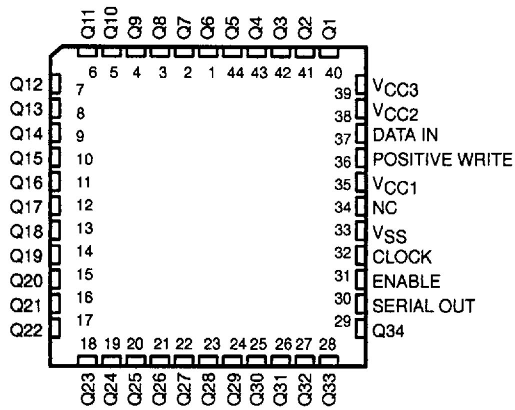
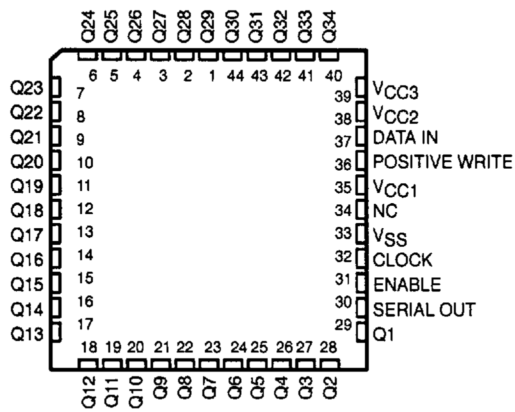
SGLS030 – D3313, OCTOBER 1989

- **Each Device Drives 34 Electrodes**
- **Selectable Open-Source or Open-Drain Output**
- **Outputs Rated at 225 V**
- **Output Current Capability –90 mA to 150 mA**
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

SN55563A . . . FJ PACKAGE (TOP VIEW)



SN55564A . . . FJ PACKAGE (TOP VIEW)



NC – No internal connection

description

The SN55563A, and SN55564A are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible. If POSITIVE WRITE is high, the Q outputs act like open-source outputs and output data is not inverted with respect to input data. If POSITIVE WRITE is low, the Q outputs act like open-drain outputs and output data is inverted with respect to input data. The SN55564A output sequences are reversed from the SN55563A for ease in printed-circuit-board layout.

Typically, composite V_{CC2}, V_{CC3}, and ground signals are externally generated by a high-voltage switching circuit. Serial data is entered into the shift register on the high-to-low transition of CLOCK. A high at the ENABLE input allows those outputs with a high in their associated register to be turned on, causing the corresponding row to be connected to V_{CC2} when POSITIVE WRITE is high or to ground when POSITIVE WRITE is low. V_{CC3} may be tied to V_{CC2} or held 5 V to 15 V above V_{CC2} for better V_{OH} characteristics. SERIAL OUTPUT from the shift register may be used to cascade additional devices. This output is not affected by the ENABLE or POSITIVE WRITE inputs.

The SN55563A and SN55564A are characterized for operation over the full military operating temperature range of –55°C to 125°C.

†BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

LOAD FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R34	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
Load	↓	X	X	Load and shift†	R34	Determined by ENABLE and POSITIVE WRITE
	No ↓	X	X	No change	D34	Determined by ENABLE and POSITIVE WRITE

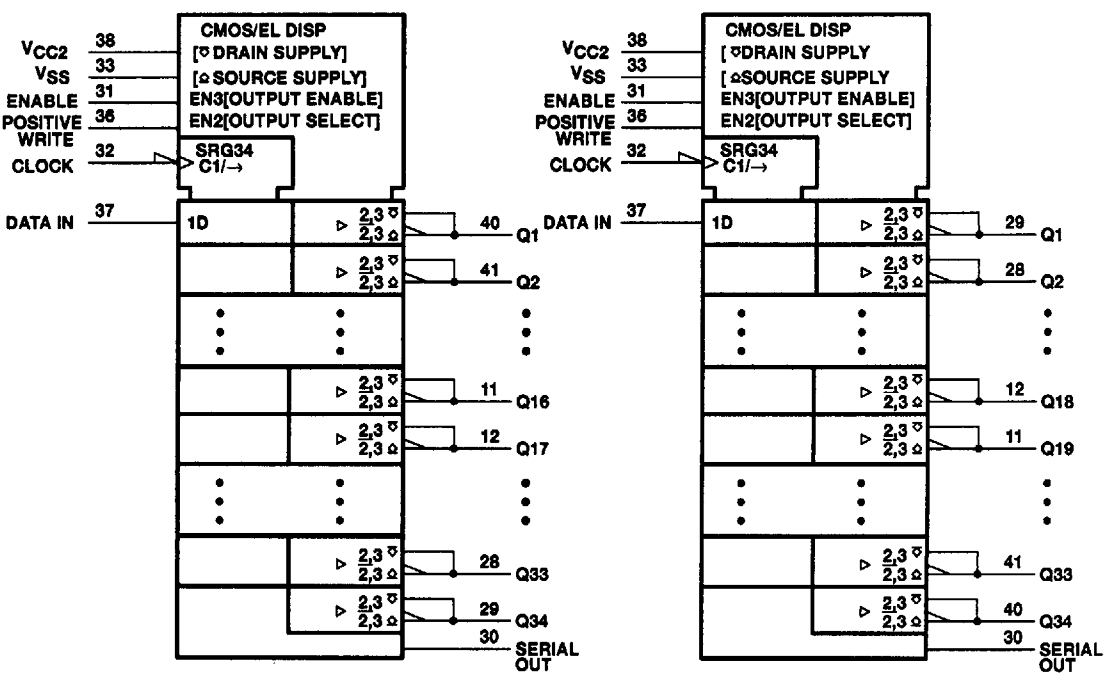
† Register R34 takes on the state of R33, R33 takes on the state of R32, . . . R2 takes on the state of R1, R1 takes on the state of the data input.

OUTPUT CONTROL FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS CONTENTS Rn FOR R1 THRU R34 (Determined Above)	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
Output Control	X	L	X	X	R34	High impedance
	X	H	H	H	R34	H
	X	H	L	H	R34	L
	X	X	X	L	R34	High impedance

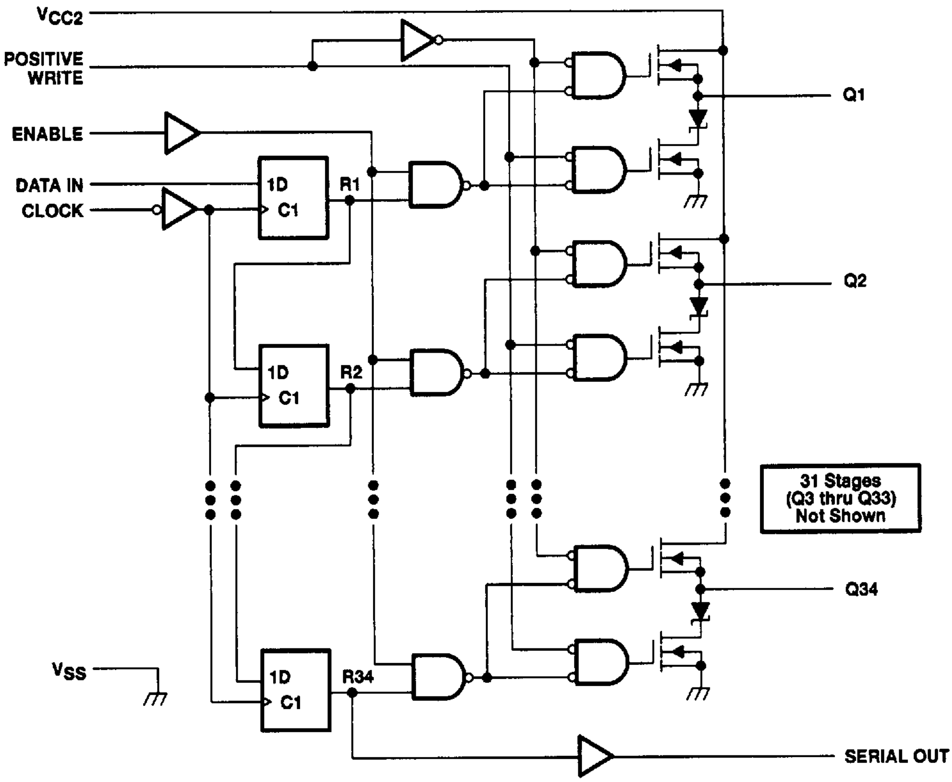
H = high, L = low, X = irrelevant, ↓ = high-to-low transition

logic symbols‡

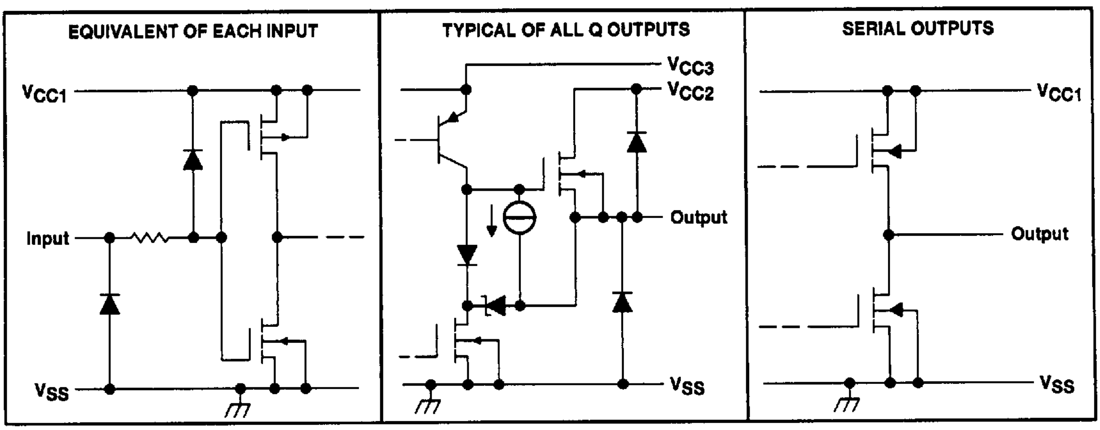


‡ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

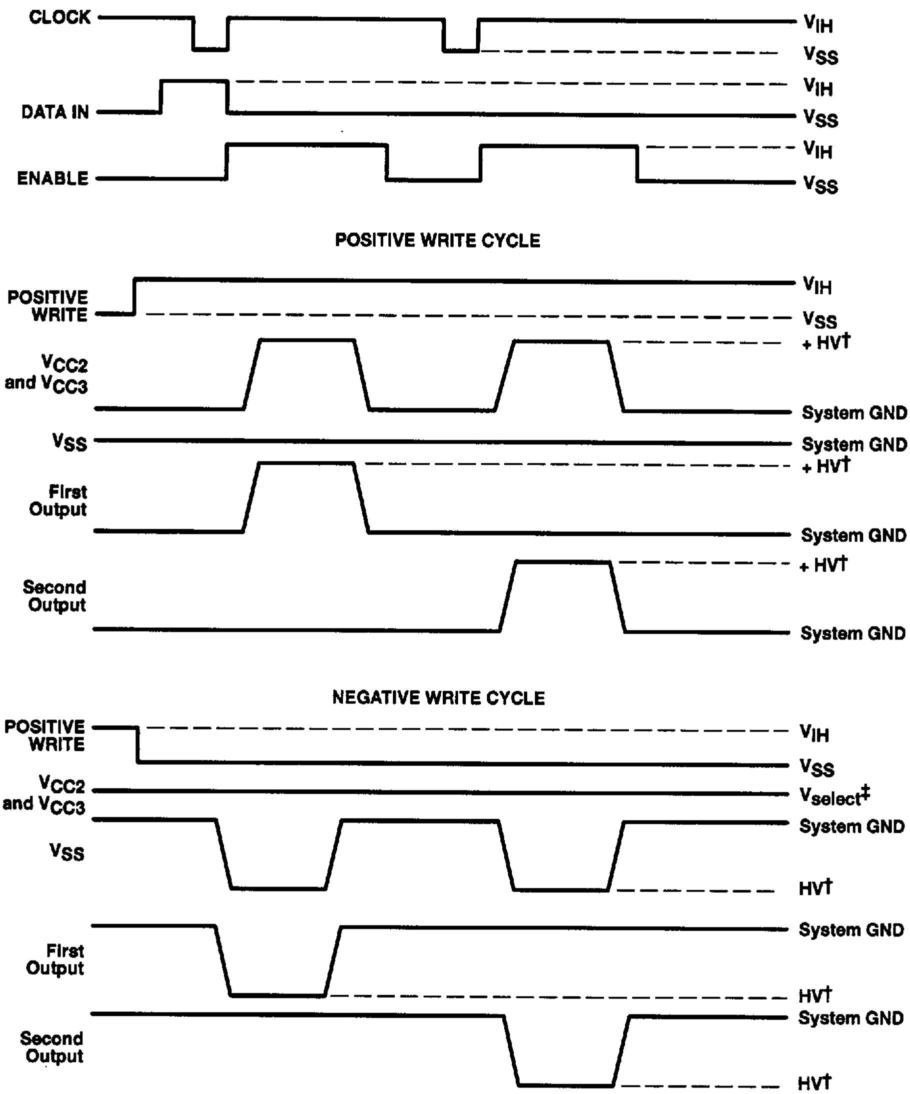
logic diagram (positive logic)



schematics of inputs and outputs



typical operating sequence



† HV = high voltage

‡ V_{SELECT} is a voltage level between V_{CC2} of the column driver and V_{SS}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) .... 15 V
Supply voltage, V_{CC2} .... 230 V
Supply voltage, V_{CC3} .... 230 V
Supply voltage, V_{SS} .... −230 V
Input voltage range, V_I .... −0.3 V to V_{CC1} + 0.3 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) .... 1825 mW
Operating free-air temperature range .... −55°C to 125°C
Storage temperature range .... −65°C to 150°C
Case temperature for 10 seconds .... 260°C

NOTES: 1. Voltage values are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, derate to 365 mW at 125°C at the rate of 14.6 mW/°C.

recommended operating conditions (see Figures 1 and 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10.8	12	13.2	V
Supply voltage, V_{CC2}	$V_{CC3}-15$		V_{CC3}	V
Supply voltage, V_{CC3}	0		225	V
Supply voltage, V_{SS}	0		−225	V
High-level input voltage, V_{IH}	$0.75V_{CC1}$		$V_{CC1}+0.3$	V
Low-level input voltage, V_{IL}	−0.3†		$0.25V_{CC1}$	V
High-level output current, I_{OH}			−90	mA
Low-level output current, I_{OL}			150	mA
Output clamp current, I_{OK}			±150	mA
Clock frequency, f_{clock}			1	MHz
Pulse duration, CLOCK high or low, $t_{w(CLK)}$	125			ns
Setup time, DATA IN high or low before CLOCK↓, t_{su1}	100			ns
Setup time, CLOCK low before V_{CC2}↑ or V_{SS}↓, t_{su2}	300‡			ns
Setup time, ENABLE high before V_{CC2}↑ or V_{SS}↓, t_{su3}	300‡			ns
Setup time, POSITIVE WRITE high or low before V_{CC2}↑ or V_{SS}↓, t_{su4}	300‡			ns
Hold time, DATA IN high or low after CLOCK↓, t_{h1}	100			ns
Hold time, CLOCK high after V_{CC2}↓ or V_{SS}↑, t_{h2}	300‡			ns
Hold time, ENABLE high after V_{CC2}↓ or V_{SS}↑, t_{h3}	0‡			ns
Hold time, POSITIVE WRITE after V_{CC2}↓ or V_{SS}↑, t_{h4}	0‡			ns
Hold time, ENABLE low between successive V_{CC2}↑, t_{h5}	12‡			µs
Hold time, ENABLE low between successive V_{SS}↓, t_{h6}	300‡			ns
Operating free-air temperature, T_A	−55		125	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
‡ These minimum recommendations are not tested during manufacturing. Performance is dependent on application voltage and temperature and must be validated by the user.

electrical characteristics over recommended operating ranges of V_{CC1} and free-air temperature range, V_{CC2} = 225 V, V_{CC3} = 225 V, V_{SS} = 0 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −70 mA, V_{CC1} = 12 V	V_{CC2}−40		V
			I_O = −90 mA, V_{CC1} = 12 V	V_{CC2}−45		
		SERIAL OUT	I_O = −100 µA, V_{CC1} = 12 V	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_O = 150 mA		30	V
		SERIAL OUT	I_O = 100 µA		1	
$I_{O(off)}$	Off-state Q output current		V_O = 225 V		150	µA
			V_O = 0		−150	
I_{IH}	High-level input current		V_{IH} = V_{CC1}		100	µA
I_{IL}	Low-level input current		V_{IL} = 0		−100	µA
I_{CC1}	Supply current from V_{CC1}		One Q output high		4	mA
			All Q outputs low or high impedance		2	
I_{CC3}	Supply current from V_{CC3}†		One Q output high, V_{CC1} = 12 V		10	mA
			All Q outputs low or high impedance, V_{CC1} = 12 V		200	µA

† I_{CC3} is measured with V_{CC2} and V_{CC3} shorted together.

switching characteristics over recommended operating range of V_{CC1}, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level SERIAL OUT from CLOCK	C_L = 50 pF to V_{SS}, See Figures 3 and 4		400	ns
t_{PHL}	Propagation delay time, high-to-low level SERIAL OUT from CLOCK			400	ns

PARAMETER MEASUREMENT INFORMATION

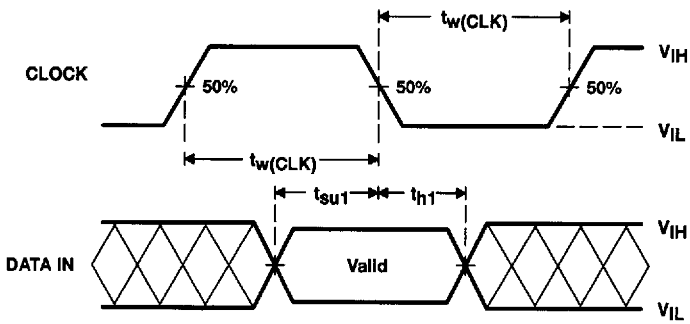
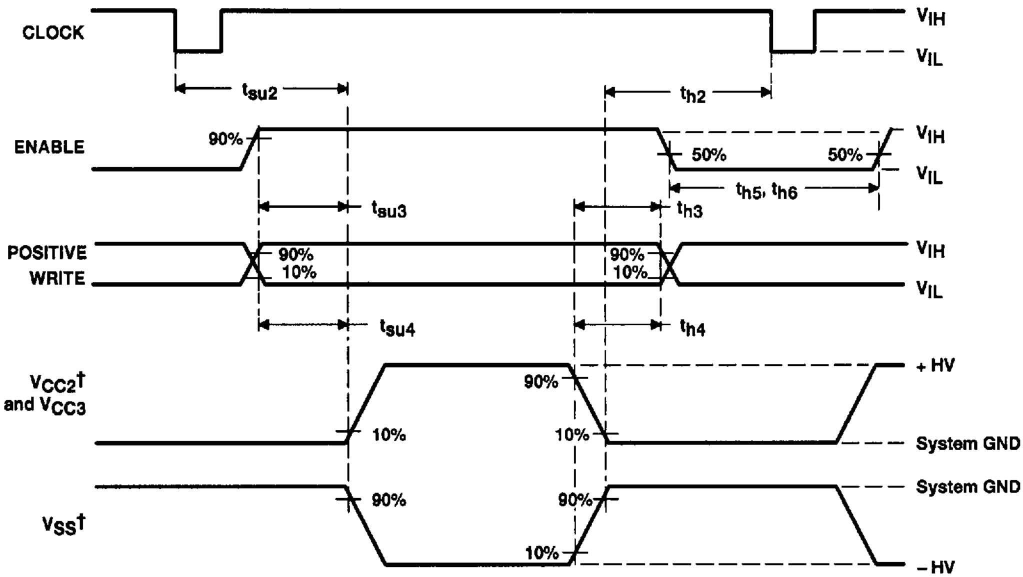


Figure 1. Input Timing Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



† Timing waveforms are with respect to V_{CC2} or V_{SS}, as appropriate.

Figure 2. Control Input Timing Voltage Waveforms

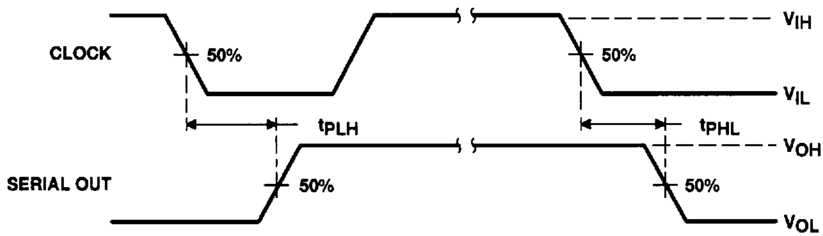
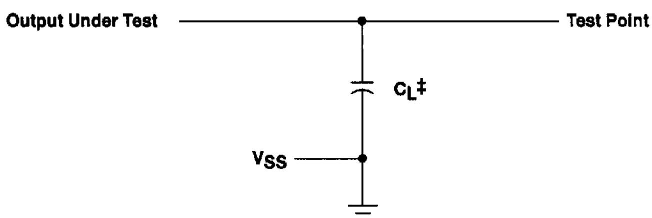


Figure 3. Voltage Waveforms for Propagation Delay Times, CLOCK to SERIAL OUT



‡ C_L includes probe and jig capacitance.

Figure 4. Load Circuit