80C152JA, ‘152JB, ‘152JC, ‘152JD

Universal Communication Controller 8-Bit Microcontroller

The 80C152, which is based on the MCS-51 CPU, is a highly integrated single-chip 8-bit microcontroller designed for cost-sensitive, high-speed, serial communications. It is well suited for implementing Integrated Services Digital Networks (ISDN), emerging Local Area Networks, and user defined serial backplane applications. In addition to the multi-protocol communication capability, the 80C152 offers traditional microcontroller features for peripheral I/O interface and control.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer’s datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. ‘Typical’ values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

8XC152JA/JB/JC/JD
UNIVERSAL COMMUNICATION CONTROLLER
8-BIT MICROCONTROLLER

- **8K Factory Mask Programmable ROM Available**

- **Superset of 80C51 Architecture**
- **Multi-Protocol Serial Communication I/O Port (2.048 Mbps/2.4 Mbps Max)**
  - **— SDLC/HDLC Only**
  - **— CSMA/CD and SDLC/HDLC**
  - **— User Definable Protocols**
- **Full Duplex/Half Duplex**
- **MCS®-51 Compatible UART**
- **16.5 MHz Maximum Clock Frequency**
- **Multiple Power Conservation Modes**
- **64KB Program Memory Addressing**
- **64KB Data Memory Addressing**
- **256 Bytes On-Chip RAM**
- **Dual On-Chip DMA Channels**
- **Hold/Hold Acknowledge**
- **Two General Purpose Timer/Counters**
- **5 or 7 I/O Ports**
- **56 Special Function Registers**
- **11 Interrupt Sources**
- **Available in 48 Pin Dual-In-Line Package and 68 Pin Surface Mount PLCC Package**
  (See Packaging Spec. Order #231369)

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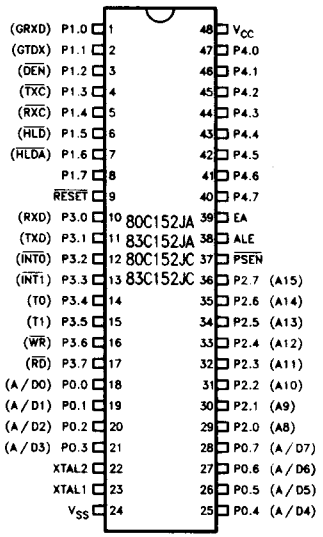
The 80C152, which is based on the MCS®-51 CPU, is a highly integrated single-chip 8-bit microcontroller designed for cost-sensitive, high-speed, serial communications. It is well suited for implementing Integrated Services Digital Networks (ISDN), emerging Local Area Networks, and user defined serial backplane applications. In addition to the multi-protocol communication capability, the 80C152 offers traditional microcontroller features for peripheral I/O interface and control.

Silicon implementations are much more cost effective than multi-wire cables found in board level parallel-to-serial and serial-to-parallel converters. The 83C152 contains, in silicon, all the features needed for the serial-to-parallel conversion. Other 83C152 benefits include: 1) better noise immunity through differential signaling or fiber optic connections, 2) data integrity utilizing the standard, designed in CRC checks, and 3) better modularity of hardware and software designs. All of these—cost, network parameter and real estate improvements—apply to 83C152 serial links between boards or systems and 83C152 serial links on a single board.

October 1989
Order Number: 270431-003



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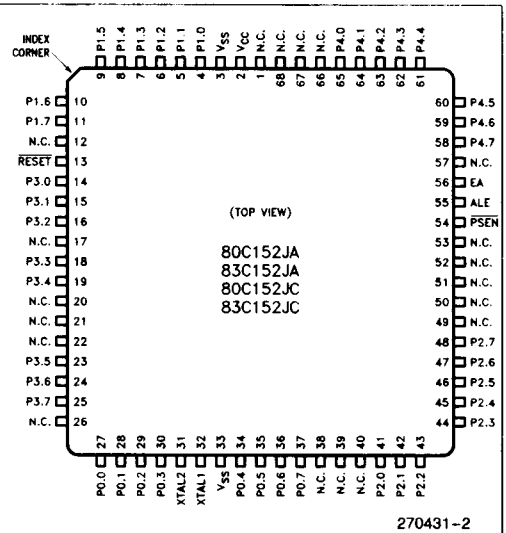

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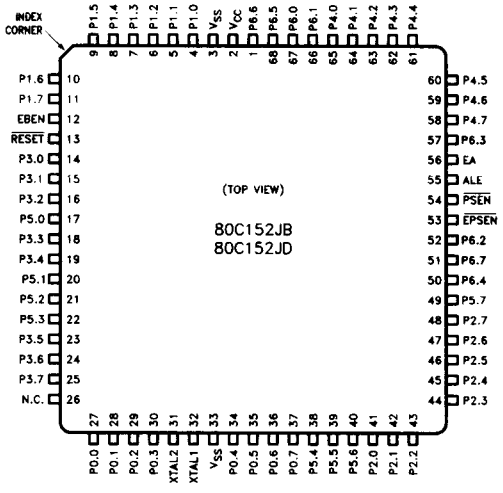

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Figure 1. Connection Diagrams

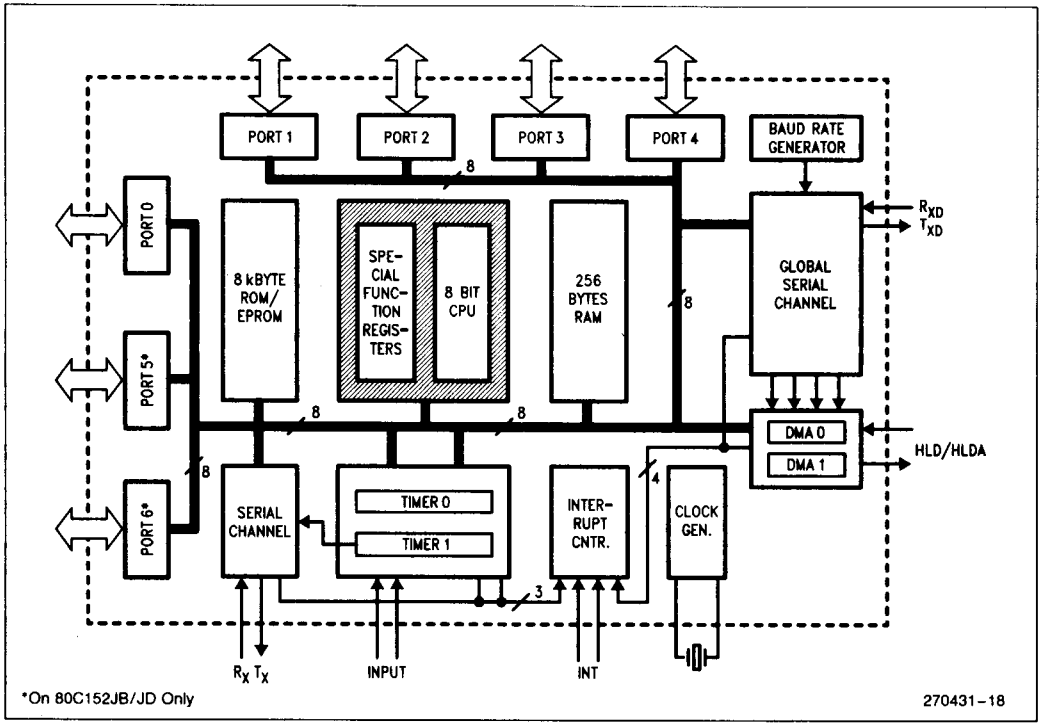


Figure 2. Block Diagram

80C152JB/JD General Description

The 80C152JB/JD is a ROMless extension of the 80C152 Universal Communication controller. The 80C152JB has the same five 8-bit I/O ports of the 80C152, plus an additional two 8-bit I/O ports, Port 5 and Port 6. The 80C152JB/JD also has two additional control pins, EBEN (**E**PROM **B**us **EN**able), and $\overline{\text{EPSEN}}$ (**E**PROM bus **P**rogram **S**tore **EN**able).

EBEN selects the functionality of Port 5 and Port 6. When EBEN is low, these ports are strictly I/O, similar to Port 4. The SFR location for Port 5 is 91H and Port 6 is 0A1H. This means Port 5 and Port 6 are not bit addressable. With EBEN low, all program memory fetches take place via Port 0 and Port 2. (The 80C152 is a ROMless only product). When EBEN is high, Port 5 and Port 6 form an address/data bus called the E-Bus (EPROM-Bus) for program memory operations.

$\overline{\text{EPSEN}}$ is used in conjunction with Port 5 and Port 6 program memory operations. $\overline{\text{EPSEN}}$ functions like $\overline{\text{PSEN}}$ during program memory operation, but supports Port 5 and Port 6. $\overline{\text{EPSEN}}$ is the read strobe to external program memory for Port 5 and Port 6. $\overline{\text{EPSEN}}$ is activated twice during each machine cycle unless an external data memory operation occurs on Port(s) 0 and Port 2. When external data memory is accessed the second activation of $\overline{\text{EPSEN}}$ is skipped, which is the same as when using $\overline{\text{PSEN}}$. Note that data memory fetches cannot be made through Ports 5 and 6.

When EBEN is high and EA is low, all program memory operations take place via Ports 5 and 6. The high byte of the address goes out on Port 6, and the low byte is output on Port 5. ALE is still used to latch the address on Port 5. Next, the op code is read on Port 5. The timing is the same as when using Ports 0 and 2 for external program memory operations.

Table 1. Program Memory Fetches

EBEN	$\overline{\text{EA}}$	Program Fetch via	$\overline{\text{PSEN}}$	$\overline{\text{EPSEN}}$	Comments
0	0	P0, P2	Active	Inactive	Addresses 0–0FFFFH
0	1	N/A	N/A	N/A	Invalid Combination
1	0	P5, P6	Inactive	Active	Addresses 0–0FFFFH
1	1	P5, P6 P0, P2	Inactive Active	Active Inactive	Addresses 0–1FFFH Addresses ≥ 2000H

Table 2. 8XC152 Product Differences

ROMless Version	CSMA/CD and HDLC/SDLC	HDLC/SDLC Only	ROM Version Available	PLCC and DIP	PLCC Only	5 I/O Ports	7 I/O Ports
80C152JA	*		*(83C152JA)	*		*	
80C152JB	*				*		*
80C152JC		*	*(83C152JC)	*		*	
80C152JD		*			*		*

NOTES:
* = options available
0 standard frequency range 3.5 MHz to 12 MHz
0 "−1" frequency range 3.5 MHz to 16.5 MHz

Pin #		Pin Description
DIP	PLCC(1)	
48	2	V_{CC}—Supply voltage.
24	3,33(2)	V_{SS}—Circuit ground.
18-21, 25-28	27-30, 34-37	**Port 0**—Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program memory if EBEN is pulled low. During accesses to external Data Memory, Port 0 always emits the low-order address byte and serves as the multiplexed data bus. In these applications it uses strong internal pullups when emitting 1s. Port 0 also outputs the code bytes during program verification. External pullups are required during program verification.
1-8	4-11	**Port 1**—Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. Port 1 also serves the functions of various special features of the 8XC152, as listed below:

Pin	Name	Alternate Function
P1.0	GRXD	GSC data input pin
P1.1	GTXD	GSC data output pin
P1.2	$\overline{DEN}$	GSC enable signal for an external driver
P1.3	$\overline{TXC}$	GSC input pin for external transmit clock
P1.4	$\overline{RXC}$	GSC input pin for external receive clock
P1.5	$\overline{HLD}$	DMA hold input/output
P1.6	$\overline{HLDA}$	DMA hold acknowledge input/output

29-36	41-48	**Port 2**—Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory if EBEN is pulled low. During accesses to external Data Memory that use 16-bit addresses (MOVX @ DPTR and DMA operations), Port 2 emits the high-order address byte. In these applications it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits during program verification.
10- 17	14-16, 18, 19, 23-25	**Port 3**—Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups. Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Pin	Name	Alternate Function
P3.0	RXD	Serial input line
P3.1	TXD	Serial output line
P3.2	$\overline{INT0}$	External Interrupt 0
P3.3	$\overline{INT1}$	External Interrupt 1
P3.4	T0	Timer 0 external input
P3.5	T1	Timer 1 external input
P3.6	$\overline{WR}$	External Data Memory Write strobe
P3.7	$\overline{RD}$	External Data Memory Read strobe

Pin Description (Continued)

Pin #		Pin Description
47-40	65-58	**Port 4**—Port 4 is an 8-bit bidirectional I/O port with internal pullups. Port 4 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 4 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. In addition, Port 4 also receives the low-order address bytes during program verification.
9	13	**$\overline{RST}$**—Reset input. A logic low on this pin for three machine cycles while the oscillator is running resets the device. An internal pullup resistor permits a power-on reset to be generated using only an external capacitor to V_{SS}. Although the GSC recognizes the reset after three machine cycles, data may continue to be transmitted for up to 4 machine cycles after Reset is first applied.
38	55	**ALE**—Address Latch Enable output signal for latching the low byte of the address during accesses to external memory. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory. While in Reset, ALE remains at a constant high level.
37	54	**$\overline{PSEN}$**—Program Store Enable is the Read strobe to External Program Memory. When the 8XC152 is executing from external program memory, $\overline{PSEN}$ is active (low). When the device is executing code from External Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to External Data Memory. While in Reset, $\overline{PSEN}$ remains at a constant high level.
39	56	**$\overline{EA}$**—External Access enable. $\overline{EA}$ must be externally pulled low in order to enable the 8XC152 to fetch code from External Program Memory locations 0000H to 0FFFH. $\overline{EA}$ must be connected to V_{CC} for internal program execution.
23	32	**XTAL1**—Input to the inverting oscillator amplifier and input to the internal clock generating circuits.
22	31	**XTAL2**—Output from the inverting oscillator amplifier.
N/A	17, 20 21, 22 38, 39 40, 49	**Port 5**—Port 5 is an 8-bit bidirectional I/O port with internal pullups. Port 5 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 5 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. Port 5 is also the multiplexed low-order address and data bus during accesses to external program memory if EBEN is pulled high. In this application it uses strong pullups when emitting 1s.
N/A	67, 66 52, 57 50, 68 1, 51	**Port 6**—Port 6 is an 8-bit bidirectional I/O port with internal pullups. Port 6 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 6 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. Port 6 emits the high-order address byte during fetches from external Program Memory if EBEN is pulled high. In this application it uses strong pullups when emitting 1s.
N/A	12	**EBEN**—E-Bus Enable input that designates whether program memory fetches take place via Ports 0 and 2 or Ports 5 and 6. Table 1 shows how the ports are used in conjunction with EBEN.
N/A	53	**$\overline{EPSEN}$**—E-bus Program Store Enable is the Read strobe to external program memory when EBEN is high. Table 2 shows when $\overline{EPSEN}$ is used relative to $\overline{PSEN}$ depending on the status of EBEN and $\overline{EA}$.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3.

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

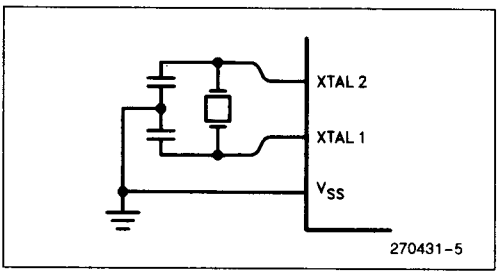


Figure 3. Using the On-Chip Oscillator

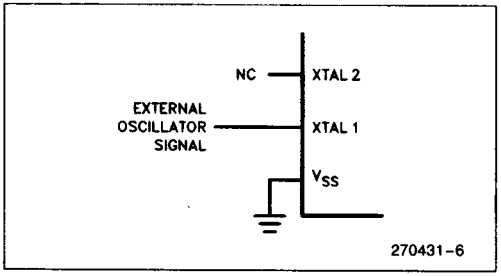


Figure 4. External Clock Drive

IDLE MODE

In Idle Mode, the CPU puts itself to sleep while most of the on-chip peripherals remain active. The major peripherals that do not remain active during Idle, are the DMA channels. The Idle Mode is invoked by software. The content of the on-chip RAM and all the Special Function Registers remain unchanged during this mode. The Idle Mode can be terminated by any enabled interrupt or by a hardware reset.

POWER DOWN MODE

In Power Down Mode, the oscillator is stopped and all on-chip functions cease except that the on-chip RAM contents are maintained. The mode Power Down is invoked by software. The Power Down Mode can be terminated only by a hardware reset.

Table 3. Status of the External Pins During Idle and Power Down Modes

80C152JA/83C152JA/80C152JC/83C152JC

Mode	Program Memory	ALE	$\overline{PSEN}$	Port 0	Port 1	Port 2	Port 3	Port 4
Idle	Internal	1	1	Data	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data	Data
Power Down	Internal	0	0	Data	Data	Data	Data	Data
Power Down	External	0	0†	Float	Data	Data	Data	Data

80C152JB/80C152JD

Mode	Instruction Bus	ALE	$\overline{PSEN}$	$\overline{EPSEN}$	Port 0	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6
Idle	P0, P2	1	1	1	Float	Data	Address	Data	Data	0FFH	0FFH
Idle	P5, P6	1	1	1	Data	Data	Data	Data	Data	0FFH	Address
Power Down	P0, P2	0	0	1	Float	Data	Data	Data	Data	0FFH	0FFH
Power Down	P5, P6	0	1†	0	Data	Data	Data	Data	Data	0FFH	0FFH

NOTE:
For more detailed information on the reduced power modes refer to the Embedded Controller Handbook, and Application Note AP-252, "Designing with the 80C51BH."
†Note difference of logic level of $\overline{PSEN}$ during Power Down for ROM JA/JC and ROM emulation mode for JC/JD.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any pin to V_{SS} . . −0.5V to (V_{CC} + 0.5V)
Voltage on V_{CC} to VSS . . . . . −0.5V to +6.5V
Power Dissipation . . . . . 1.0W(9)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V)

Symbol	Parameter	Min	Typ (Note 3)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (All Except $\overline{EA}$, EBEN)	−0.5		$0.2V_{CC}-0.1$	V	
V_{IL1}	Input Low Voltage ($\overline{EA}$, EBEN)	−0.5		$0.2V_{CC}-0.3$	V	
V_{IH}	Input High Voltage (Except XTAL1, $\overline{RST}$)	$0.2V_{CC}+0.9$		$V_{CC}+0.5$	V	
V_{IH1}	Input High Voltage (XTAL1, $\overline{RST}$)	$0.7V_{CC}$		$V_{CC}+0.5$	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3, 4, 5, 6)			0.45	V	I_{OL} = 1.6 mA (Note 4)
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$, $\overline{EPSEN}$)			0.45	V	I_{OL} = 3.2 mA (Note 4)
V_{OH}	Output High Voltage (Ports 1, 2, 3, 4, 5, 6 COMM9 ALE, $\overline{PSEN}$, $\overline{EPSEN}$)	2.4			V	I_{OH} = −60 μA V_{CC} = 5V ±10%
		$0.9V_{CC}$			V	I_{OH} = −10 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4			V	I_{OH} = −400 μA V_{CC} = 5V ±10%
		$0.9V_{CC}$			V	I_{OH} = −40 μA (Note 5)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3, 4, 5, 6)			−50	μA	V_{IN} = 0.45V
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3, 4, 5, 6)			−650	μA	V_{IN} = 2V
I_{LI}	Input Leakage (Port 0, $\overline{EA}$)			±10	μA	$0.45 < V_{IN} < V_{CC}$
RRST	Reset Pullup Resistor	40			kΩ	
I_{IH}	Logical 1 Input Current (EBEN)			+60	μA	
I_{CC}	Power Supply Current : Active (16.5 MHz)		31	41.1	mA	(Note 6)
	Idle (16.5 MHz)		8	15.4	mA	(Note 6)
	Power Down Mode		10		μA	V_{CC} = 2.0V to 5.5V

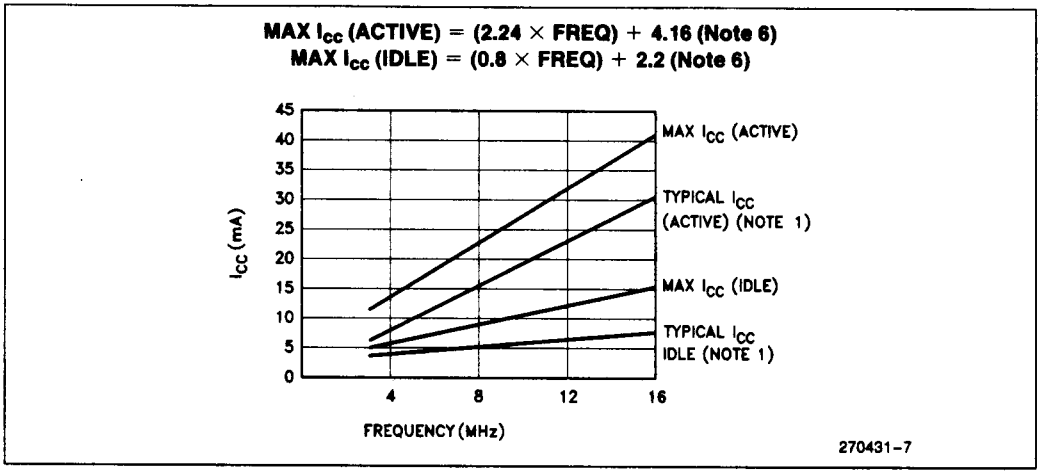


Figure 5. I_{CC} vs Frequency

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address.
C: Clock
D: Input data.
H: Logic level HIGH.
I: Instruction (program memory contents).
L: Logic level LOW, or ALE.
P: $\overline{PSEN}$.
Q: Output data.
R: $\overline{READ}$ signal.
T: Time.
V: Valid.
W: $\overline{WRITE}$ signal.
X: No longer a valid logic level.
Z: Float.

For example,

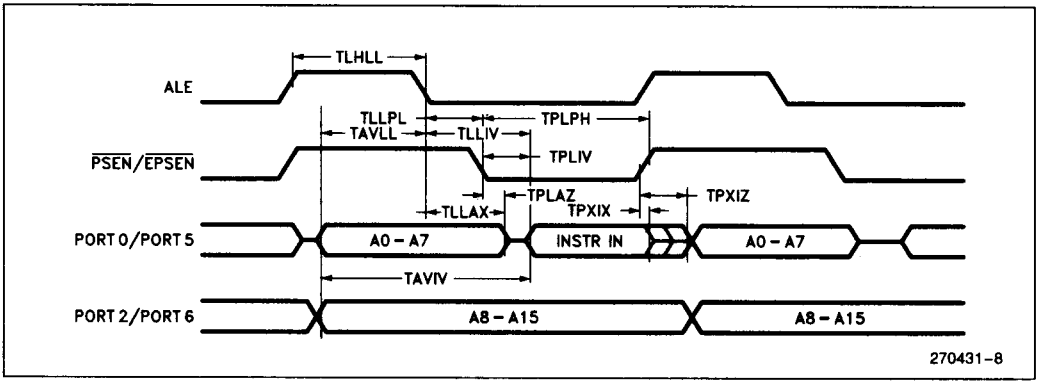
TAVLL = Time for Address Valid to ALE Low.
TLLPL = Time for ALE Low to $\overline{PSEN}$ Low.

A.C. CHARACTERISTICS (T_A = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V; Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

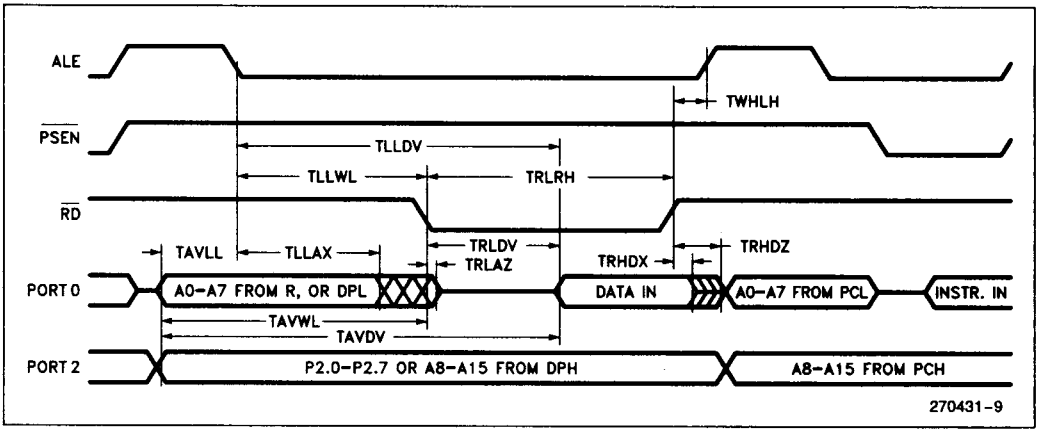
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS (Note 7, 10)

Symbol	Parameter	16.5 MHz		Variable Oscillator		Unit
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 80C152JA/JC 83C152JA/JC 80C152JB/JD			3.5	12	MHz
	80C152JA/JC-1 83C152JA/JC-1 80C152JB/JD-1			3.5	16.5	MHz
TLHLL	ALE Pulse Width	81		2TCLCL-40		ns
TAVLL	Address Valid to ALE Low	5		TCLCL-55		ns
TLLAX	Address Hold After ALE Low	25		TCLCL-35		ns
TLLIV	ALE Low to Valid Instruction In		142		4TCLCL-100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	20		TCLCL-40		ns
TPLPH	$\overline{PSEN}$ Pulse Width	137		3TCLCL-45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		77		3TCLCL-105	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		35		TCLCL-25	ns
TAVIV	Address to Valid Instruction In		198		5TCLCL-105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	263		6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	263		6TCLCL-100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		138		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		51		2TCLCL-70	ns
TLLDV	ALE Low to Valid Data In		335		8TCLCL-150	ns
TAVDV	Address to Valid Data In		380		9TCLCL-165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	132	232	3TCLCL-50	3TCLCL + 50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	112		4TCLCL-130		ns
TQVWX(8)	Data Valid to $\overline{WR}$ Transition	196		6TCLCL-167		ns
TWHQX	Data Hold After $\overline{WR}$	10		TCLCL-50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	20	100	TCLCL-40	TCLCL + 40	ns

EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



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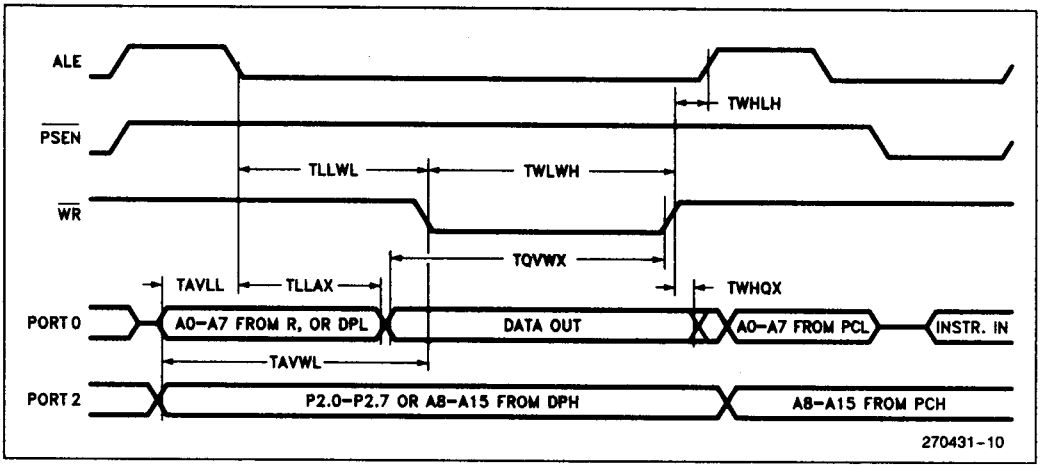
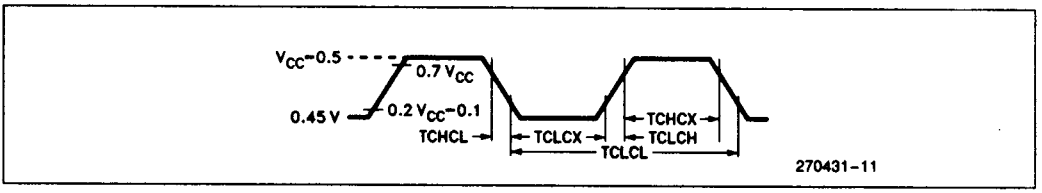
EXTERNAL DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	16.5	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

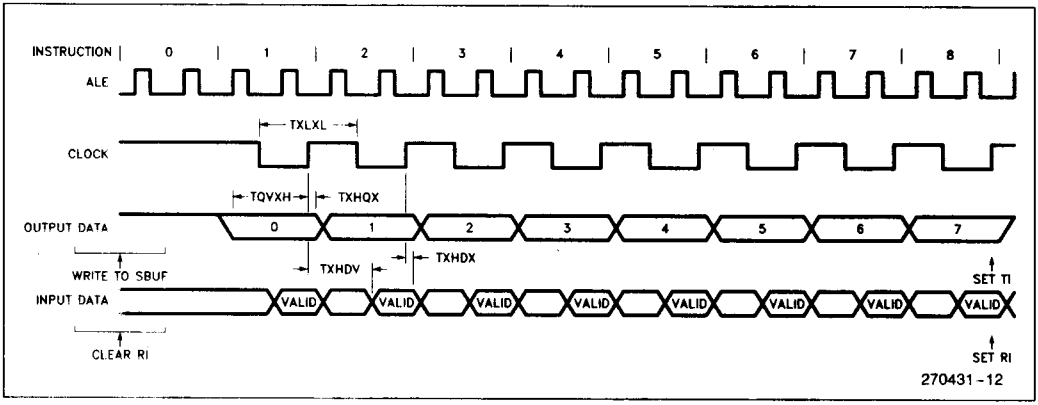
EXTERNAL CLOCK DRIVE WAVEFORM



LOCAL SERIAL CHANNEL TIMING—SHIFT REGISTER MODE

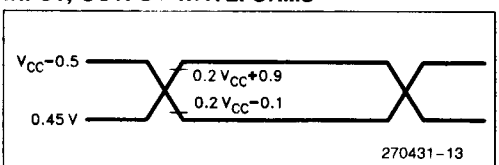
Symbol	Parameter	16.5 MHz		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	727		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	473		10TCLCL-133		ns
TXHQX	Output Data Hold After Clock Rising Edge	4		2TCLCL-117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		473		10TCLCL-133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS



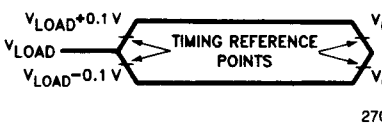
A.C. TESTING:

INPUT, OUTPUT WAVEFORMS



AC Inputs During Testing are Driven at $V_{CC}-0.5$ for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at V_{IH} Min for a Logic "1" and V_{IL} Max for a Logic "0".

FLOAT WAVEFORM

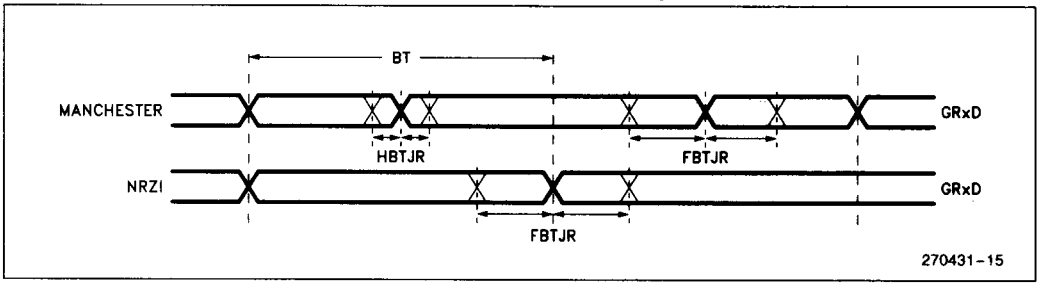


For Timing Purposes a Port Pin is no Longer Floating when a 100 mV change from Load Voltage Occurs, and Begins to Float when a 100 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} \geq \pm 20$ mA.

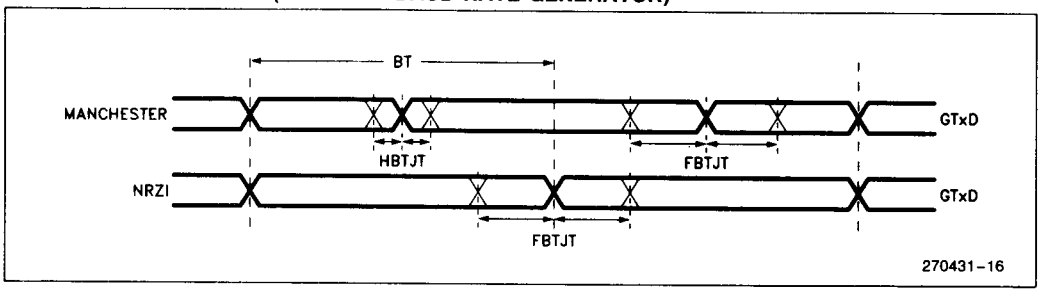
GLOBAL SERIAL PORT TIMINGS—Internal Baud Rate Generator

Symbol	Parameter	16.5 MHz (BAUD = 0)		Variable Oscillator		Unit
		Min	Max	Min	Max	
HBTJR	Allowable jitter on the Receiver for ½ bit time (Manchester encoding only)		0.0375		(0.125 × (BAUD + 1) × 8TCLCL) − 25 ns	µs
FBTJR	Allowable jitter on the Receiver for one full bit time (NRZI and Manchester)		0.10		(0.25 × (BAUD + 1) × 8TCLCL) − 25 ns	µs
HBTJT	Jitter of data from Transmitter for ½ bit time (Manchester encoding only)		±10		±10	ns
FBTJT	Jitter of data from Transmitter for one full bit time (NRZI and Manchester)		±10		±10	ns
DRTR	Data rise time for Receiver(11)		20		20	ns
DFTR	Data fall time for Receiver(12)		20		20	ns

GSC RECEIVER TIMINGS (INTERNAL BAUD RATE GENERATOR)



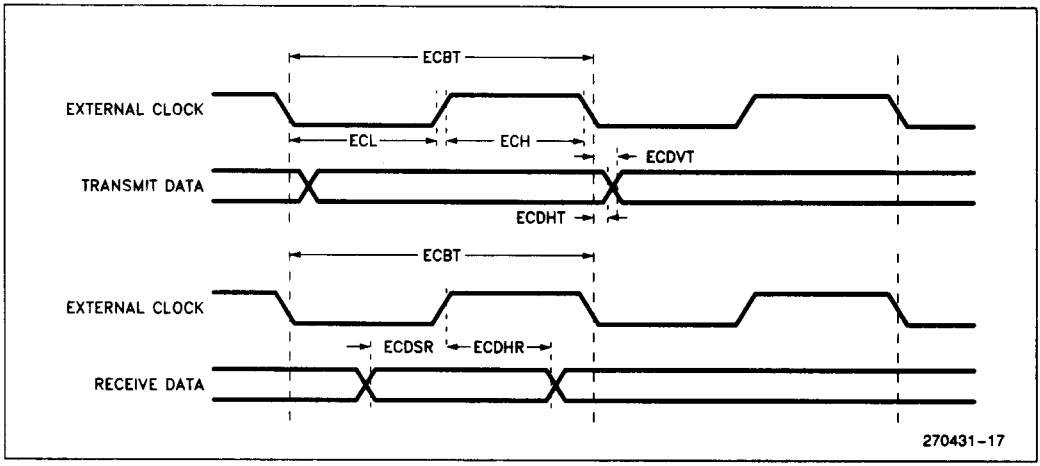
GSC TRANSMIT TIMINGS (INTERNAL BAUD RATE GENERATOR)



GLOBAL SERIAL PORT TIMINGS—External Clock

Symbol	Parameter	16.5 MHz		Variable Oscillator		Unit
		Min	Max	Min	Max	
1/ECBT	GSC Frequency with an External Clock		2.4	0.009	$F_{OSC} \times 0.145$	MHz
ECH	External Clock High	170		2TCLCL + 45 ns		ns
ECL(13)	External Clock Low	170		2TCLCL + 45 ns		ns
ECRT	External Clock Rise Time(11)		20		20	ns
ECFT	External Clock Fall Time(12)		20		20	ns
ECDVT	External Clock to Data Valid Out - Transmit (to External Clock Negative Edge)		150		150	ns
ECDHT	External Clock Data Hold - Transmit (to External Clock Negative Edge)	0		0		ns
ECDSR	External Clock Data Set-up - Receiver (to External Clock Positive Edge)	45		45		ns
ECDHR	External Clock to Data Hold - Receiver (to External Clock Positive Edge)	50		50		ns

GSC TIMINGS (EXTERNAL CLOCK)



NOTES:

1. N.C. pins on PLCC package may be connected to internal die and should not be used in customer applications.
2. It is recommended that both Pin 3 and Pin 33 be grounded for PLCC devices.
3. "Typicals" are based on samples taken from early manufacturing lots and are not guaranteed. The measurements were made with V_{CC} = 5V at room temperature.
4. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0 8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
5. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
6. I_{CC} is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; Port 0 pins connected to V_{CC}. "Operating" current is measured with $\overline{EA}$ connected to V_{CC} and $\overline{RST}$ connected to V_{SS}. "Idle" current is measured with $\overline{EA}$ connected to V_{SS}, $\overline{RST}$ connected to V_{CC} and GSC inactive.
7. The specifications relating to external data memory characteristics are also applicable to DMA operations.
8. TQVWX should not be confused with TQVWX as specified for 80C51BH. On 80C152, TQVWX is measured from data valid to rising edge of $\overline{WR}$. On 80C51BH, TQVWX is measured from data valid to falling edge of $\overline{WR}$. See timing diagrams.
9. This value is based on the maximum allowable die temperature and the thermal resistance of the package.
10. All specifications relating to external program memory characteristics are applicable to:
    $\overline{EPSEN}$ for $\overline{PSEN}$
    Port 5 for Port 0
    Port 6 for Port 2
    when EBEN is at a Logical 1 on the 80C152JB/JD.
11. Same as TCLCH, use External Clock Drive Waveform.
12. Same as TCHCL, use External Clock Drive Waveform.
13. When using the same external clock to drive both the receiver and transmitter, the minimum ECL spec effectively becomes 195 ns at all frequencies (assuming 0 ns propagation delay) because ECDVT (150 ns) plus ECDSR (45 ns) requirements must also be met (150 + 45 = 195 ns). The 195 ns requirement would also increase to include the maximum propagation delay between receivers and transmitters.

DESIGN NOTES

Within the 8XC152 there exists a race condition that may set both the RDN and AE bits at the end of a valid reception. This will not cause a problem in the application as long as the following steps are followed:

—Never give the receive error interrupt a higher priority than the valid reception interrupt

—Do not leave the valid reception interrupt service routine when AE is set by using a RETI instruction until AE is cleared. To clear AE set the GREN bit, this enables the receiver. If the user desires that the receiver remain disabled, clear GREN after setting it before leaving the interrupt service routine.

—If the AE bit is checked by user software in response to a valid reception interrupt, the status of AE should be considered invalid.

The race condition is dependent upon both the temperature that the device is currently operating at and the processing the device received during the wafer fabrication.

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

DATA SHEET REVISION SUMMARY

The following represent the key differences between the "-003" and the "-002" version of the 80C152/83C152 data sheet. Please review this summary carefully.

1. Removed minimum GSC frequency spec when used with an external clock.
2. Change figure "External Program Memory Read Cycle" to show Port 0/Port 5 address floating after PSEN goes low.
3. Added design note on terminating idle with reset.
4. Added status of PSEN during Power Down mode to Table 3.
5. Moved all notes to back of data sheet.
6. Changed microcomputer to microcontroller.
7. Added External Oscillator start-up capacitance note.

The following represent the key differences between the "-002" and the "-001" version of the 80C152/83C152 data sheet. Please review this summary carefully.

1. Status of data sheet changed from "ADVANCED" to "PRELIMINARY".
2. 80C152JC, 83C152JC, and 80C152JD were added.
3. Added AE/RDN design note.
4. This revision summary was added.
5. Note #13 was added (Effective ECL spec at higher clock rates).
6. Table #2 changed to Table #3 (Status of pins during Idle/Power Down).
7. Current Table #2 was added (JA vs. JB vs. JC vs. JD matrix).
8. Transmit jitter spec changed from ±35 ns and ±70 ns to ±10 ns.