

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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SWITCHING  
P-CHANNEL POWER MOS FET  
INDUSTRIAL USE

DESCRIPTION

The 2SJ330 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance  
 $R_{DS(on)} = 40 \text{ m}\Omega \text{ TYP. (} V_{GS} = -10 \text{ V, } I_D = -10 \text{ A)}$   
 $R_{DS(on)} = 70 \text{ m}\Omega \text{ TYP. (} V_{GS} = -4 \text{ V, } I_D = -8 \text{ A)}$
- Low  $C_{iss}$        $C_{iss} = 2\,570 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes

QUALITY GRADE

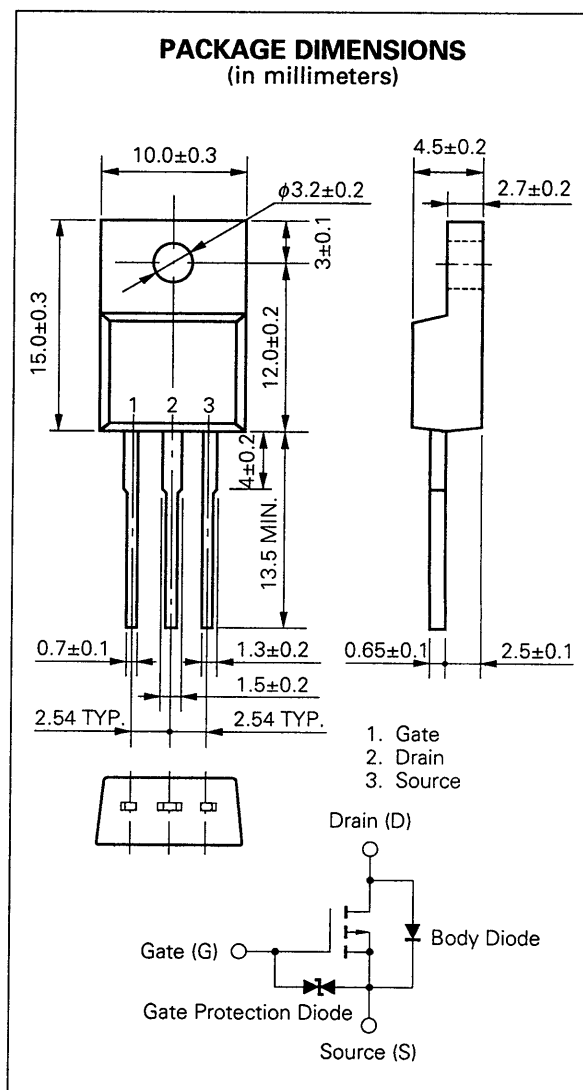
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ( $T_a = 25 \text{ }^\circ\text{C}$ )

Drain to Source Voltage	$V_{DSS}$	-60	V
Gate to Source Voltage	$V_{GSS(AC)}$	$\mp 20$	V
Gate to Source Voltage	$V_{GSS(DC)}$	-20, +10	V
Drain Current (DC)	$I_{D(DC)}$	$\mp 20$	A
Drain Current (pulse)	$I_{D(pulse)^*}$	$\mp 80$	A
Total Power Dissipation ( $T_c = 25 \text{ }^\circ\text{C}$ )	$PT_1$	35	W
Total Power Dissipation ( $T_a = 25 \text{ }^\circ\text{C}$ )	$PT_2$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C MAX.}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

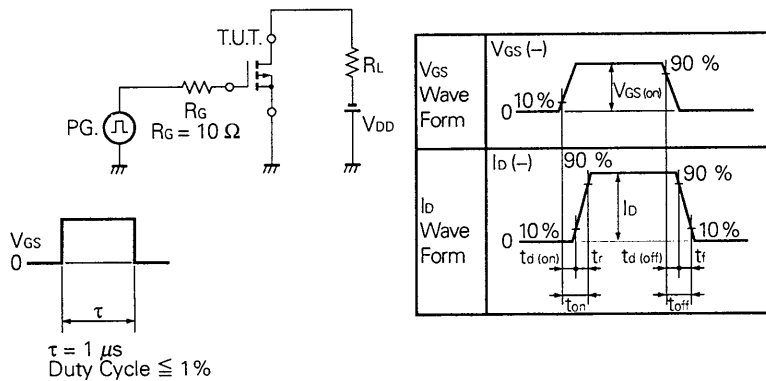
\*  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1 \%$



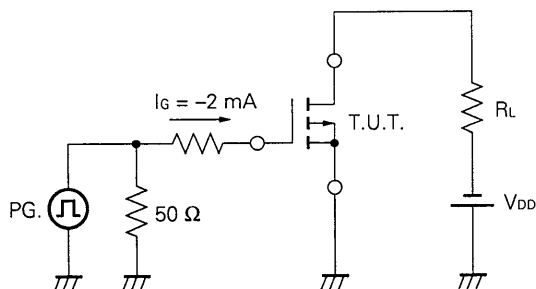
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.04	0.05	Ω	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -10 A
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.07	0.09	Ω	V <sub>GS</sub> = -4 V, I <sub>D</sub> = -8 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	-1.0	-1.6	-2.0	V	V <sub>DS</sub> = -10 V, I <sub>b</sub> = -1 mA
Forward Transfer Admittance	y <sub>fs</sub>	10			S	V <sub>DS</sub> = -10 V, I <sub>b</sub> = -10 A
Drain Leakage Current	I <sub>DSS</sub>			-10	μA	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		2 570		pF	V <sub>DS</sub> = -10 V V <sub>GS</sub> = 0 f = 1 MHz
Output Capacitance	C <sub>oss</sub>		1 460		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		640		pF	
Turn-On Delay Time	t <sub>d(on)</sub>		50		ns	V <sub>GS(on)</sub> = -10 V V <sub>DD</sub> = -30 V I <sub>D</sub> = -10 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 3.0 Ω
Rise Time	t <sub>r</sub>		200		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		340		ns	
Fall Time	t <sub>f</sub>		230		ns	
Total Gate Charge	Q <sub>G</sub>		90		nC	V <sub>GS</sub> = -10 V I <sub>b</sub> = -20 A V <sub>DD</sub> = -48 V
Gate to Source Charge	Q <sub>GS</sub>		7		nC	
Gate to Drain Charge	Q <sub>GD</sub>		36		nC	
Diode Forward Voltage	V <sub>SD</sub>		0.9		V	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		100		ns	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		490		nC	di/dt = 50 A/μs

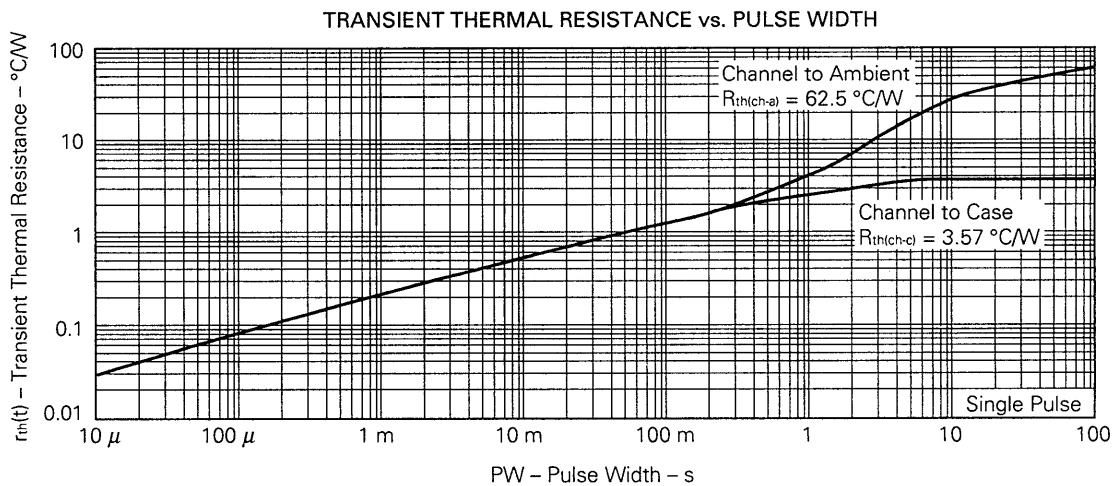
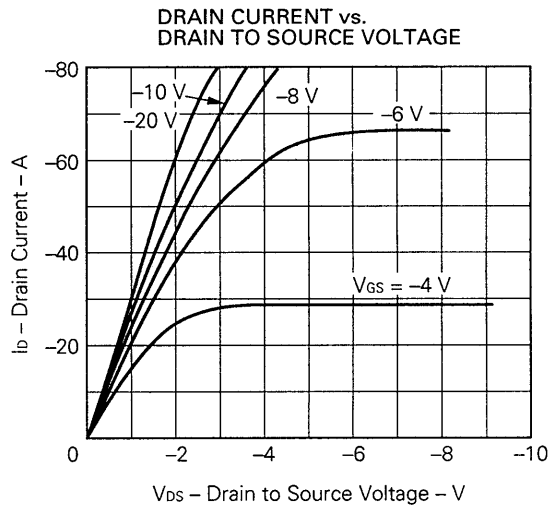
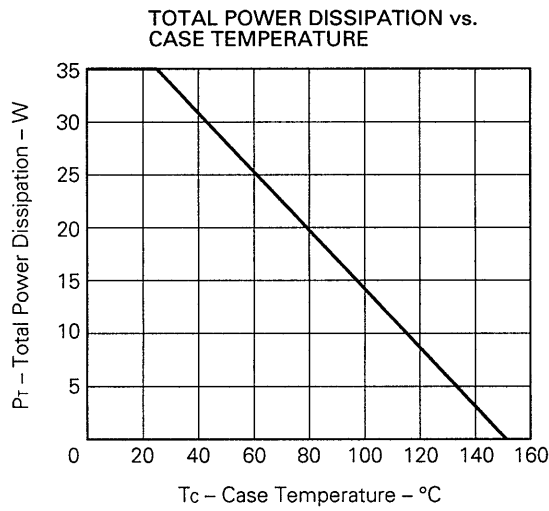
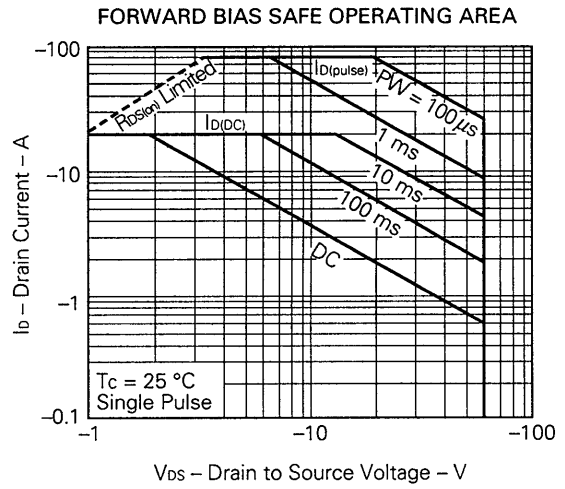
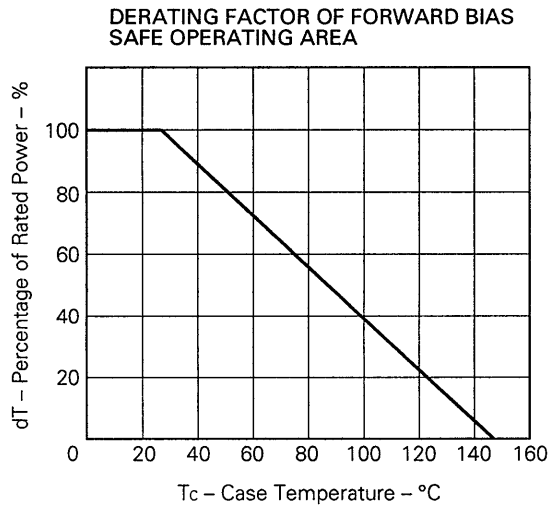
**Test Circuit 1: Switching Time**

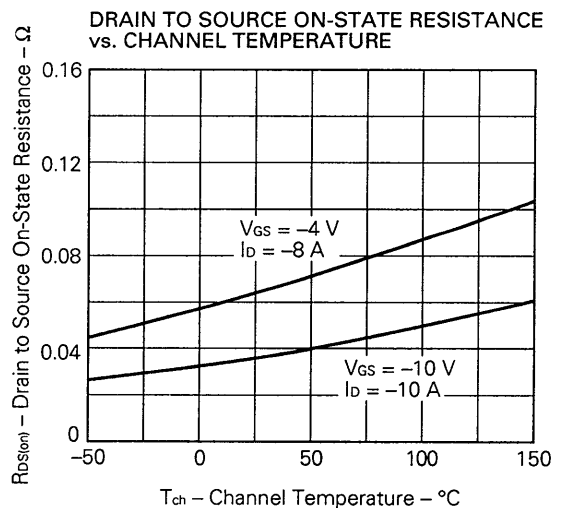
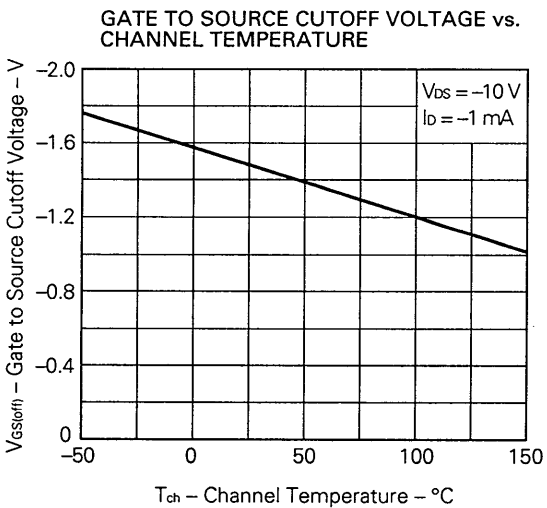
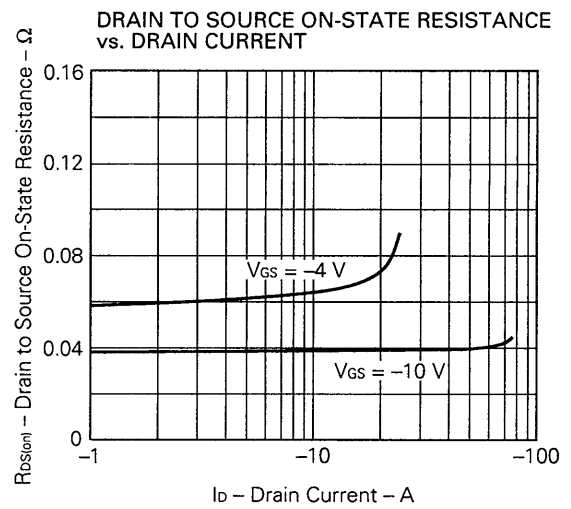
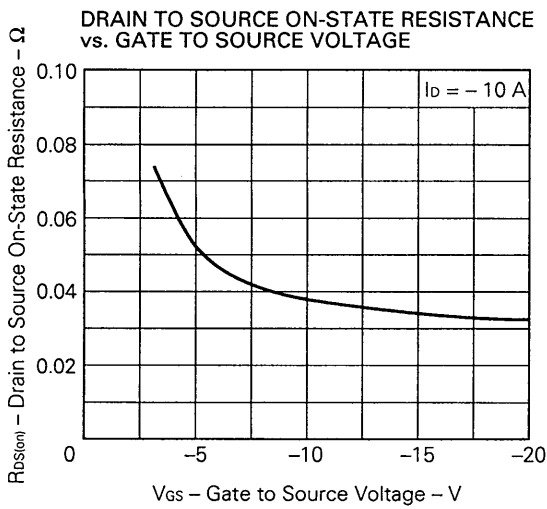
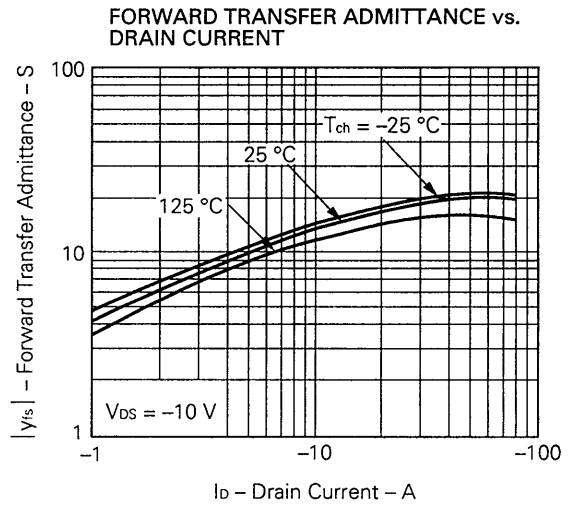
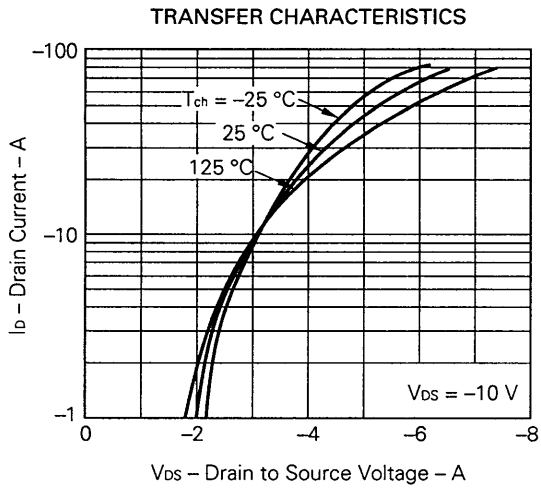


**Test Circuit 2: Gate Charge**

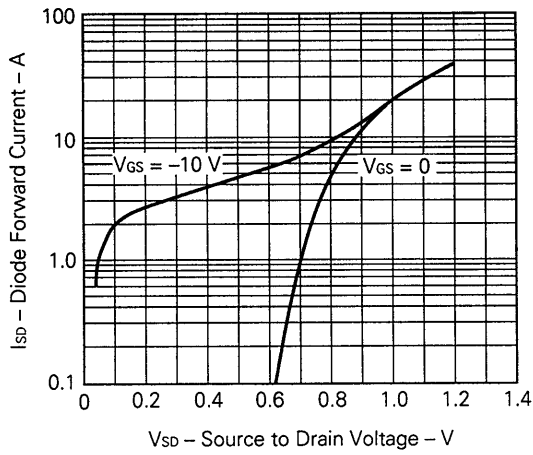


TYPICAL CHARACTERISTICS ( $T_a = 25\text{ }^\circ\text{C}$ )

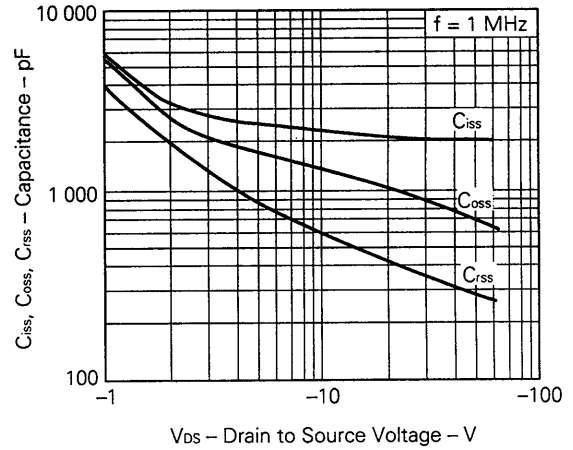




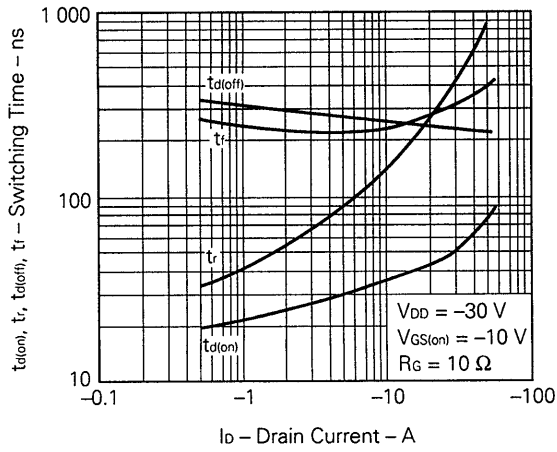
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



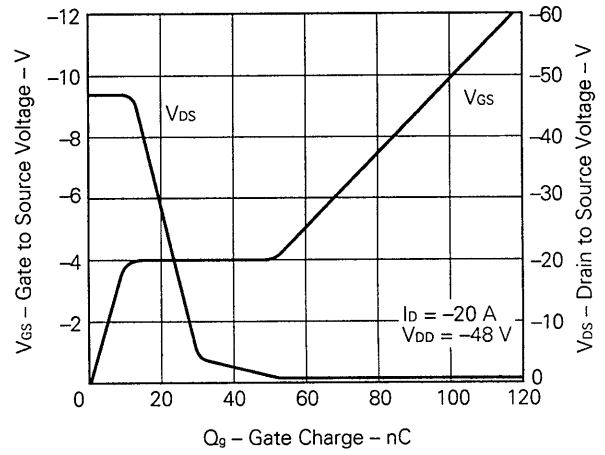
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



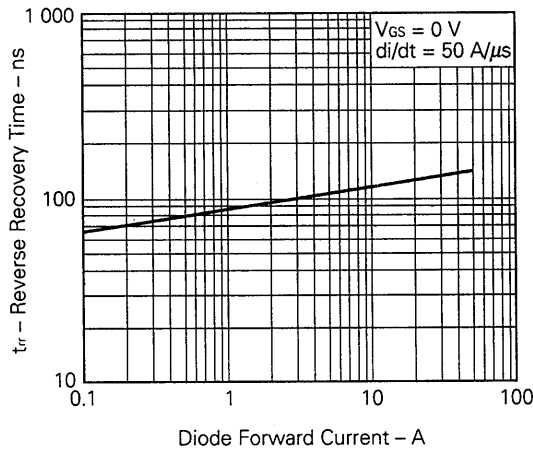
SWITCHING CHARACTERISTICS



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT



**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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