Am29F016D

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **21444** Revision **E** Amendment **3** Issue Date **June 4, 2004**

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Am29F016D

16 Megabit (2 M x 8-Bit)
CMOS 5.0 Volt-only, Uniform Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10%, single power supply operation**
  - — Minimizes system level power requirements
- **Manufactured on 0.23 µm process technology**
  - — Compatible with 0.5 µm Am29F016 and 0.32 µm Am29F016B devices
- **High performance**
  - — Access times as fast as 70 ns
- **Low power consumption**
  - — 25 mA typical active read current
  - — 30 mA typical program/erase current
  - — 1 µA typical standby current (standard access time to active mode)
- **Flexible sector architecture**
  - — 32 uniform sectors of 64 Kbytes each
  - — Any combination of sectors can be erased
  - — Supports full chip erase
  - — Group sector protection:

    A hardware method of locking sector groups to prevent any program or erase operations within that sector group

    Temporary Sector Group Unprotect allows code changes in previously locked sectors
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies bytes at specified addresses
- **Unlock Bypass Program Command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Minimum 1,000,000 program/erase cycles per sector guaranteed**
- **20-year data retention at 125°C**
  - — Reliable operation for the life of the system
- **Package options**
  - — 48-pin and 40-pin TSOP
  - — 44-pin SO
  - — Known Good Die (KGD) (see publication number 21551)
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply Flash standard
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase cycle completion
- **Ready/Busy# output (RY/BY#)**
  - — Provides a hardware method for detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - — Suspends a sector erase operation to read data from, or program data to, a non-erasing sector, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Resets internal state machine to the read mode

Publication# **21444** Rev: **E** Amendment/**+3**
Issue Date: **June 4, 2004**

GENERAL DESCRIPTION

The Am29F016D is a 16 Mbit, 5.0 volt-only Flash memory organized as 2,097,152 bytes. The 8 bits of data appear on DQ0–DQ7. The Am29F016D is offered in 48-pin TSOP, 40-pin TSOP, and 44-pin SO packages. The device is also available in Known Good Die (KGD) form. For more information, refer to publication number 21551. This device is designed to be programmed in-system with the standard system 5.0 volt V_{CC} supply. A 12.0 volt V_{PP} is not required for program or erase operations. The device can also be programmed in standard EPROM programmers.

This device is manufactured using AMD's 0.23 µm process technology, and offers all the features and benefits of the Am29F016, which was manufactured using 0.5 µm process technology.

The standard device offers access times of 70, 90, 120, and 150 ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus contention, the device has separate chip enable (CE#), write enable (WE#), and output enable (OE#) controls.

The device requires only a **single 5.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The system can place the device into the **standby mode**. Power consumption is greatly reduced in this mode.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

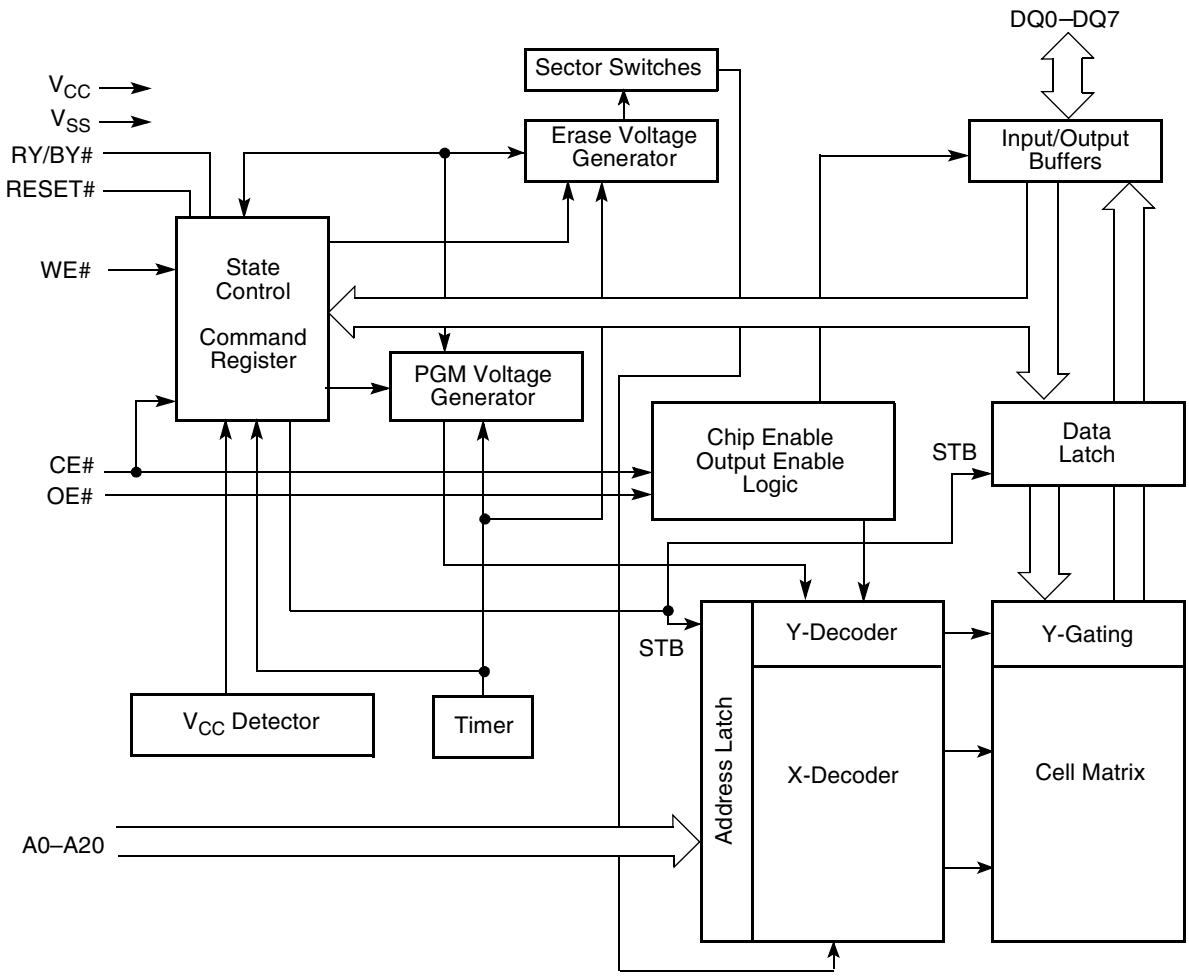
TABLE OF CONTENTS

PRODUCT SELECTOR GUIDE

Family Part Number	Am29F016D			
Speed Options (V_{CC} = 5.0 V ± 10%)	**-70**	**-90**	**-120**	**-150**
Max Access Time (ns)	70	90	120	150
CE# Access (ns)	70	90	120	150
OE# Access (ns)	40	40	50	75

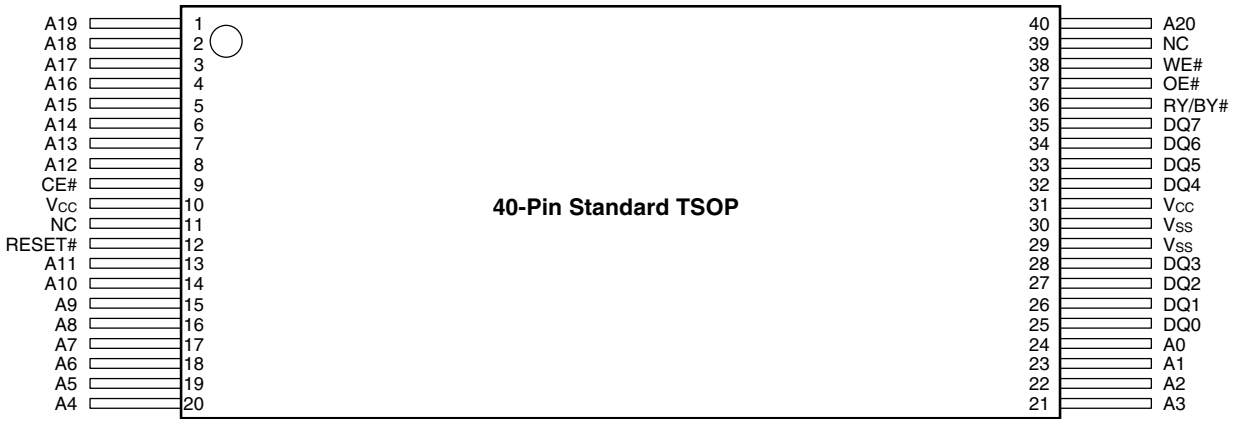
Note: *See the AC Characteristics section for more information.*

BLOCK DIAGRAM

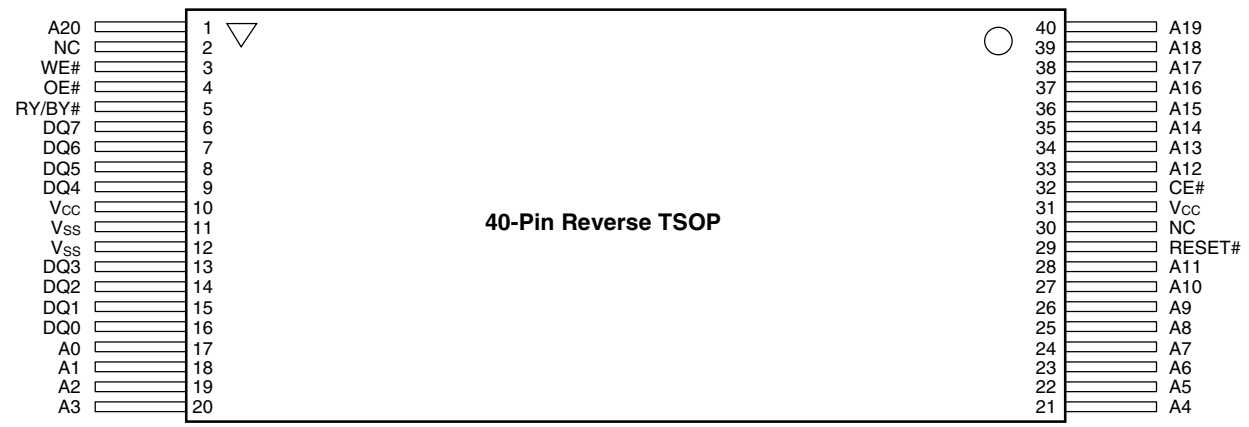


CONNECTION DIAGRAMS

This device is also available in Known Good Die (KGD) form. Refer to publication number 21551 for more information.



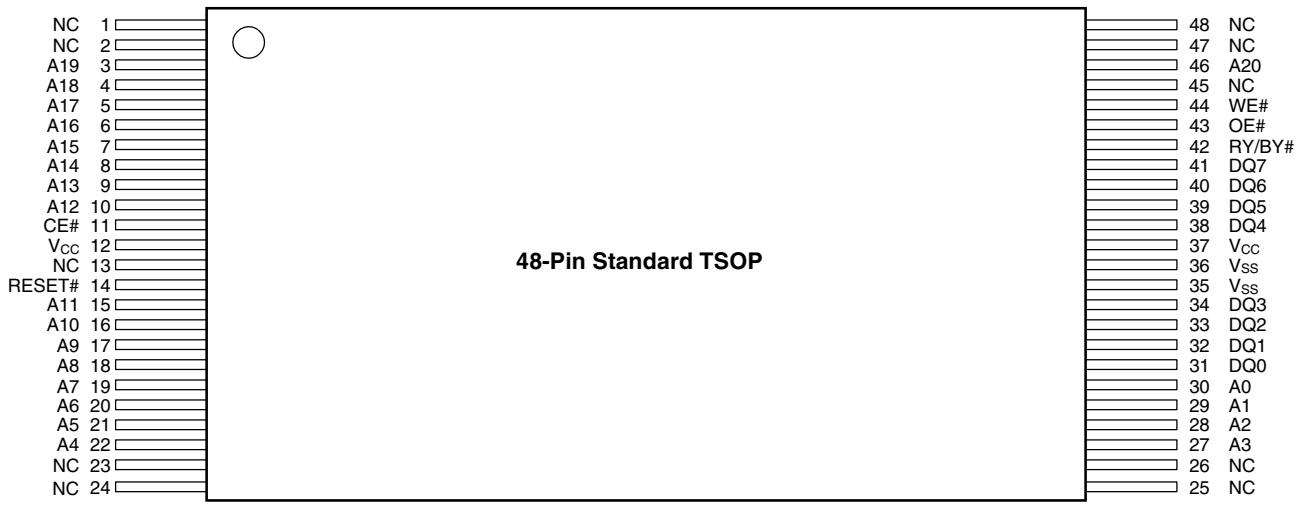
40-Pin Standard TSOP



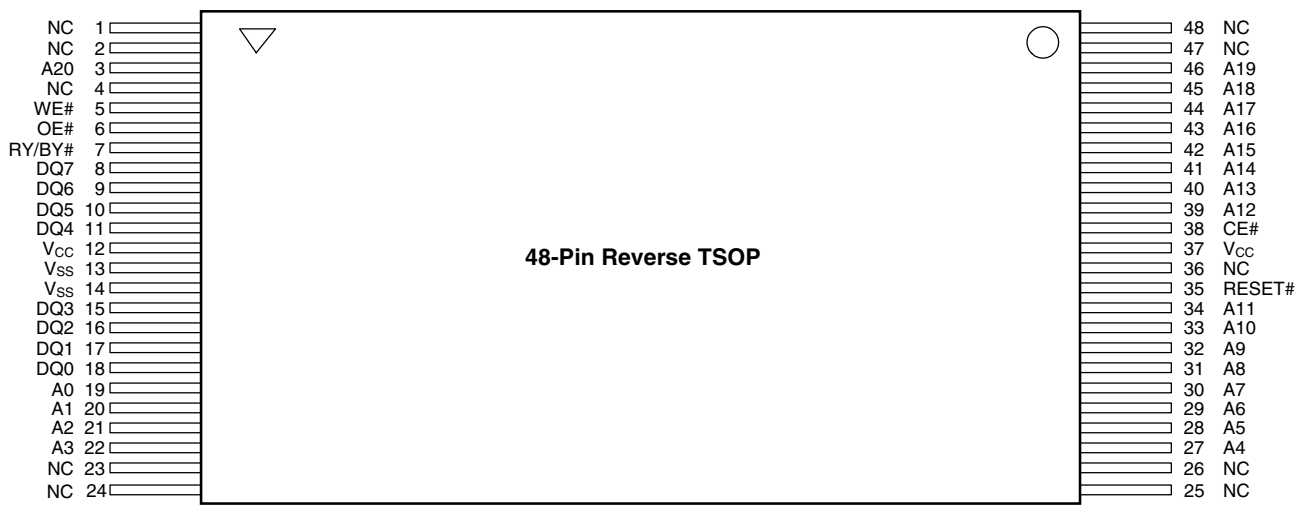
40-Pin Reverse TSOP

CONNECTION DIAGRAMS

This device is also available in Known Good Die (KGD) form. Refer to publication number 21551 for more information.



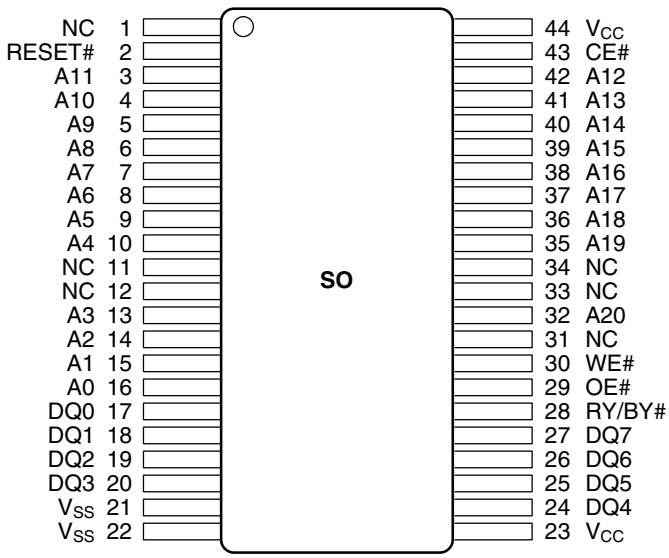
48-Pin Standard TSOP



48-Pin Reverse TSOP

CONNECTION DIAGRAMS

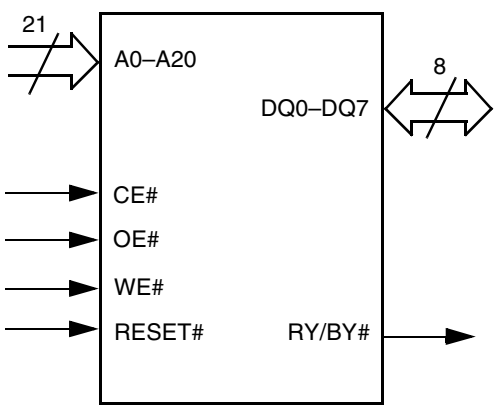
This device is also available in Known Good Die (KGD) form. Refer to publication number 21551 for more information.



PIN CONFIGURATION

A0–A20	=	21 Addresses
DQ0–DQ7	=	8 Data Inputs/Outputs
CE#	=	Chip Enable
WE#	=	Write Enable
OE#	=	Output Enable
RESET#	=	Hardware Reset Pin, Active Low
RY/BY#	=	Ready/Busy Output
V_{CC}	=	+5.0 V single power supply (see Product Selector Guide for device speed ratings and voltage supply tolerances)
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

Am29F016D -70 E I

TEMPERATURE RANGE

C = Commercial (0°C to +70°C)
D = Commercial (0°C to +70°C) with Pb-free package
I = Industrial (–40°C to +85°C)
F = Industrial (–40°C to +85°C)with Pb-free package

PACKAGE TYPE

E = 48-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 048)
F = 48-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR048)
E4 = 40-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 040)
F4 = 40-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR040)
S = 44-Pin Small Outline Package (SO 044)

This device is also available in Known Good Die (KGD) form. See publication number 21551 for more information.

SPEED OPTION

See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION

Am29F016D
16 Megabit (2 M x 8-Bit) CMOS 5.0 Volt-only Sector Erase Flash Memory
5.0 V Read, Program, and Erase

Valid Combinations	
AM29F016D-70	EC, EI, FC, FI, ED, EF, E4D, E4F, SD, SF, E4C, E4I, F4C, F4I, SC, SI
AM29F016D-90	EC, EI, FC, FI, E4C, E4I, F4C, F4I, SC, SI, ED, EF, E4D, E4F, SD, SF
AM29F016D-120	
AM29F016D-150	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29F016D Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	A0–A20	DQ0–DQ7
Read	L	L	H	H	A_{IN}	D_{OUT}
Write	L	H	L	H	A_{IN}	D_{IN}
CMOS Standby	V_{CC} ± 0.5 V	X	X	V_{CC} ± 0.5 V	X	High-Z
TTL Standby	H	X	X	H	X	High-Z
Output Disable	L	H	H	H	X	High-Z
Hardware Reset	X	X	X	L	X	High-Z
Temporary Sector Unprotect (See Note)	X	X	X	V_{ID}	A_{IN}	D_{IN}

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, D_{IN} = Data In, D_{OUT} = Data Out, A_{IN} = Address In

Note: *See the sections on Sector Group Protection and Temporary Sector Unprotect for more information*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to the Read Operations Timings diagram for the timing waveforms. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. See the "Command Definitions" section for details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to each AC Characteristics section for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when CE# and RESET# pins are both held at $V_{CC} \pm 0.5$ V. (Note that this is a more restricted voltage range than V_{IH}.) The device enters the TTL standby mode when CE# and RESET# pins are both held at V_{IH}. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

The device also enters the standby mode when the RESET# pin is driven low. Refer to the next section, "RESET#: Hardware Reset Pin".

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

In the DC Characteristics tables, I_{CC3} represents the standby current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the system drives the RESET# pin low for at least a period of t_{RP}, the device **immediately terminates** any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{IL}, the device enters the TTL standby mode; if RESET# is held at $V_{SS} \pm 0.5$ V, the device enters the CMOS standby mode.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Sector Address Table

Sector	A20	A19	A18	A17	A16	Address Range
SA0	0	0	0	0	0	000000h-00FFFFh
SA1	0	0	0	0	1	010000h-01FFFFh
SA2	0	0	0	1	0	020000h-02FFFFh
SA3	0	0	0	1	1	030000h-03FFFFh
SA4	0	0	1	0	0	040000h-04FFFFh
SA5	0	0	1	0	1	050000h-05FFFFh
SA6	0	0	1	1	0	060000h-06FFFFh
SA7	0	0	1	1	1	070000h-07FFFFh
SA8	0	1	0	0	0	080000h-08FFFFh
SA9	0	1	0	0	1	090000h-09FFFFh
SA10	0	1	0	1	0	0A0000h-0AFFFFh
SA11	0	1	0	1	1	0B0000h-0BFFFFh
SA12	0	1	1	0	0	0C0000h-0CFFFFh
SA13	0	1	1	0	1	0D0000h-0DFFFFh
SA14	0	1	1	1	0	0E0000h-0EFFFFh
SA15	0	1	1	1	1	0F0000h-0FFFFFh
SA16	1	0	0	0	0	100000h-10FFFFh
SA17	1	0	0	0	1	110000h-11FFFFh
SA18	1	0	0	1	0	120000h-12FFFFh
SA19	1	0	0	1	1	130000h-13FFFFh
SA20	1	0	1	0	0	140000h-14FFFFh
SA21	1	0	1	0	1	150000h-15FFFFh
SA22	1	0	1	1	0	160000h-16FFFFh
SA23	1	0	1	1	1	170000h-17FFFFh
SA24	1	1	0	0	0	180000h-18FFFFh
SA25	1	1	0	0	1	190000h-19FFFFh
SA26	1	1	0	1	0	1A0000h-1AFFFFh
SA27	1	1	0	1	1	1B0000h-1BFFFFh
SA28	1	1	1	0	0	1C0000h-1CFFFFh
SA29	1	1	1	0	1	1D0000h-1DFFFFh
SA30	1	1	1	1	0	1E0000h-1EFFFFh
SA31	1	1	1	1	1	1F0000h-1FFFFFh

Note: *All sectors are 64 Kbytes in size.*

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Autoselect Codes (High Voltage Method) table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Table 3. Am29F016D Autoselect Codes (High Voltage Method)

Description	CE#	OE#	WE#	A20-A18	A17-A10	A9	A8-A7	A6	A5-A2	A1	A0	DQ7-DQ0
Manufacturer ID: AMD	L	L	H	X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IL}	01h
Device ID: Am29F016D	L	L	H	X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IH}	ADh
Sector Group Protection Verification	L	L	H	Sector Group Address	X	V_{ID}	X	V_{IL}	X	V_{IH}	V_{IL}	01h (protected)
												00h (unprotected)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Sector Group Protection/Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector group. Each sector group consists of four adjacent sectors. Table 4 shows how the sectors are grouped, and the address range that each sector group contains. The hardware sector group unprotection feature re-enables both program and erase operations in previously protected sector groups.

Sector group protection/unprotection must be implemented using programming equipment. The procedure requires a high voltage (V_{ID}) on address pin A9 and the control pins. Details on this method are provided in a supplement, publication number 23922. Contact an AMD representative to obtain a copy of the appropriate document. Note that the sector group protection and unprotection scheme differs from that used with the previous versions of this device, namely the Am29F016B and Am29F016.

The device is shipped with all sector groups unprotected. AMD offers the option of programming and protecting sector groups at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector group is protected or unprotected. See "Autoselect Mode" for details.

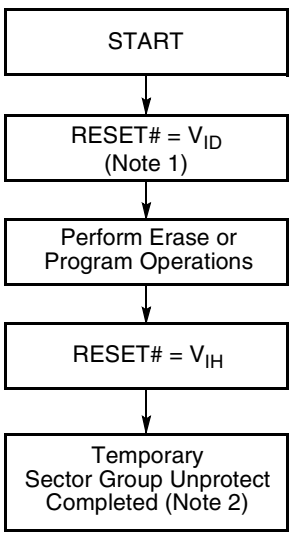
Table 4. Sector Group Addresses

Sector Group	A20	A19	A18	Sectors
SGA0	0	0	0	SA0–SA3
SGA1	0	0	1	SA4–SA7
SGA2	0	1	0	SA8–SA11
SGA3	0	1	1	SA12–SA15
SGA4	1	0	0	SA16–SA19
SGA5	1	0	1	SA20–SA23
SGA6	1	1	0	SA24–SA27
SGA7	1	1	1	SA28–SA31

Temporary Sector Group Unprotect

This feature allows temporary unprotection of previously protected sector groups to change data in-system. The Sector Group Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses.

Once V_{ID} is removed from the RESET# pin, all the previously protected sector groups are protected again. Figure 1 shows the algorithm, and the Temporary Sector Group Unprotect diagram (Figure 16) shows the timing waveforms, for this feature.



Notes:

1. *All protected sector groups unprotected.*
2. *All previously protected sector groups are protected once again.*

Figure 1. Temporary Sector Group Unprotect Operation

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to the Command Definitions table). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 5–8. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 5–8. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/products/nvd/overview/cfi.html. Alternatively, contact an AMD representative for copies of these documents.

Table 5. CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	51h 52h 59h	Query Unique ASCII string “QRY”
13h 14h	02h 00h	Primary OEM Command Set
15h 16h	40h 00h	Address for Primary Extended Table
17h 18h	00h 00h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	00h 00h	Address for Alternate OEM Extended Table (00h = none exists)

Table 6. System Interface String

Addresses	Data	Description
1Bh	45h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	55h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	00h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	00h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	03h	Typical timeout per single byte/word write 2^N µs
20h	00h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	0Ah	Typical timeout per individual block erase 2^N ms
22h	00h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	05h	Max. timeout for byte/word write 2^N times typical
24h	00h	Max. timeout for buffer write 2^N times typical
25h	04h	Max. timeout per individual block erase 2^N times typical
26h	00h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 7. Device Geometry Definition

Addresses	Data	Description
27h	15h	Device Size = 2^N byte
28h 29h	00h 00h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	00h 00h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	01h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	1Fh 00h 00h 01h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)

Table 8. Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	50h 52h 49h	Query-unique ASCII string “PRI”
43h	31h	Major version number, ASCII
44h	31h	Minor version number, ASCII
45h	00h	Address Sensitive Unlock 0 = Required, 1 = Not Required
46h	02h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	04h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	01h	Sector Temporary Unprotect: 00 = Not Supported, 01 = Supported
49h	04h	Sector Protect/Unprotect scheme 01 = 29F040 mode, 02 = 29F016 mode, 03 = 29F400 mode, 04 = 29LV800A mode
4Ah	00h	Simultaneous Operation: 00 = Not Supported, 01 = Supported
4Bh	00h	Burst Mode Type: 00 = Not Supported, 01 = Supported
4Ch	00h	Page Mode Type: 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	00h	ACC supply minimum
4Eh	00h	ACC supply maximum
4Fh	00h	Top/bottom boot sector flag 2 = bottom, 3 = top. If address 2Ch = 01h, ignore this field

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. The Command Definitions table defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/ Erase Resume Commands" for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

See also "Requirements for Reading Array Data" in the "Device Bus Operations" section for more information. The Read Operations table provides the read parameters, and Read Operation Timings diagram shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. The Command Definitions table shows the address and data requirements. This method is an alternative to that shown in the Autoselect Codes (High Voltage Method) table, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in returns 01h if that sector is protected, or 00h if it is unprotected. Refer to the Sector Address tables for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Byte Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verify the programmed cell margin. The Command Definitions take shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See "Write Operation Status" for information on these status bits.

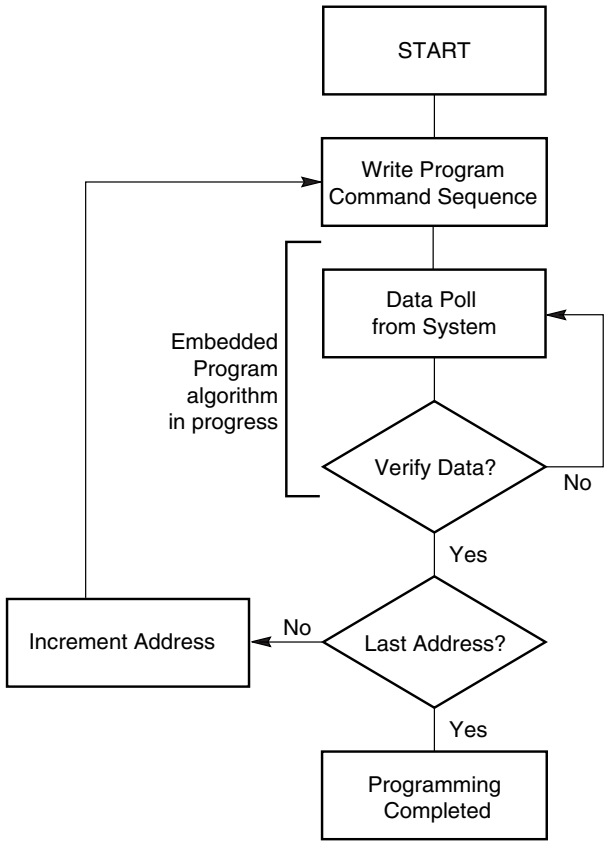
Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a "0" back to a "1".** Attempting to do so may halt the operation and set DQ5 to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 9 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care for both cycles. The device then returns to reading array data.



Note:
See the appropriate Command Definitions table for program command sequence.

Figure 2. Program Operation

Chip Erase Command Sequence

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. See "Write Operation Status" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 3 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to the Chip/Sector Erase Operation Timings for timing waveforms.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the "DQ3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to "Write Operation Status" for information on these status bits.

Figure 3 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't-cares" when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

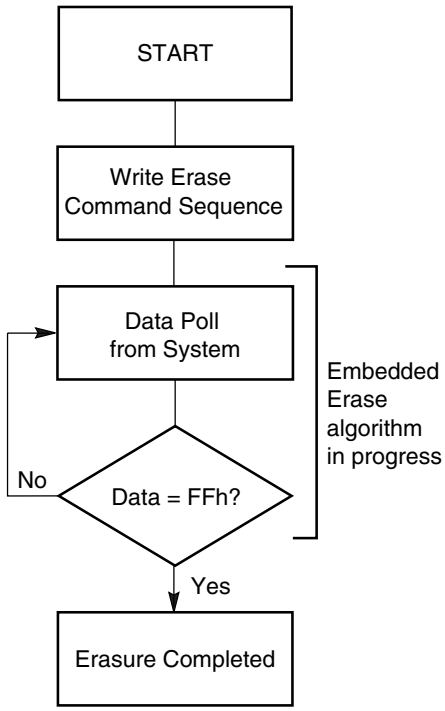
After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or

DQ6 status bits, just as in the standard program operation. See “Write Operation Status” for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See “Autoselect Command Sequence” for more information.

The system must write the Erase Resume command (address bits are “don’t care”) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.



Notes:

1. *See the appropriate Command Definitions table for erase command sequence.*
2. *See “DQ3: Sector Erase Timer” for more information.*

Figure 3. Erase Operation

Command Definitions

Table 9. Am29F016D Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–4)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
	Device ID	4	555	AA	2AA	55	555	90	X01	AD				
	Sector Group Protect Verify (Note 8)	4	555	AA	2AA	55	555	90	SGA X02	XX00				
										XX01				
CFI Query (Note 9)		1	55	98										
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 10)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 9)		1	XXX	B0										
Erase Resume (Note 10)		1	XXX	30										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A20–A16 select a unique sector.

SGA = Address of the sector group to be verified. Address bits A20–A18 select a unique sector group.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except when reading array or autoselect data, all bus cycles are write operations.*
4. *Address bits A20–A11 are don't cares for unlock and command cycles, unless SA or PA required.*
5. *No unlock or command cycles required when reading array data.*
6. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
7. *The fourth cycle of the autoselect command sequence is a read cycle.*
8. *The data is 00h for an unprotected sector group and 01h for a protected sector group.See "Autoselect Command Sequence" for more information.*
9. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
10. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
11. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.*
12. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
13. *The Erase Resume command is valid only during the Erase Suspend mode.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 10 and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

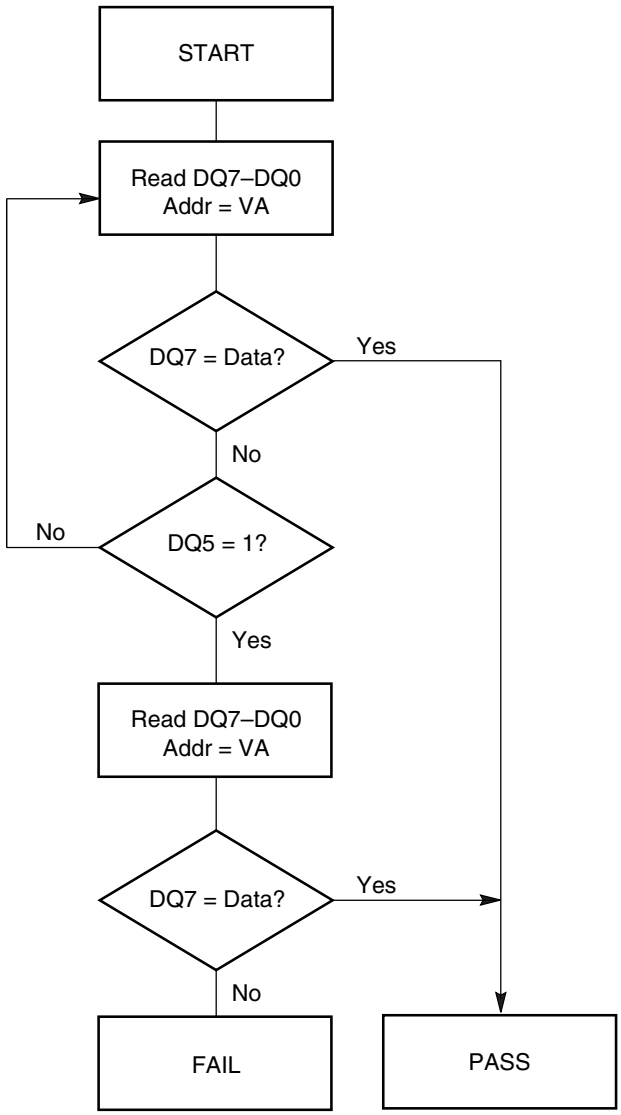
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 2 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to “1”; prior to this, the device outputs the “complement,” or “0.” The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. The Data# Polling Timings (During Embedded Algorithms) figure in the “AC Characteristics” section illustrates this.

Table 10 shows the outputs for Data# Polling on DQ7. Figure 4 shows the Data# Polling algorithm.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 4. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 10 shows the outputs for RY/BY#. The timing diagrams for read, reset, program, and erase shows the relationship of RY/BY# to other signals.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either OE# or CE# to control the read cycles.) When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 μs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on “DQ7: Data# Polling”).

If a program address falls within a protected sector, DQ6 toggles for approximately 2 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

The Write Operation Status table shows the outputs for Toggle Bit I on DQ6. Refer to Figure 5 for the toggle bit algorithm, and to the Toggle Bit Timings figure in the “AC Characteristics” section for the timing diagram. The DQ2 vs. DQ6 figure shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on “DQ2: Toggle Bit II”.

DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 10 to compare outputs for DQ2 and DQ6.

Figure 5 shows the toggle bit algorithm in flowchart form, and the section “DQ2: Toggle Bit II” explains the algorithm. See also the “DQ6: Toggle Bit I” subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The DQ2 vs. DQ6 figure shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 5 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and

the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 5).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed.

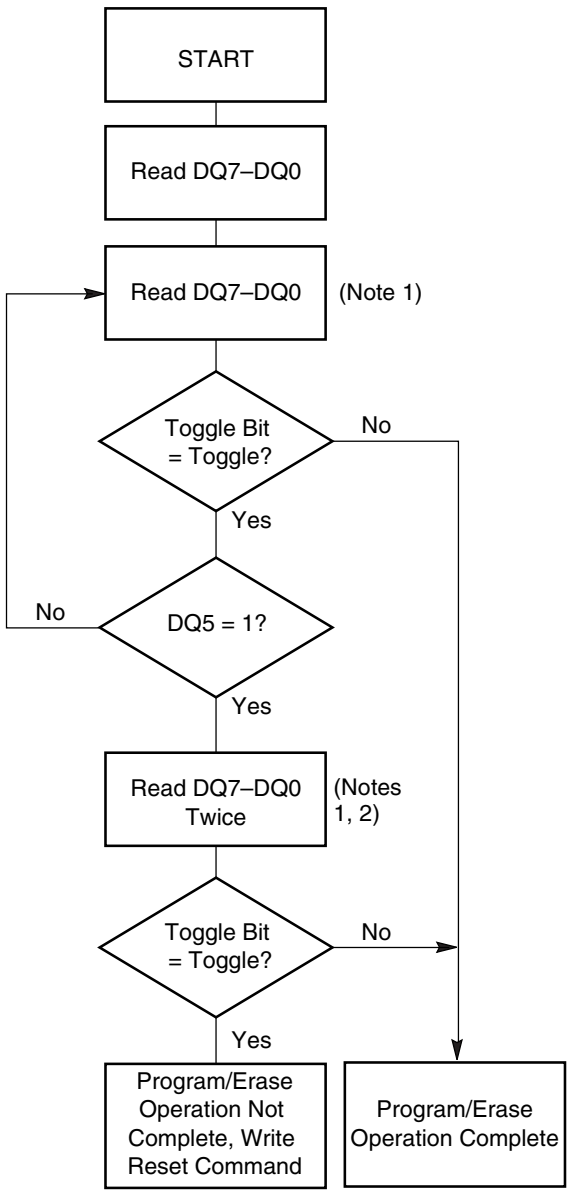
The DQ5 failure condition may appear if the system tries to program a "1" to a location that is previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a "1."

Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from "0" to "1." The system may ignore DQ3 if the system can guarantee that the time between additional sector erase commands will always be less than 50 µs. See also the "Sector Erase Command Sequence" section.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is "1", the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 10 shows the outputs for DQ3.



Notes:

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to "1". See text.*

Figure 5. Toggle Bit Algorithm

Table 10. Write Operation Status

Operation		DQ7 (Note 1)	DQ6	DQ5 (Note 2)	DQ3	DQ2 (Note 1)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
2. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "DQ5: Exceeded Timing Limits" for more information.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +125°C

Ambient Temperature
with Power Applied. . . . . –55°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –2.0 V to 7.0 V

A9, OE#, RESET# (Note 2) . . . . . –2.0 V to 12.5 V

All other pins (Note 1) . . . . . –2.0 V to 7.0 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See . Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See .*
2. *Minimum DC input voltage on A9, OE#, RESET# pins is –0.5 V. During voltage transitions, A9, OE#, RESET# pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See . Maximum DC input voltage on A9, OE#, and RESET# is 12.5 V which may overshoot to 13.5 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses greater than those listed in this section may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

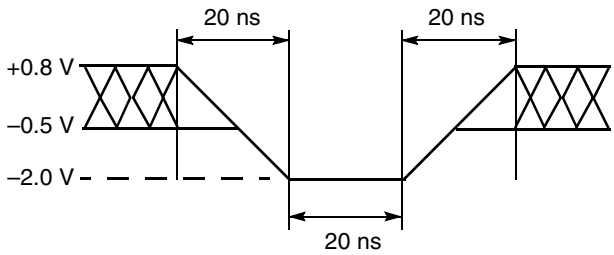


Figure 6. Maximum Negative Overshoot Waveform

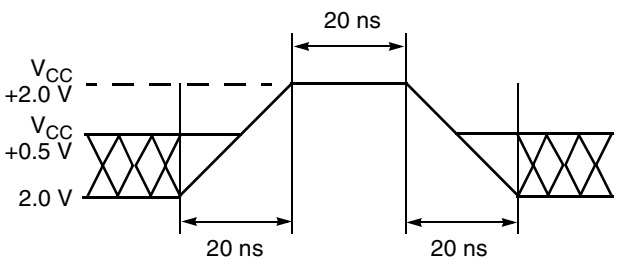


Figure 7. Maximum Positive Overshoot Waveform

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_C) . . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_C) . . . . . –40°C to +85°C

V_{CC} Supply Voltages

V_{CC} for ± 10% devices . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{CC1}	V_{CC} Read Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}		25	40	mA
I_{CC2}	V_{CC} Write Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}		40	60	mA
I_{CC3}	V_{CC} Standby Current (CE# Controlled)	$V_{CC} = V_{CC}$ Max, CE# = V_{IH}, RESET# = V_{IH}		0.4	1.0	mA
I_{CC4}	V_{CC} Standby Current (RESET# Controlled)	$V_{CC} = V_{CC}$ Max, RESET# = V_{IL}		0.4	1.0	mA
V_{IL}	Input Low Level		–0.5		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.0 V	11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH}	Output High Level	I_{OH} = –2.5 mA $V_{CC} = V_{CC}$ Min	2.4			V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2		4.2	V

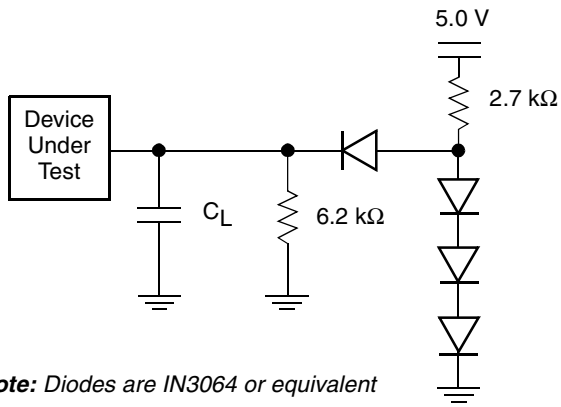
CMOS Compatible

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{CC1}	V_{CC} Read Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}		25	40	mA
I_{CC2}	V_{CC} Write Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}		30	40	mA
I_{CC3}	V_{CC} Standby Current (CE# Controlled) (Note 4)	$V_{CC} = V_{CC}$ Max, CE# = V_{CC} ± 0.5 V, RESET# = V_{CC} ± 0.5 V		1	5	µA
I_{CC4}	V_{CC} Standby Current (RESET# Controlled) (Note 4)	$V_{CC} = V_{CC}$ Max, RESET# = V_{SS} ± 0.5 V		1	5	µA
V_{IL}	Input Low Level		–0.5		0.8	V
V_{IH}	Input High Level		0.7x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.0 V	11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min	V_{CC} – 0.4			V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2		4.2	V

Notes for DC Characteristics (both tables):

1. *The I_{CC} current is typically less than 1 mA/MHz, with OE# at V_{IH}.*
2. *I_{CC} active while Embedded Program or Embedded Erase algorithm is in progress.*
3. *Not 100% tested.*
4. *For CMOS mode only I_{CC3}, I_{CC4} = 20 µA at extended temperature (>+85°C).*

TEST CONDITIONS



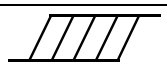
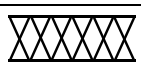
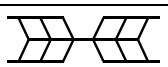
Note: *Diodes are IN3064 or equivalent*

Figure 8. Test Setup

Table 11. Test Specifications

Test Condition	All speed options	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	100	pF
Input Rise and Fall Times	20	ns
Input Pulse Levels	0.45–2.4	V
Input timing measurement reference levels	0.8	V
Output timing measurement reference levels	2.0	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

KS000010-PAL

AC CHARACTERISTICS

Read-only Operations

Parameter Symbol		Parameter Description		Test Setup		Speed Options				Unit
JEDEC	Std					-70	-90	-120	-150	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	90	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		$CE\# = V_{IL}$ $OE\# = V_{IL}$	Max	70	90	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		$OE\# = V_{IL}$	Max	70	90	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	40	40	50	55	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0	0	0	0	ns
			Toggle and Data# Polling		Min	10	10	10	10	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	20	20	30	35	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	20	20	30	35	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses CE# or OE# Whichever Occurs First			Min	0	0	0	0	ns
	t_{Ready}	RESET# Pin Low to Read Mode (Note 1)			Max	20	20	20	20	µs

Notes:

1. *Not 100% tested.*
2. *Refer to and for test specifications.*

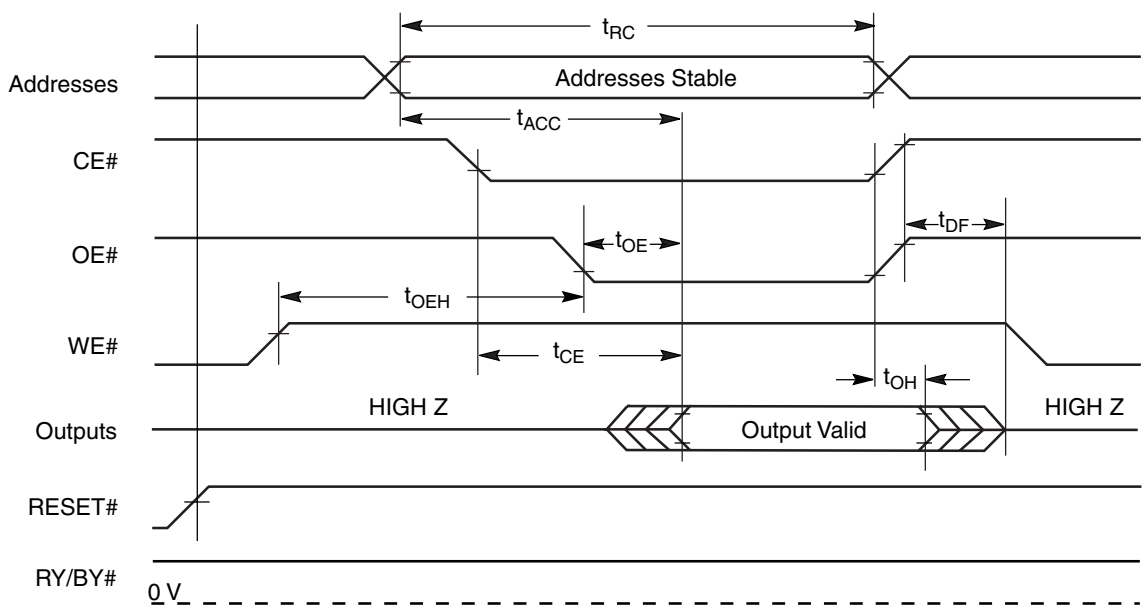


Figure 9. Read Operation Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std					
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	RESET# Pulse Width		Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)		Min	50	ns
	t_{RB}	RY/BY# Recovery Time		Min	0	ns

Note:
Not 100% tested.

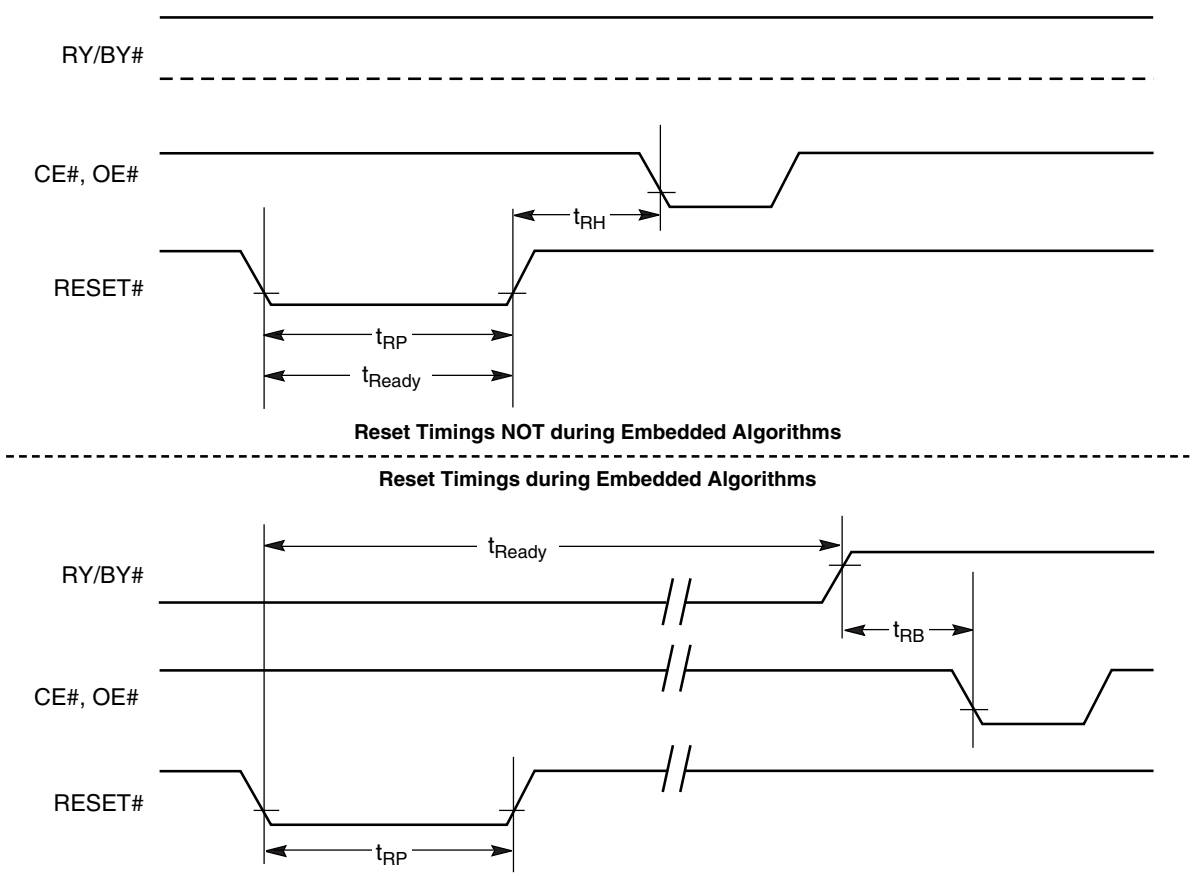


Figure 10. RESET# Timings

AC CHARACTERISTICS

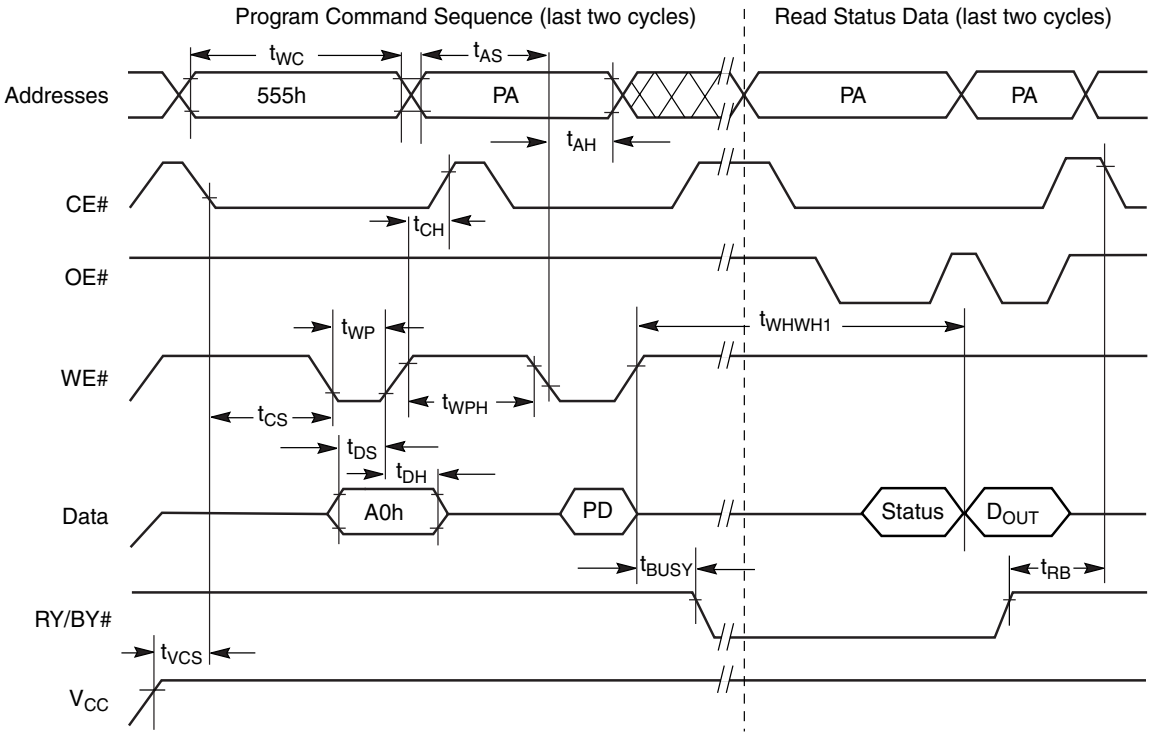
Erase/Program Operations

Parameter		Parameter Description		Speed Options				Unit
JEDEC	Std			-70	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	70	90	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	40	45	50	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	40	45	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OES}	Output Enable Setup Time	Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write (OE# high to WE# low)	Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	40	45	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20				ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 2)	Typ	7				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	1				sec
			Max	8				sec
	t_{VCS}	V_{CC} Set Up Time (Note 1)	Min	50				µs
	t_{BUSY}	WE# to RY/BY# Valid	Min	40	40	50	60	ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*

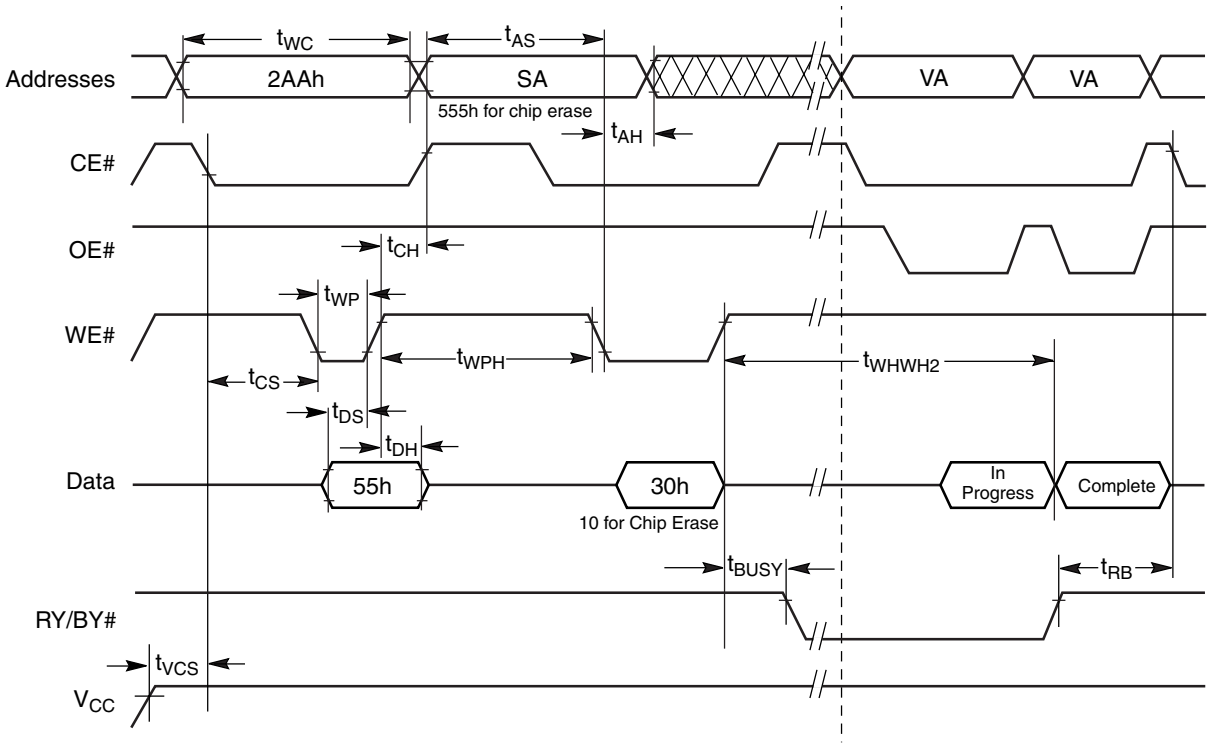
AC CHARACTERISTICS



Note: *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*

Figure 11. Program Operation Timings

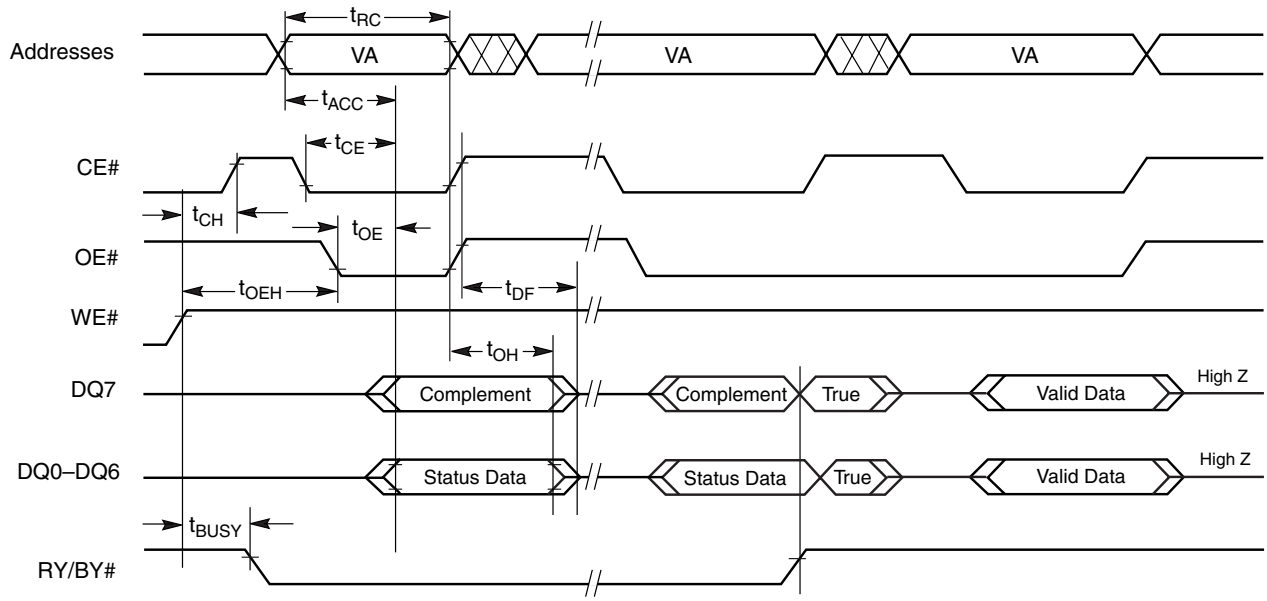
AC CHARACTERISTICS



Note:
SA = Sector Address. VA = Valid Address for reading status data.

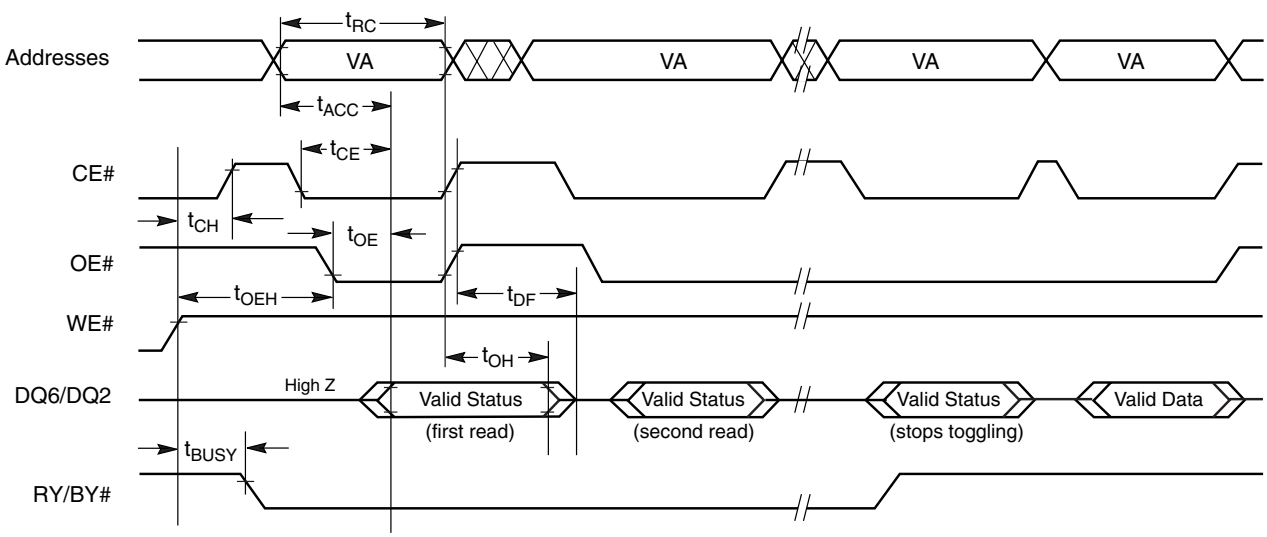
Figure 12. Chip/Sector Erase Operation Timings

AC CHARACTERISTICS



Note:
VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

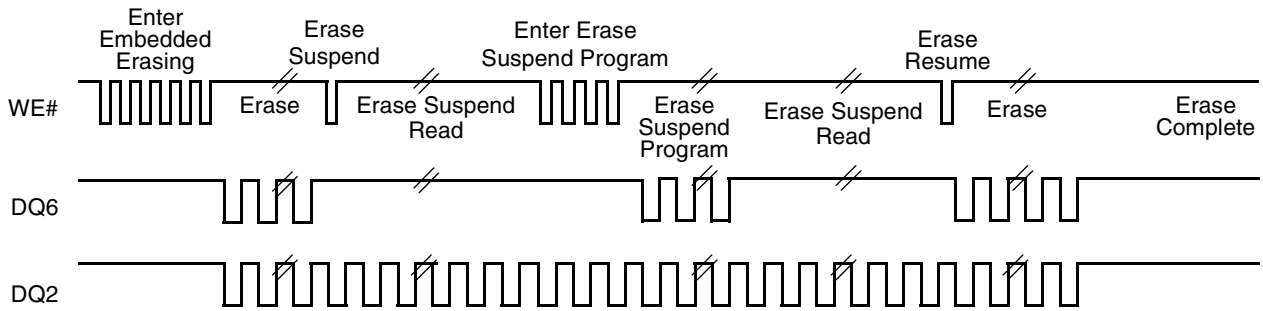
Figure 13. Data# Polling Timings (During Embedded Algorithms)



Note:
VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 14. Toggle Bit Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note:
The system may use OE# or CE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within the erase-suspended sector.

Figure 15. DQ2 vs. DQ6

Temporary Sector Unprotect

Parameter					
JEDEC	Std	Description		All Speed Options	Unit
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note:
Not 100% tested.

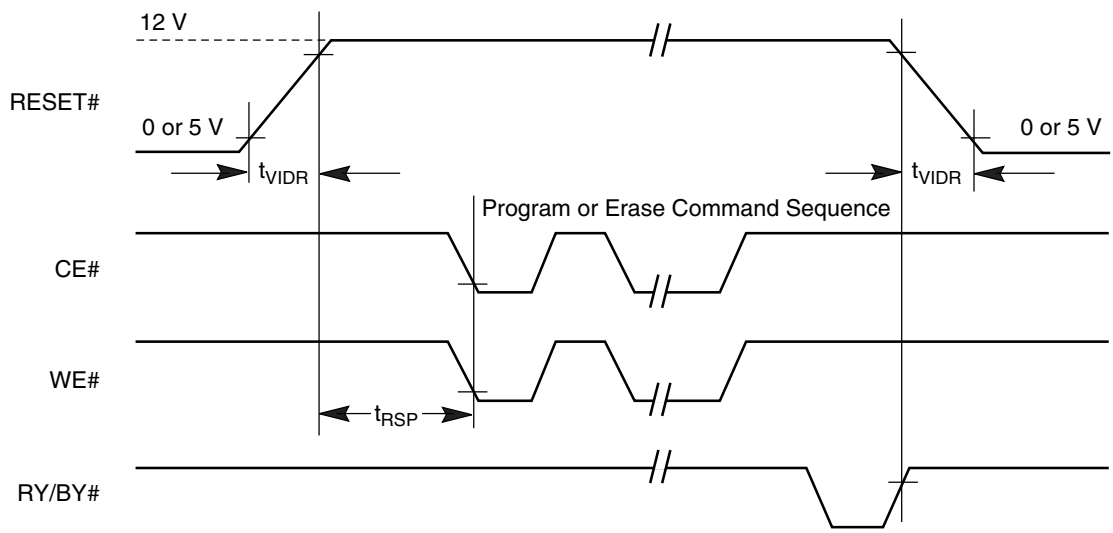


Figure 16. Temporary Sector Group Unprotect Timings

AC CHARACTERISTICS

Erase and Program Operations

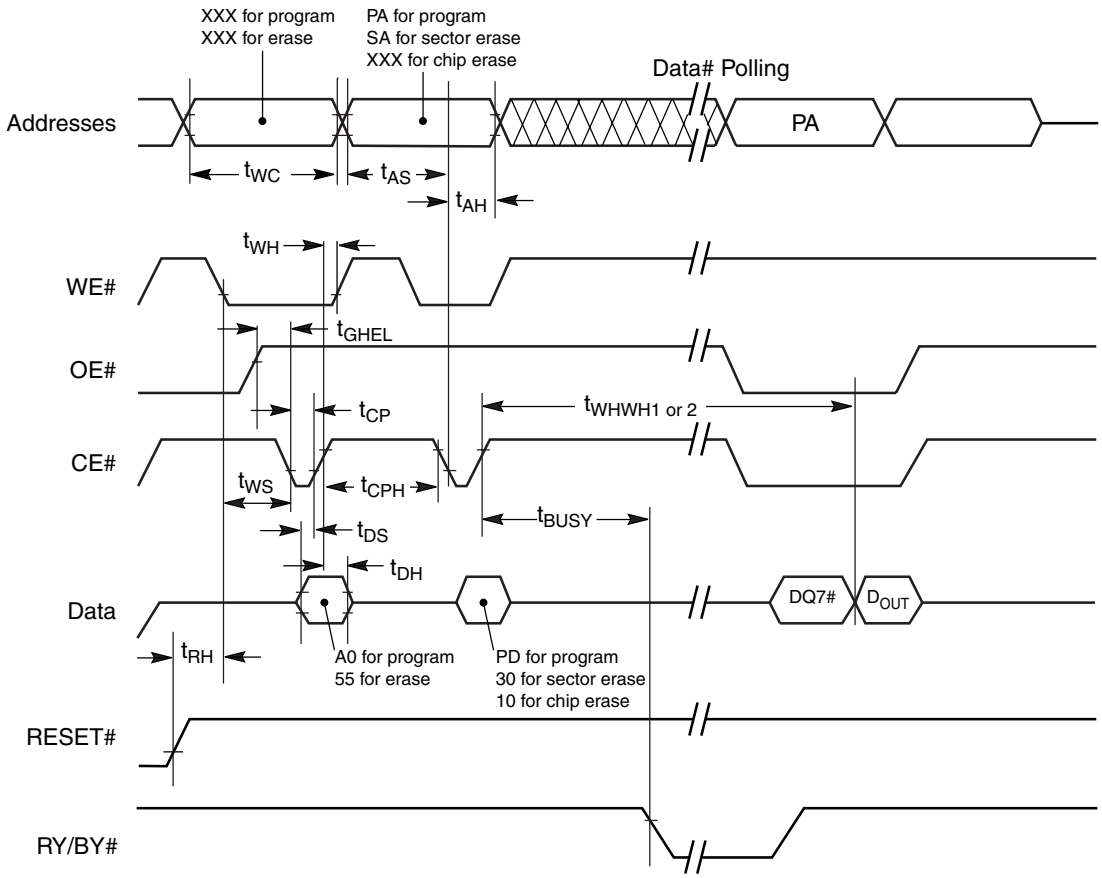
Alternate CE# Controlled Writes

Parameter Symbol		Parameter Description		Speed Options				Unit
JEDEC	Std			-70	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	70	90	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	40	45	50	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	40	45	50	50	ns
t_{EHDX}	t_{DH}	Address Hold Time	Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	Min	0				ns
t_{WLEL}	t_{WS}	CE# Setup Time	Min	0				ns
t_{EHWH}	t_{WH}	CE# Hold Time	Min	0				ns
t_{ELEH}	t_{CP}	Write Pulse Width	Min	40	45	50	50	ns
t_{EHEL}	t_{CPH}	Write Pulse Width High	Min	20				ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 2)	Typ	7				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	1				sec
			Max	8				sec

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*

AC CHARACTERISTICS



Notes:

1. *PA = Program Address, PD = Program Data, SA = Sector Address, DQ7# = Complement of Data Input, D_{OUT} = Array Data.*
2. *Figure indicates the last two bus cycles of the command sequence.*

Figure 17. Alternate CE# Controlled Write Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	1	8	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	32	256	sec	
Byte Programming Time	7	300	µs	Excludes system-level overhead (Note 5)
Chip Programming Time (Note 3)	14.4	43.2	sec	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 5.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 4.5 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum byte program time listed. If the maximum byte program time given is exceeded, only then does the device set DQ5 = 1. See the section on DQ5 for further information.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the four-bus-cycle sequence for programming. See Table 6 for further information on command definitions.*
6. *The device has a guaranteed minimum erase and program cycle endurance of 1,000,000 cycles.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 Volt, one pin at a time.*

TSOP AND SO PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

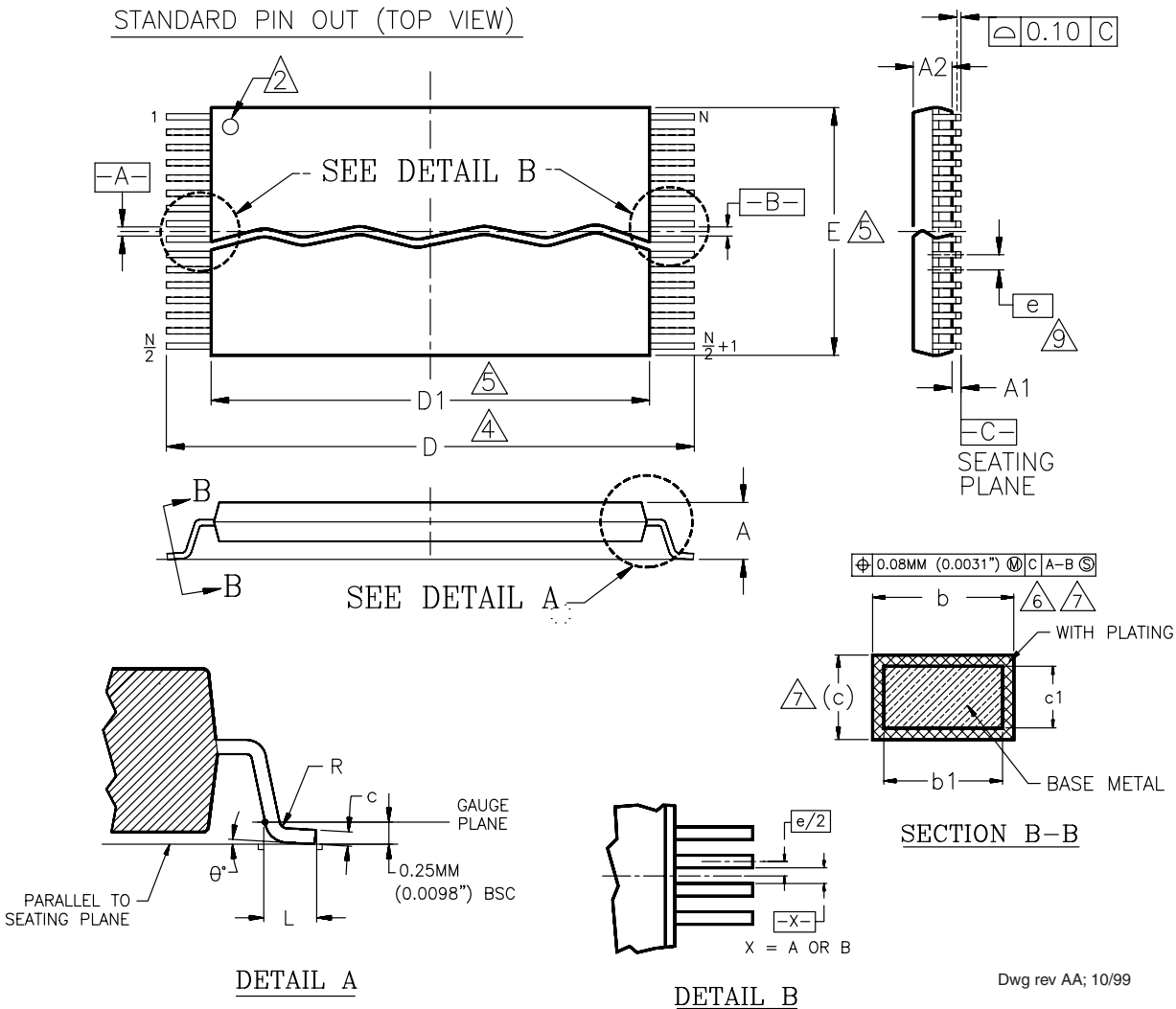
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS

TS 040—40-Pin Standard Thin Small Outline Package



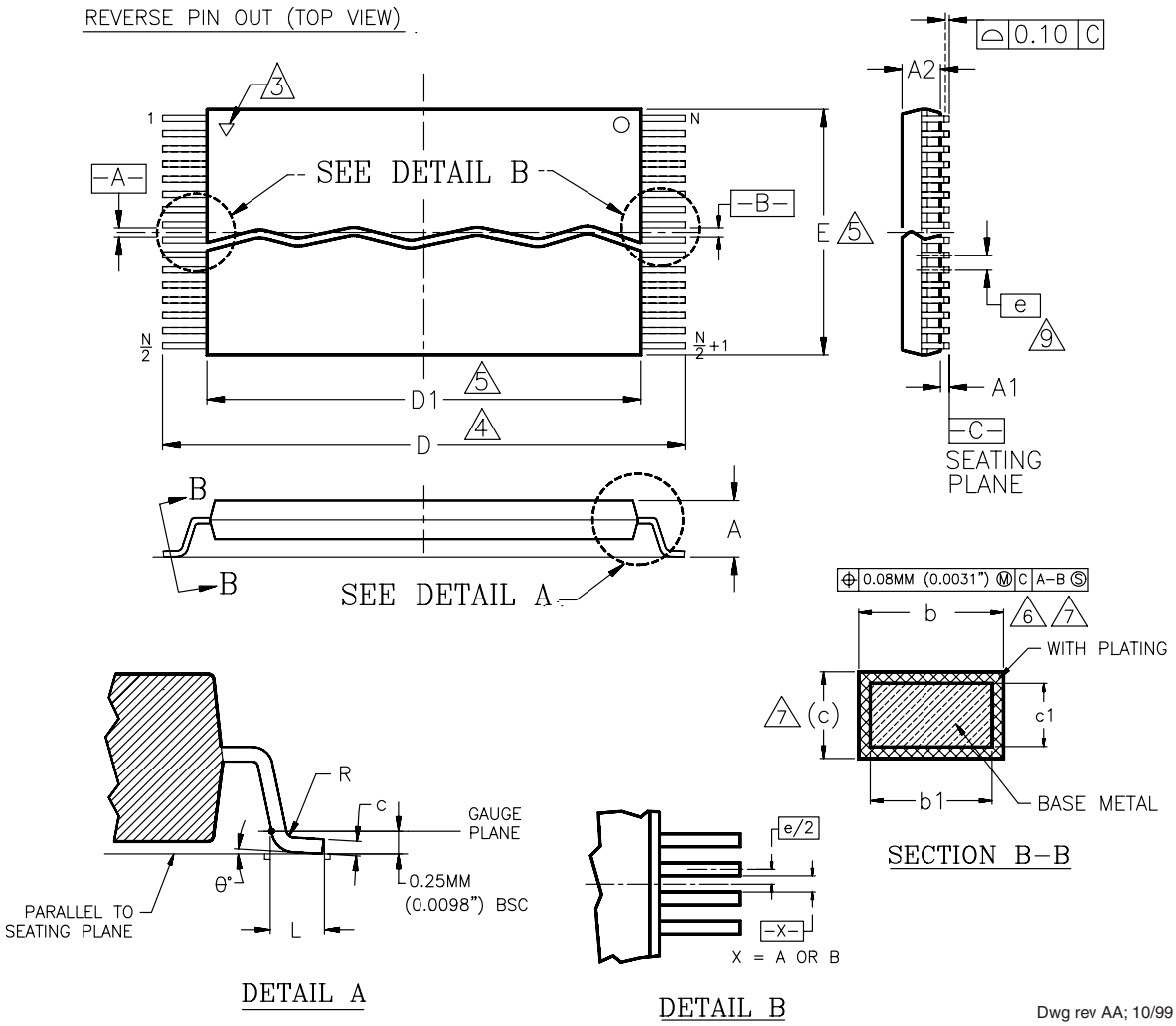
Package	TS 40		
Jedec	MO-142 (B) CD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	9.90	10.00	10.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	40		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. `PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

PHYSICAL DIMENSIONS (continued)

TSR040—40-Pin Reverse Thin Small Outline Package



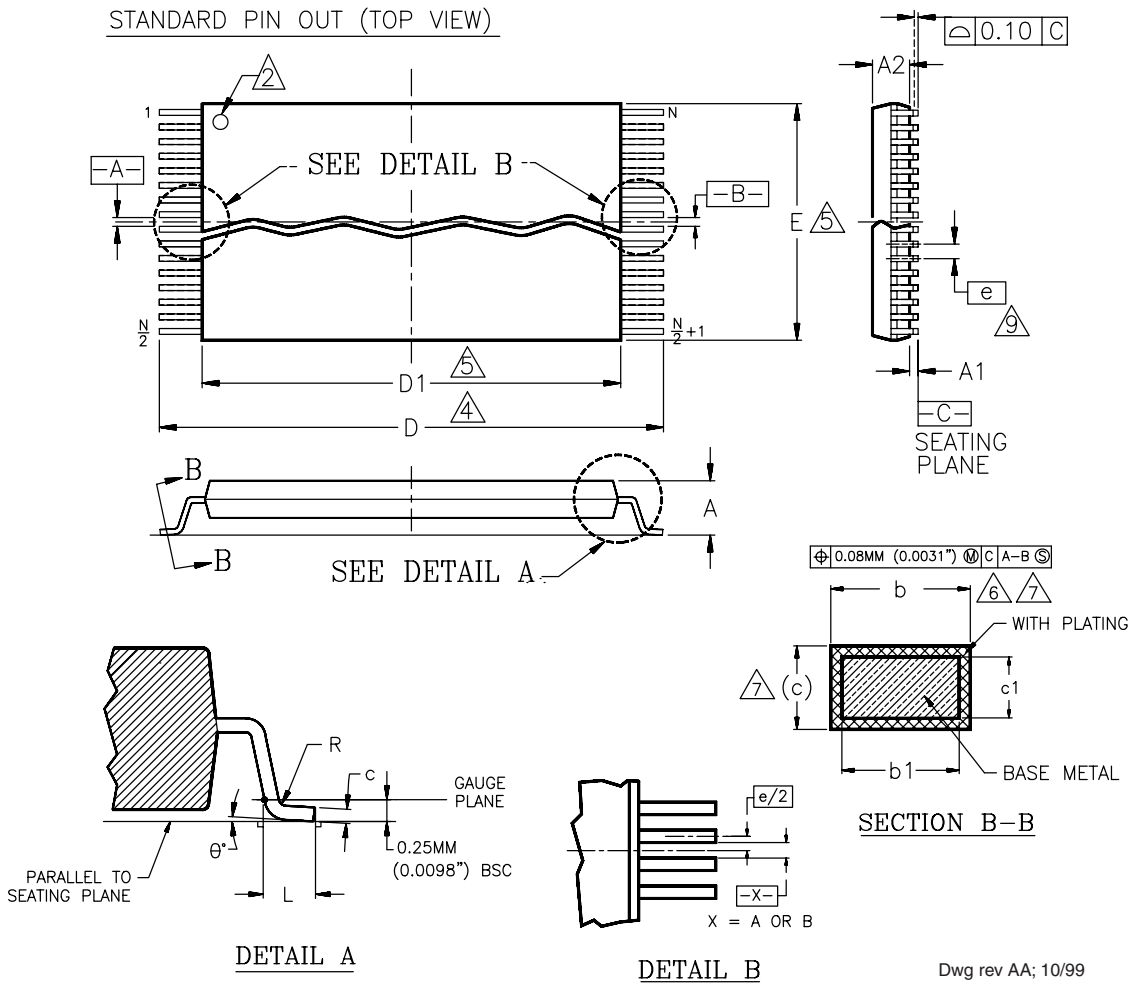
Package	TSR 40		
Jedec	MO-142 (B) CD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	9.90	10.00	10.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	40		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

PHYSICAL DIMENSIONS (continued)

TS 048—48-Pin Standard Thin Small Outline Package



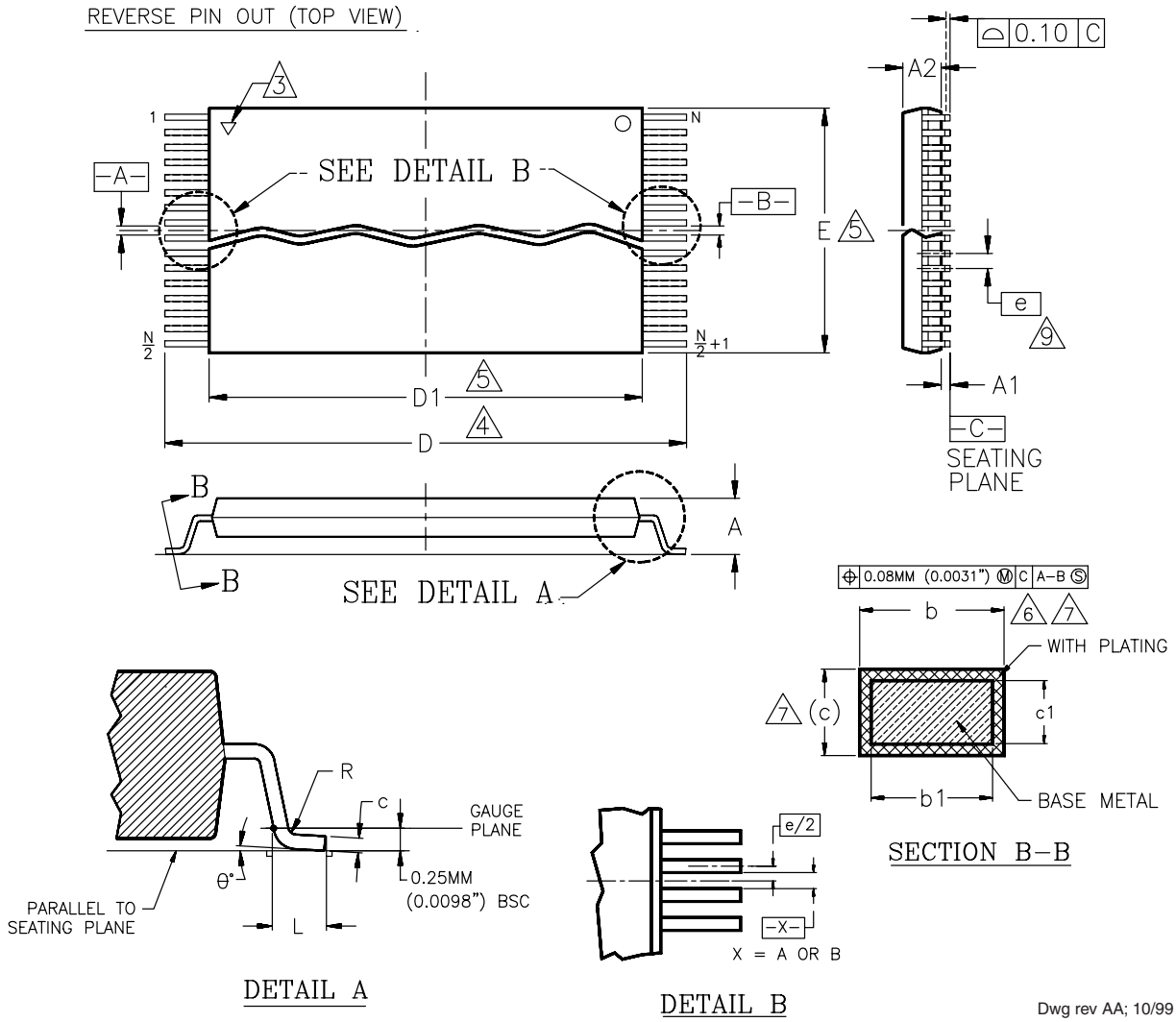
Package	TS 48		
Jedec	MO-142 (B) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	48		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

PHYSICAL DIMENSIONS (continued)

TSR048—48-Pin Reverse Thin Small Outline Package



Dwg rev AA; 10/99

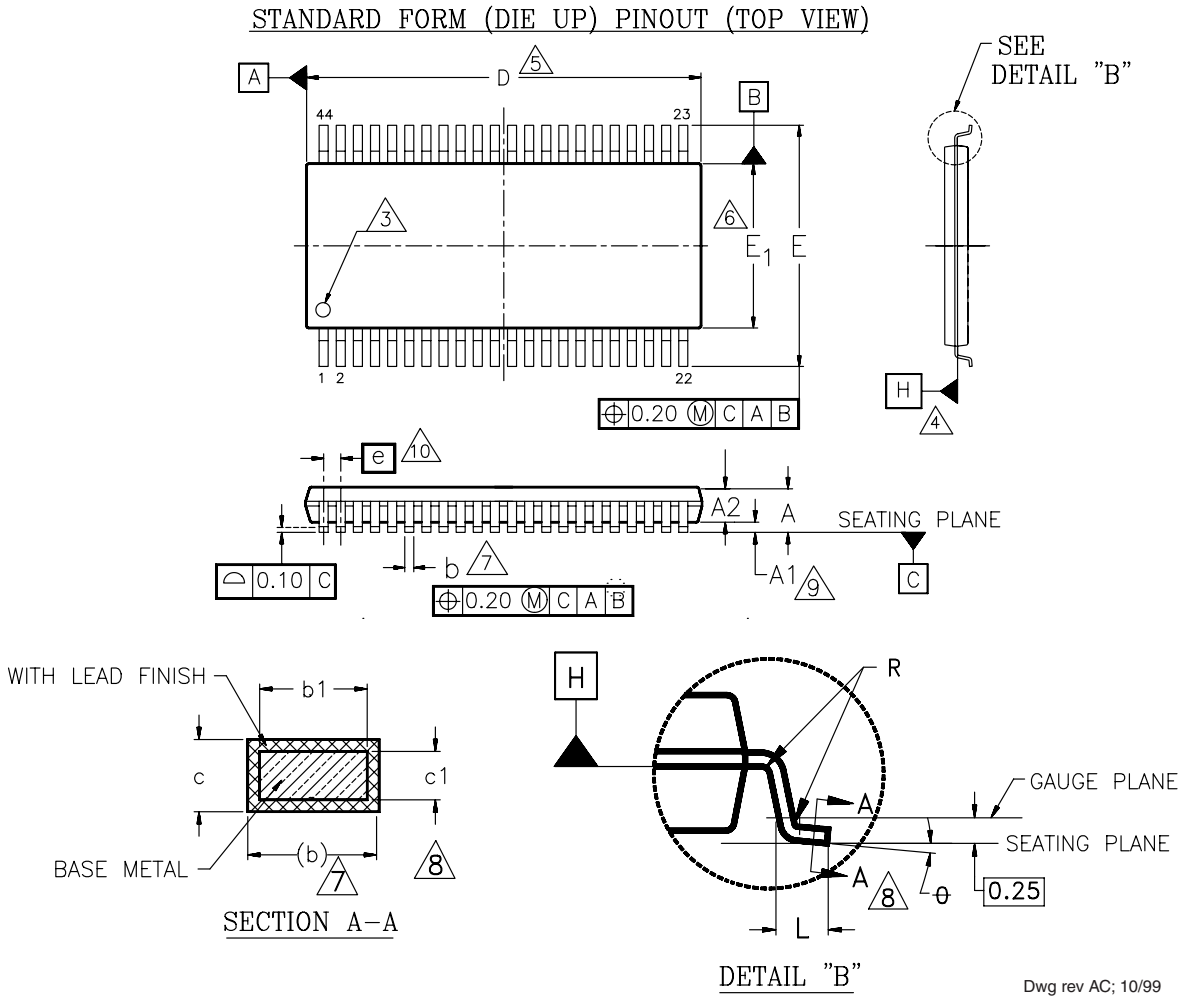
Package	TSR 48		
Jedec	MO-142 (B) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	48		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

PHYSICAL DIMENSIONS (continued)

SO 044—44-Pin Small Outline Package



PACKAGE	SO 044		
JEDEC	MO–180 (A) AA		
SYMBOL	MIN	NOM	MAX
A	—	—	2.80
A1	0.15	0.23	0.35
A2	2.17	2.30	2.45
b	0.35	—	0.50
b1	0.35	0.40	0.45
c	0.10	—	0.21
c1	0.10	0.15	0.18
D	28.00	28.20	28.40
E	15.70	16.00	16.30
E1	13.10	13.30	13.50
e	1.27 BSC		
L	0.60	0.80	1.00
R	0.09	—	—
θ	0°	4°	8°

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm).
2. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994.
3. PIN 1 IDENTIFIER FOR STANDARD FORM (DIE UP) OR REVERSE FORM (DIE DOWN) PINOUTS.
4. DATUMS A AND B AND DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END.
6. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT EXCEED 0.15 mm PER SIDE. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07 mm AT LEAST MATERIAL CONDITION.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIPS.
9. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE.
10. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
11. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THER SEATING PLANE.

REVISION SUMMARY

Revision A (May 1997)

Initial release of Am29F016B (0.35 µm) device.

Revision B (January 1998)

Global

Made formatting and layout consistent with other data sheets. Used updated common tables and diagrams.

Revision B+1 (January 1998)

AC Characteristics—Read-only Operations

Deleted note referring to output driver disable time.

Figure 16—Temporary Sector Group Unprotect Timings

Corrected title to indicate "sector group."

Revision B+2 (April 1998)

Global

Added -70 speed option, deleted -75 speed option.

Distinctive Characteristics

Changed minimum 100K write/erase cycles guaranteed to 1,000,000.

Ordering Information

Added extended temperature availability to -90, -120, and -150 speed options.

Operating Ranges

Added extended temperature range.

DC Characteristics, CMOS Compatible

Corrected the CE# and RESET# test conditions for I_{CC3} and I_{CC4} to V_{CC} ±0.5 V.

AC Characteristics

Erase/Program Operations; Erase and Program Operations Alternate CE# Controlled Writes: Corrected the notes reference for t_{WHWH1} and t_{WHWH2}. These parameters are 100% tested. Corrected the note reference for t_{VCS}. This parameter is not 100% tested.

Temporary Sector Unprotect Table

Added note reference for t_{VIDR}. This parameter is not 100% tested.

Erase and Programming Performance

Changed minimum 100K program and erase cycles guaranteed to 1,000,000.

Revision C (January 1999)

Global

Updated for CS39S process technology.

Distinctive Characteristics

Added:

- 20-year data retention at 125°C
  - — Reliable operation for the life of the system

DC Characteristics—CMOS Compatible

I_{CC3}, I_{CC4}: Added Note 4, "For CMOS mode only I_{CC3}, I_{CC4} = 20 µA at extended temperature (>+85°C)".

DC Characteristics—TTL/NMOS Compatible and CMOS Compatible

I_{CC1}, I_{CC2}, I_{CC3}, I_{CC4}: Added Note 2 "Maximum I_{CC} specifications are tested with $V_{CC} = V_{CCmax}$".

I_{CC3}, I_{CC4}: Deleted $V_{CC} = V_{CC}$Max.

Revision C+1 (March 23, 1999)

Operating Ranges

The temperature ranges are now specified as ambient.

Revision C+2 (May 17, 1999)

Product Selector Guide

Corrected the t_{OE} specification for the -150 speed option to 55 ns.

Operating Ranges

V_{CC} Supply Voltages: Added "V_{CC} for ± 5% devices . +4.75 V to +5.25 V".

Revision C+3 (July 2, 1999)

Global

Added references to availability of device in Known Good Die (KGD) form.

Revision D (November 16, 1999)

AC Characteristics—Figure 11. Program Operations Timing and Figure 12. Chip/Sector Erase Operations

Deleted t_{GHWL} and changed OE# waveform to start at high.

Physical Dimensions

Replaced figures with more detailed illustrations.

Revision E (May 19, 2000)

Global

Changed part number to Am29F016D. This reflects the new 0.23 µm process technology upon which this device will now be built.

The Am29F016D is compatible with the previous 0.32 µm Am29F016B device, with the exception of the sector group protect and unprotect algorithms. These algorithms are provided in a seperate document. Contact AMD for more information or to request a copy of that document.

This data sheet will be marked preliminary until the device has been in full production for a number of months.

The -75 speed option (70 ns, ±5% V_{CC}) has been replaced by a -70 speed option (70 ns, ±10 V_{CC}).

The burn-in option is no longer available.

The device now has the Unlock Bypass Program feature.

The publication number of the document describing sector protection/unprotection implementation is now 23922.

Revision E+1 (December 4, 2000)

Global

Added table of contents. Removed Preliminary status from document.

Revision E+2 (March 23, 2001)

Common Flash Memory Interface (CFI)

Added section.

Table 9, Am29F016D Command Definitions

Corrected the addresses for the three-cycle unlock bypass command sequence. Added Note 9 and CFI Query command to table.

Revision E+3 (June 4, 2004)

Ordering Information

Added Lead-free (Pb-free) options to the Temperature Range breakout of the OPN table and the Valid Combinations table..