

# PSMN035-150B

## N-channel TrenchMOS SiliconMAX standard level FET

Rev. 04 — 17 November 2009

Product data sheet

## 1. Product profile

### 1.1 General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

### 1.3 Applications

- Switched-mode power supplies

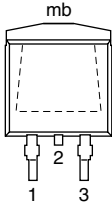
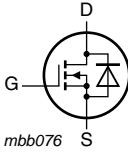
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	150	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> and <a href="#">2</a>	-	-	50	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	-	250	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 50\text{ A}$ ; $V_{DS} = 120\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 13</a>	-	33	45	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	30	35	m $\Omega$

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain <a href="#">[1]</a>		
3	S	source		
mb	D	mounting base; connected to drain		

**SOT404 (D2PAK)**

[1] It is not possible to make connection to pin 2.

## 3. Ordering information

Table 3. Ordering information

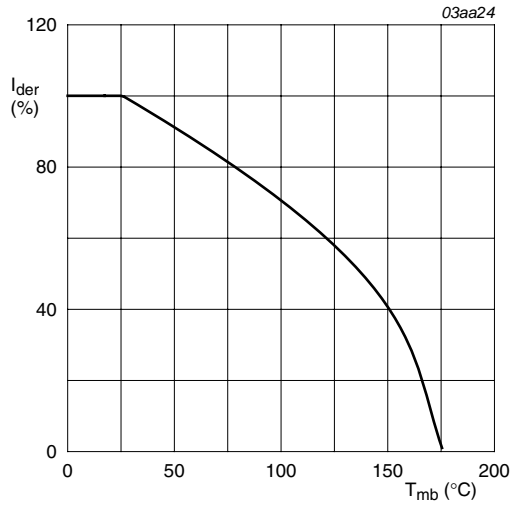
Type number	Package		Version
	Name	Description	
PSMN035-150B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Limiting values

Table 4. Limiting values

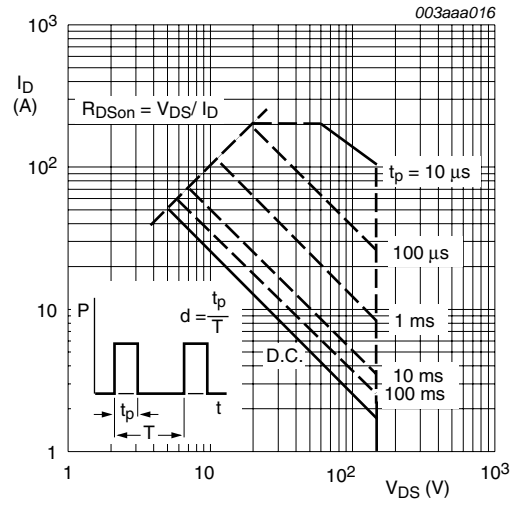
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	150	V
$V_{DGR}$	drain-gate voltage	$T_j \leq 175\text{ °C}$ ; $T_j \geq 25\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	150	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a> and <a href="#">2</a>	-	36	A
		$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> and <a href="#">2</a>	-	50	A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	200	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	250	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	50	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	200	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 47\text{ A}$ ; $V_{sup} \leq 50\text{ V}$ ; unclamped; $t_p = 0.1\text{ ms}$ ; $R_{GS} = 50\text{ }\Omega$ ; see <a href="#">Figure 4</a>	-	460	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 50\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped; see <a href="#">Figure 4</a>	-	50	A



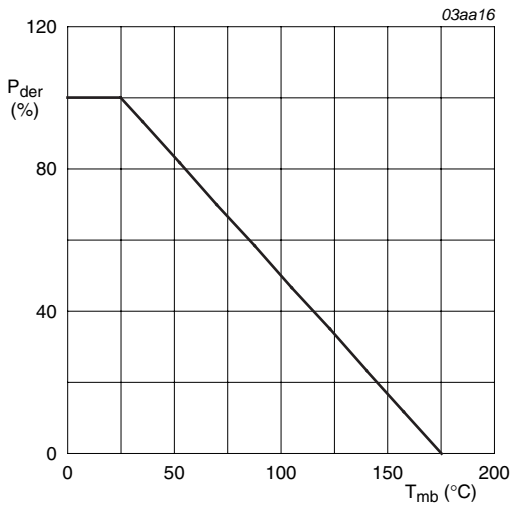
$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



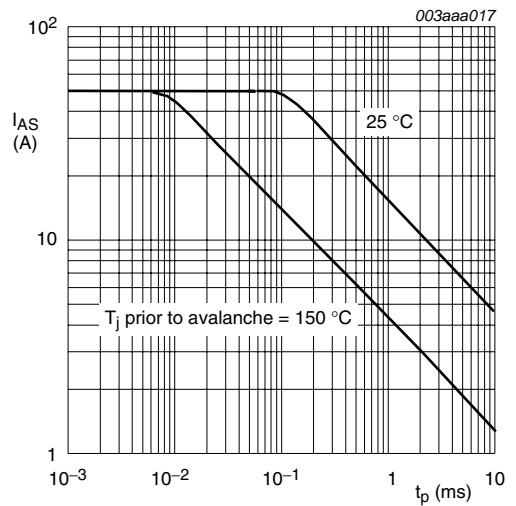
$T_{mb} = 25^\circ C; I_{DM}$  is single pulse

Fig 2. Safe operating area; continuous and peak drain currents as a function of drain-source volt



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 3. Normalized total power dissipation as a function of mounting base temperature



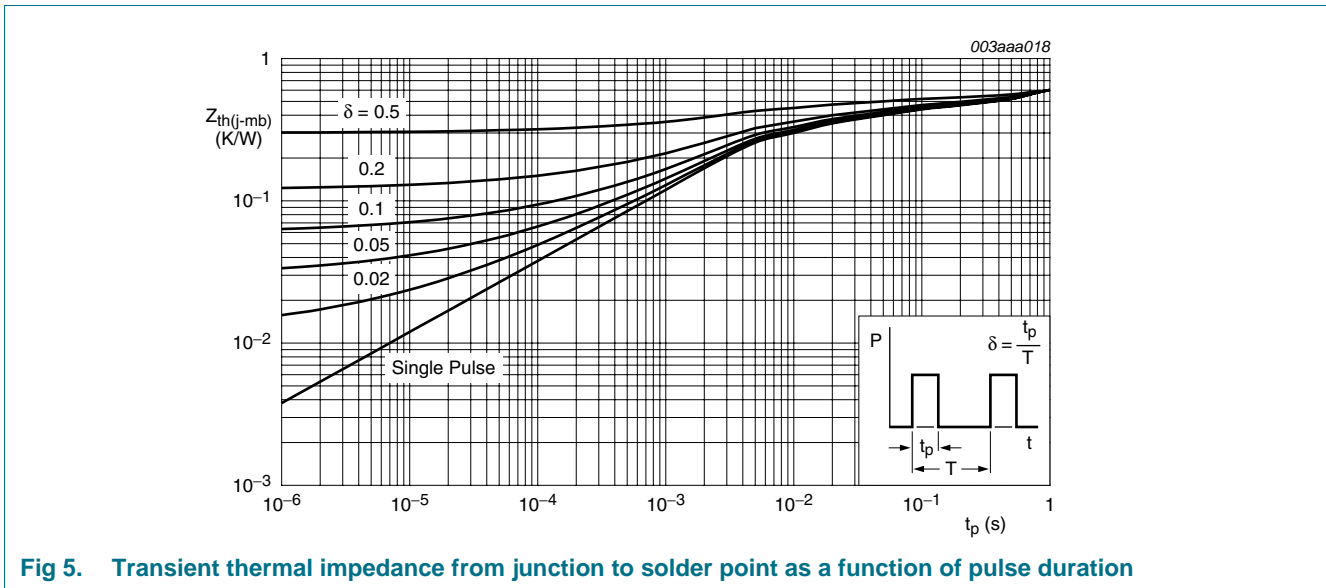
Unclamped inductive load;  $V_{DS} \leq 15V; R_{GS} = 50\Omega; V_{GS} = 10V$

Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 5</a>	-	0.6	-	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board; minimum footprint	-	-	50	K/W

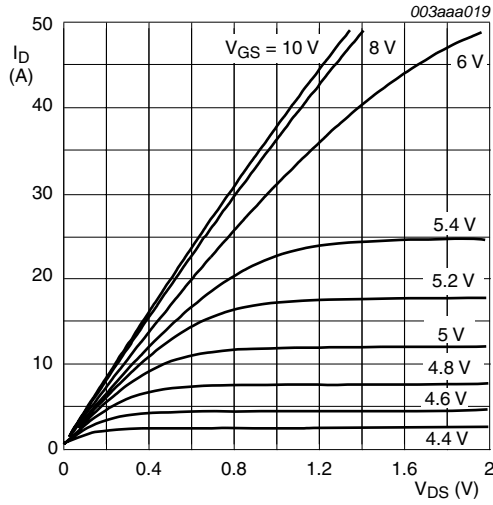


**Fig 5. Transient thermal impedance from junction to solder point as a function of pulse duration**

## 6. Characteristics

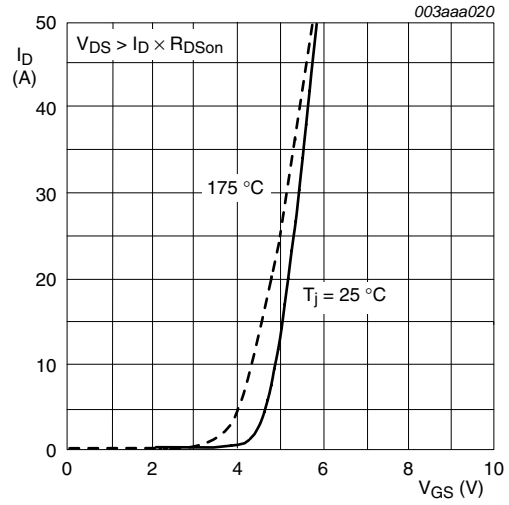
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	150	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 10</a>	1	-	-	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 10</a>	2	3	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 150 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	0.05	10	$\mu A$
		$V_{DS} = 150 V$ ; $V_{GS} = 0 V$ ; $T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V$ ; $I_D = 25 A$ ; $T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	-	98	m $\Omega$
		$V_{GS} = 10 V$ ; $I_D = 25 A$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	30	35	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 50 A$ ; $V_{DS} = 120 V$ ; $V_{GS} = 10 V$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 13</a>	-	79	-	nC
$Q_{GS}$	gate-source charge		-	17	-	nC
$Q_{GD}$	gate-drain charge		-	33	45	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 V$ ; $V_{GS} = 0 V$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 14</a>	-	4720	-	pF
$C_{oss}$	output capacitance	$V_{DS} = 25 V$ ; $V_{GS} = 0 V$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 13</a>	-	456	-	pF
$C_{rss}$	reverse transfer capacitance		-	208	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 75 V$ ; $R_L = 1.5 \Omega$ ; $V_{GS} = 10 V$ ; $R_{G(ext)} = 5.6 \Omega$ ; $T_j = 25 \text{ }^\circ C$	-	25	-	ns
$t_r$	rise time		-	138	-	ns
$t_{d(off)}$	turn-off delay time		-	79	-	ns
$t_f$	fall time		-	93	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 15</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 A$ ; $di_S/dt = -100 A/\mu s$ ; $V_{GS} = 0 V$ ; $V_{DS} = 30 V$ ; $T_j = 25 \text{ }^\circ C$	-	118	-	ns
$Q_r$	recovered charge		-	0.66	-	nC



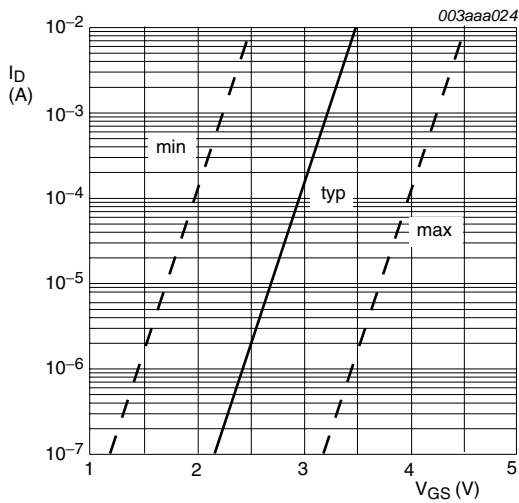
$T_j = 25^\circ\text{C}$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



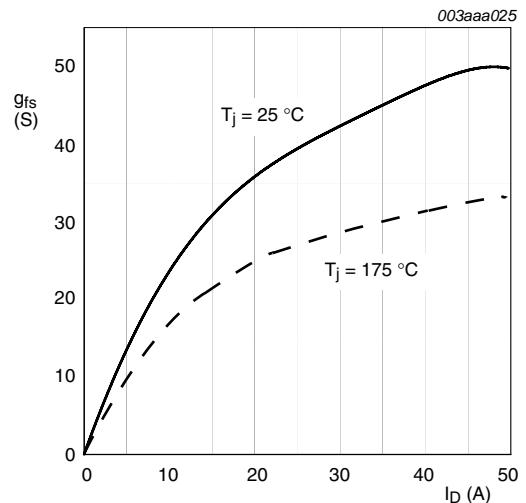
$T_j = 25^\circ\text{C}$  and  $175^\circ\text{C}; V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



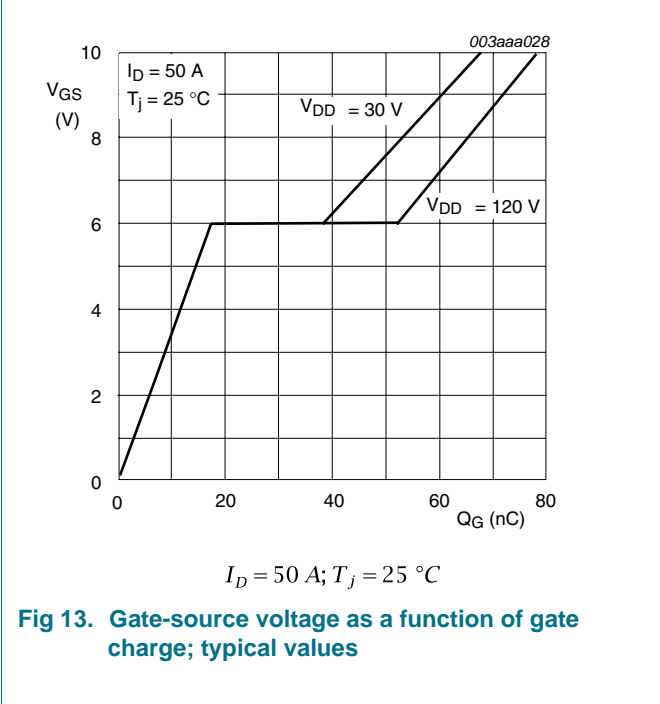
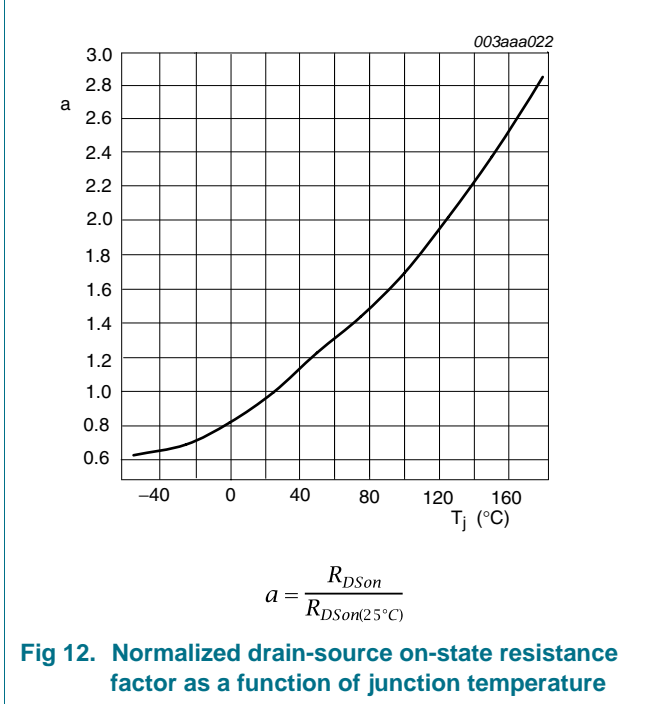
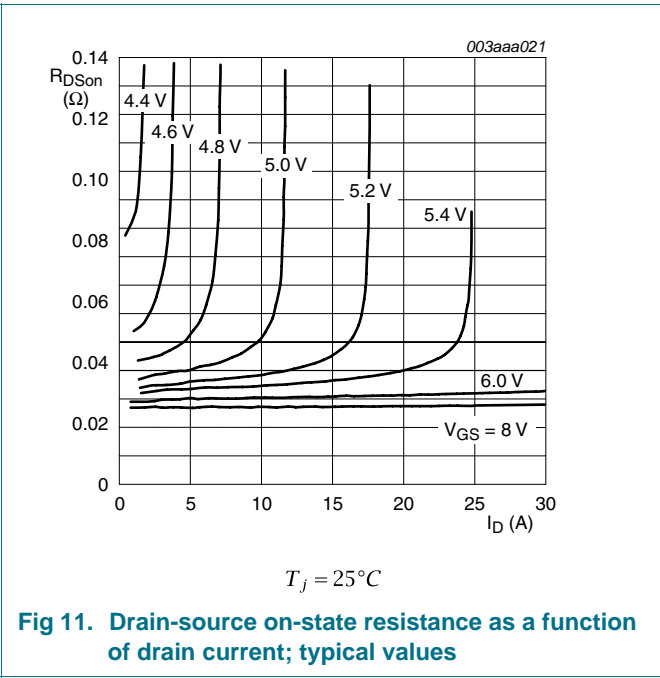
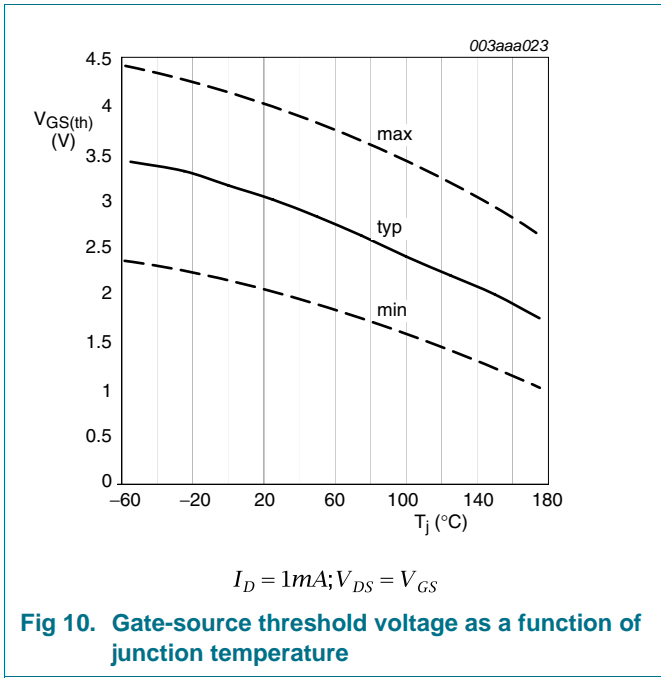
$T_j = 25^\circ\text{C}$

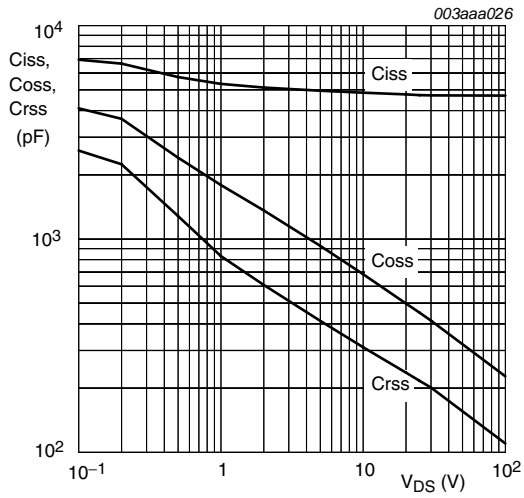
Fig 8. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25^\circ\text{C}$  and  $175^\circ\text{C}; V_{DS} > I_D \times R_{DSon}$

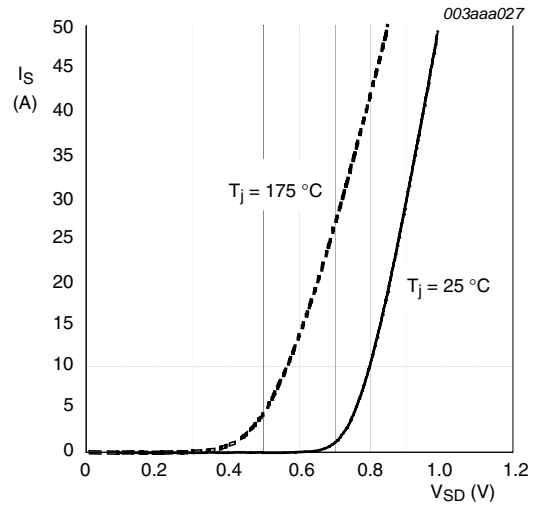
Fig 9. Forward transconductance as a function of drain current; typical values





$V_{GS} = 0V; f = 1MHz$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$T_j = 25^\circ C$  and  $175^\circ C; V_{GS} = 0V$

**Fig 15. Source current as a function of source-drain voltage; typical values**



7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

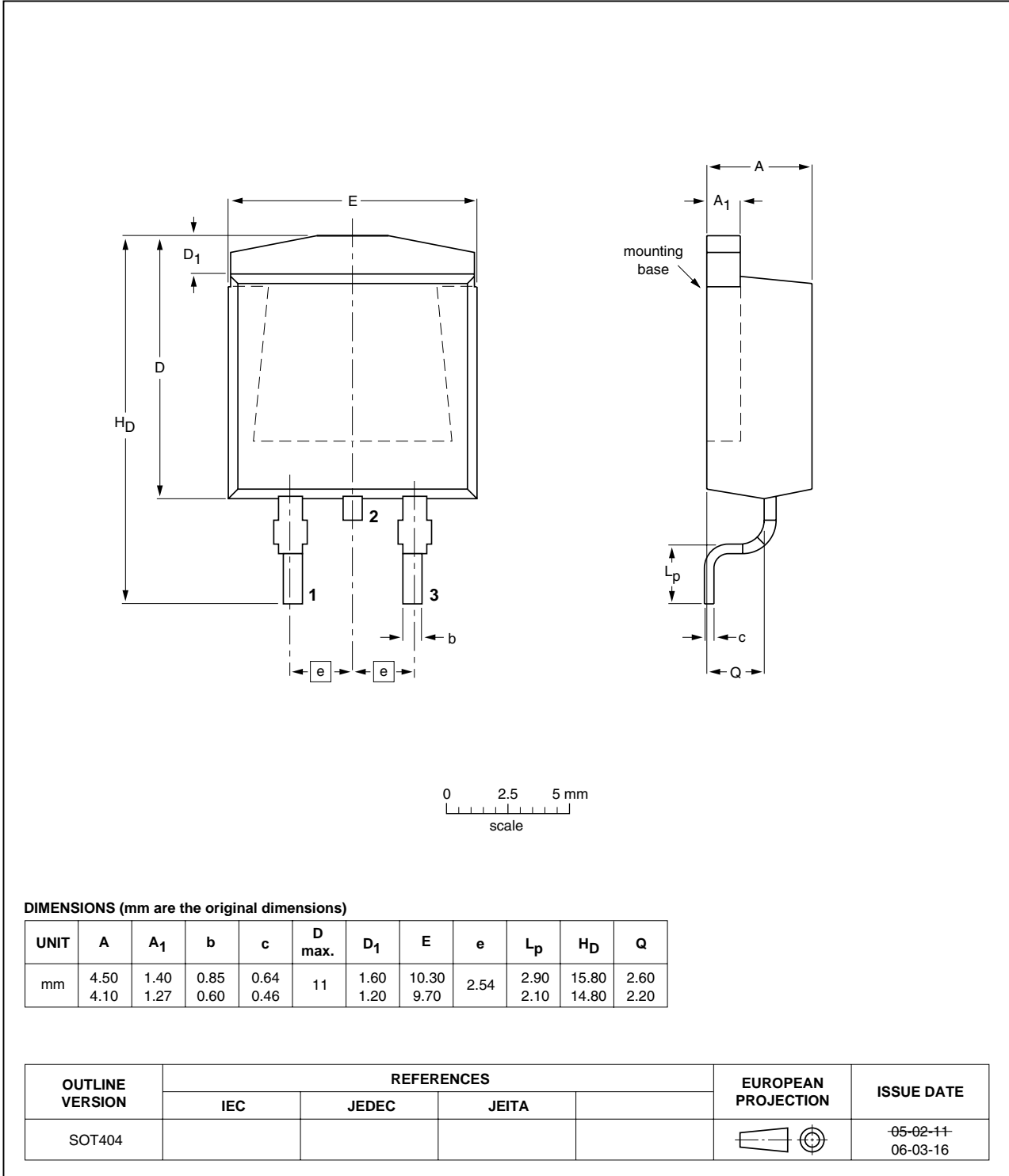


Fig 16. Package outline SOT404 (D2PAK)

## 8. Revision history

**Table 7. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN035-150B_4	20091117	Product data sheet	-	PSMN035-150_SERIES_HG_3
Modifications:		<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number PSMN035-150B separated from data sheet PSMN035-150_SERIES_HG_3.</li> </ul>		
PSMN035-150_SERIES_HG_3	20000328	Product specification	-	PSMN035-150_SERIES_2
PSMN035-150_SERIES_2	19990801	Product specification	-	PSMN035-150_SERIES_1
PSMN035-150_SERIES_1	19990201	Objective specification	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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