LP8728-Q1 Quad-Output Step-Down DC/DC Converter

1 Features

- LP8728-Q1 is an Automotive Grade Product that is AECQ-100 Grade 1 Qualified
- Four High Efficiency Step-Down DC/DC Converters:
  - 93% Peak Efficiency (V_{IN} = 5 V, V_{OUT} 3.3 V)
  - Max Output Current 1 A
  - Forced PWM Operation
  - Soft-Start Control
  - V_{OUT1} = 3.3 V
  - V_{OUT2} = 1.25 V
  - V_{OUT3} = 1.8 V or 2.65 V (pin selectable)
  - V_{OUT4} = 1.8 V
- Separate Enable Inputs for each Converter Control
- Separate Power Good Outputs for each Converter
- Output Overcurrent and Input Overvoltage Protection
- Overtemperature Protection
- Undervoltage Lockout (UVLO)

2 Applications

- FPGA, DSP Core Power
- Processor Power for Mobile Devices
- Peripheral I/O Power
- Automotive Safety Cameras
- Automotive Infotainment

3 Description

The LP8728-Q1 is a quad-output Power Management Unit (PMU), optimized for low-power FPGAs, microprocessors, and DSPs for automotive applications. This device integrates four highly efficient step-down DC/DC converters into one package. Each converter has high current capability and separate controls which allows flexibility to use the device in multiple applications. All the converters operate above the AM band with a fixed 3.2-MHz switching frequency. Each buck converter's high-side switch turnon time is phase shifted to minimize input current spikes.

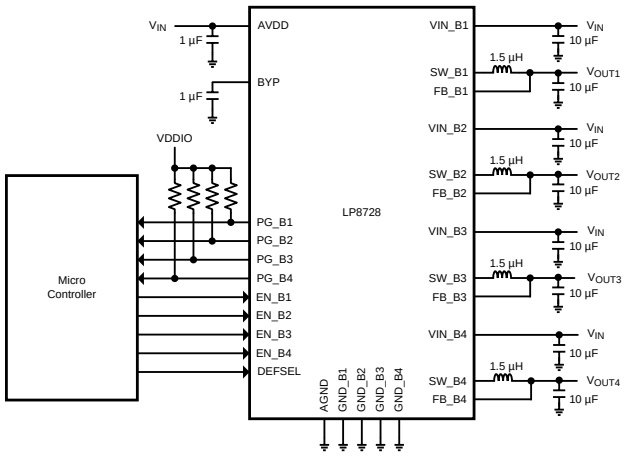
The protection features include output short-circuit protection, switch current limits, input overvoltage protection, input undervoltage lockout, and thermal shutdown functions. During start-up, the device controls the output slew rate to minimize output voltage overshoot and the input inrush current.

Device Information(1)

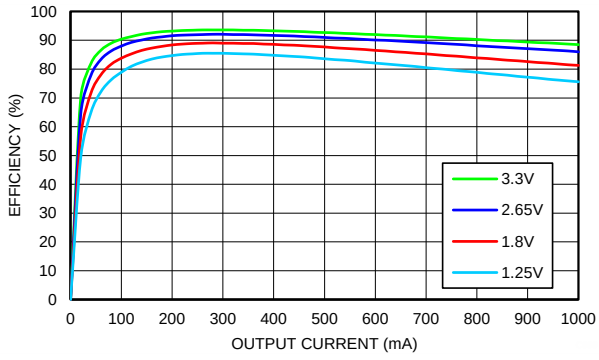
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP8728-Q1	WQFN (28)	5.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Efficiency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2014) to Revision B — **Page**

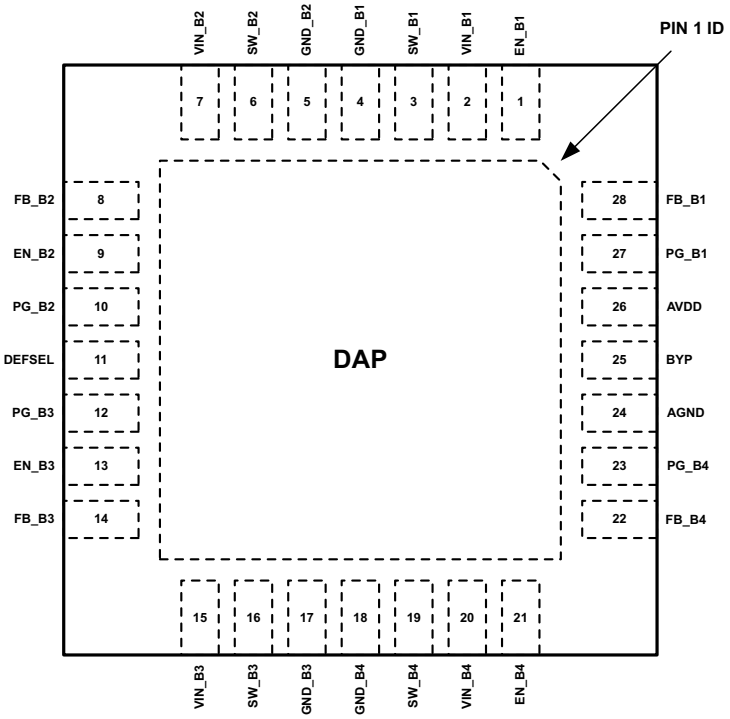
- Changed simplified schematic circuit drawing to correct pin placements for SW_B3 and SW_B4 ... 1
- Added *ESD Ratings* table to replace *Handling Ratings* ... 5
- Changed typical application circuit drawing to correct pin placements for SW_B3 and SW_B4 ... 15

Changes from Original (August 2013) to Revision A — **Page**

- Added *Device Information* and *Handling Ratings* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout* , *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; moved some curves to *Application Curves* section. ... 1

5 Pin Configuration and Functions

WQFN (RSG) Package
28 Pins
TOP VIEW



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	EN_B1	D/I	Enable Buck 1
2	VIN_B1	P	Positive power supply input for Buck 1
3	SW_B1	P	Switch node for Buck 1
4	GND_B1	G	Power ground for Buck 1
5	GND_B2	G	Power ground for Buck 2
6	SW_B2	P	Switch node for Buck 2
7	VIN_B2	P	Positive power supply input for Buck 2
8	FB_B2	A	Feedback pin for Buck 2. Referenced against AGND.
9	EN_B2	D/I	Enable Buck 2
10	PG_B2	D/O	Open-drain Power Good output for Buck 2
11	DEFSEL	D/I	Buck 3 output voltage selection pin
12	PG_B3	D/O	Open-drain Power Good output for Buck 3
13	EN_B3	D/I	Enable buck 3
14	FB_B3	A	Feedback pin for Buck 3. Referenced against AGND.
15	VIN_B3	P	Positive power supply input for Buck 3
16	SW_B3	P	Switch node for Buck 3
17	GND_B3	G	Power ground for Buck 3
18	GND_B4	G	Power ground for Buck 4
19	SW_B4	P	Switch node for Buck 4
20	VIN_B4	P	Positive power supply input for Buck 4

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
21	EN_B4	D/I	Enable Buck 4
22	FB_B4	A	Feedback pin for Buck 4. Referenced against AGND.
23	PG_B4	D/O	Open-drain Power Good output for Buck 4
24	AGND	G	Analog ground
25	BYP	A	Internal 1.8-V supply voltage capacitor pin. A ceramic low ESR 1-µF capacitor should be connected from this pin to AGND. The BYP voltage is generated internally, do not supply or load this pin externally.
26	AVDD	P	Analog positive power supply pin (VIN level)
27	PG_B1	D/O	Open-drain Power Good output for Buck 1
28	FB_B1	A	Feedback pin for Buck 1. Referenced against AGND.
DAP	Die Attachment Pad		Exposed die attachment pad should to be connected to GND plane with thermal vias to improve the thermal performance of the system.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{IN}	Voltage on power pins (AVDD, VIN_Bx)	–0.3	6	V
V_{FB}	Voltage on feedback pins (FB_Bx)	–0.3	6	
V_{SW}	Voltage on buck converter switch pins (SW_Bx)	(GND_Bx – 0.2 V) to (VIN_Bx + 0.2 V) with 6 V max		
V_{DIG}	Voltage on digital pins (PG_Bx, EN_Bx, DEFSEL)	(AGND – 0.2V) to (AVDD + 0.2 V) with 6 V max		
V_{BYP}	Voltage on BYP pin	–0.3	2	
$T_{J(MAX)}$	Maximum operating junction temperature (2)		150	°C
	Maximum lead temperature (Soldering)	See (3)		
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).
(3) For detailed soldering specifications and information, please refer to Texas Instruments Application Note *Leadless Leadframe Package (LLP)* SNOA401.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage on AVDD, VIN_B1, VIN_B2, VIN_B3 and VIN_B4 Pins	4.5	5	5.5	V
T_A	Operating ambient temperature (2)	–40		125	°C
C_{OUT}	Effective output capacitance during operation. Min value over T_A –40°C to 125°C.	5	10	12	µF
C_{IN}	Effective input capacitance during operation. 4.5 V ≤ V_{IN_Bx} ≤ 5.5 V. Min value over T_A –40°C to 125°C.	2.5	10		
L	Effective inductance during operation Min value over T_A –40°C to 125°C.	0.47	1.5	2	

(1) All voltage values are with respect to network ground terminal.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_{D(max)})$

6.4 Thermal Information

THERMAL METRIC (1)		LP8728-Q1 WQFN (RSG) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	36.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Calculated using 4-layer standard JEDEC thermal test board with 5 thermal vias between the die attach pad in the first copper layer and second copper layer.

6.5 Electrical Characteristics[1][2]

Unless otherwise noted, V_{IN} = 5 V, typical values apply for T_A = 25°C, and minimum/maximum limits apply over junction temperature range, T_J = –40°C to 125°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SHDN}	Shutdown supply current into power connections	EN_Bx = 0 V		1	6	µA
I_{OP}	Operating current	All buck-converters active, I_{OUT} = 0 mA		20		mA
LOGIC INPUTS (EN_Bx, DEFSEL)						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.6			V
R_{PD_DI}	EN_Bx and DEFSEL internal pull-down resistance		300	520	820	kΩ
T_{H_MIN}	Minimum EN_Bx high time			1		ms
T_{L_MIN}	Minimum EN_Bx low time			10		µs
LOGIC OUTPUTS (PG_Bx)						
V_{OL}	Output low level	I_{SINK} = 3 mA			0.4	V
R_{PU}	Recommended pull-up resistor			10		kΩ
BUCK CONVERTERS						
V_{OUT1}	Output voltage for Buck 1	Fixed voltage		3.3		V
V_{OUT2}	Output voltage for Buck 2	Fixed voltage		1.25		V
V_{OUT3}	Output voltage for Buck 3	DEFSEL = 1		2.65		V
		DEFSEL = 0		1.8		
V_{OUT4}	Output voltage for Buck 4	Fixed voltage		1.8		V
V_{FB_Bx}	Output voltage accuracy		–3%		3%	
ΔV_{OUT}	Line regulation	4.5 V ≤ V_{IN_Bx} ≤ 5.5 V I_{LOAD} = 10 mA		3		mV
	Load regulation	V_{IN} = 5 V 100 mA ≤ I_{LOAD} ≤ 900 mA		3		mV
I_{OUT}	Output current	DC load T_A = 25°C.			1000	mA
F_{SW}	Switching frequency		3.03	3.2	3.37	MHz
GBW	Gain bandwidth			300		kHz
I_{LIMITP}	High side switch current limit		1200	1500	1800	mA
I_{LIMITN}	Low side switch current limit	Reverse current		500		mA
R_{DSONP}	Pin-pin resistance for PFET	I_{OUT} = 200 mA		210	300	mΩ
R_{DSONN}	Pin-pin resistance for NFET	I_{OUT} = 200 mA		140	240	mΩ
I_{LK_SW}	Switch pin leakage current	V_{OUT} = 1.8V			1	µA
R_{PD_FB}	Pull-down resistor from FB_Bx pin to GND	Only active when converter disabled. All limits apply for T_A = 25°C.	40	70	100	Ω
K_{RAMP}	Slew rate control	DEFSEL from 0 to 1		10		mV/µs
T_{START}	Start-up time	Time from first EN_Bx high to start of switching		420		µs
K_{START}	Soft-start VOUT slew rate			18		mV/µs
VOLTAGE MONITORING						
V_{PG}	Power good threshold voltage	Power good threshold for voltage rising	93.5%	96%	98%	
		Power good threshold for voltage falling	91%	93%	95%	
V_{OVP}	Input overvoltage protection trigger point	Voltage monitored on AVDD Pin, voltage rising	5.5	5.7	5.9	V
		Hysteresis		80		mV

(1) All voltage values are with respect to network ground terminal.
(2) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis. Typical (Typ) numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = 5 V and T_J = 25°C.

Electrical Characteristics[1][2] (continued)

Unless otherwise noted, V_{IN} = 5 V, typical values apply for T_A = 25°C, and minimum/maximum limits apply over junction temperature range, T_J = –40°C to 125°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	Input undervoltage lockout (UVLO) turn-on threshold.	Voltage monitored on AVDD Pin, voltage falling		4.35		V
		Hysteresis		80		mV
THERMAL SHUTDOWN AND MONITORING						
TSD	Thermal shutdown	Threshold, temperature rising		150		°C
		Hysteresis		20		

6.6 System Characteristics[1][2][3]

Typical values apply for T_A = 25°C. Unless otherwise noted, V_{IN} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{OUT}	Load transient response	I_{OUT} 10% max load → 90% max load, 1-µs load step		70		mV
		I_{OUT} 90% max load → 10% max load, 1-µs load step		70		mV
	Line transient response	V_{IN_Bx} stepping 4.5V ↔ 5.5V tr = tf = 10 µs, I_{OUT} = 400 mA		20		mV
V_{RIPPLE}	Output voltage ripple	C_{OUT} ESR = 10 mΩ, I_{OUT} = 200 mA		10		mV_{PP}
η	Efficiency	V_{OUT} = 3.3 V, I_{OUT} = 300 mA		94%		
		V_{OUT} = 2.65 V, I_{OUT} = 300 mA		92%		
		V_{OUT} = 1.8 V, I_{OUT} = 300 mA		89%		
		V_{OUT} = 1.2 V, I_{OUT} = 300 mA		85%		

(1) All voltage values are with respect to network ground terminal.
(2) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis. Typical (Typ) numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = 5 V and T_J = 25°C.
(3) System Characteristics are highly dependent on external components and PCB layout. System Characteristics are verified using inductor type: TOKO MDT2520-CN1R5M, input and output capacitor type: MuRata GRM21BR71A106KE51L.

6.7 Typical Characteristics

Unless otherwise noted, V_{IN} = 5 V, T_A = 25°C

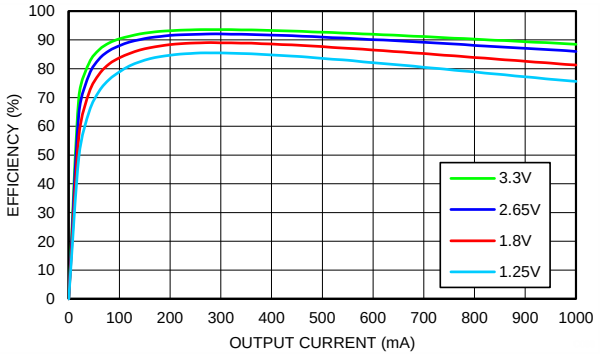


Figure 1. Efficiency vs Output Current

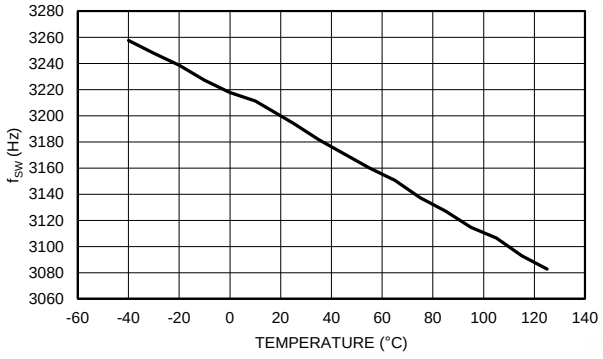


Figure 2. Switching Frequency vs Temperature

Typical Characteristics (continued)

Unless otherwise noted, V_{IN} = 5 V, T_A = 25°C

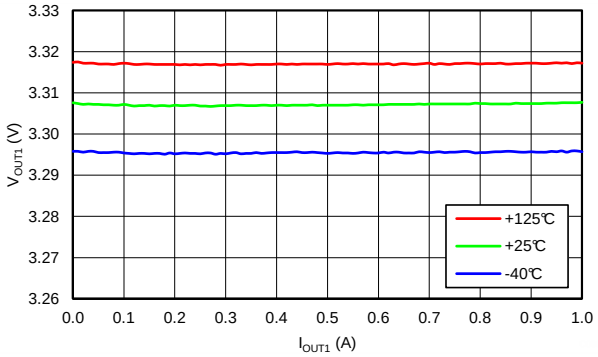


Figure 3. Buck1 Load Regulation

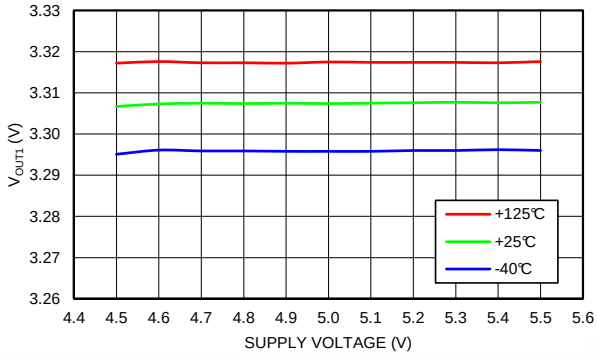


Figure 4. Buck1 Line Regulation

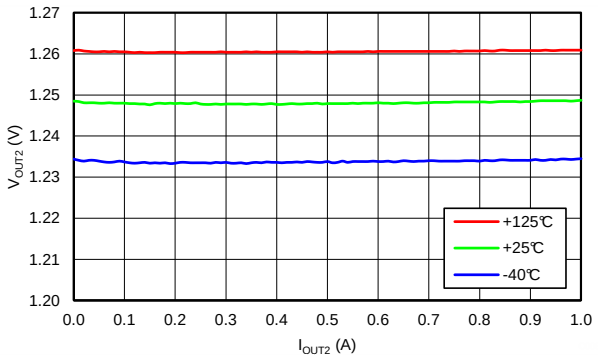


Figure 5. Buck2 Load Regulation with 1.25-V Setting

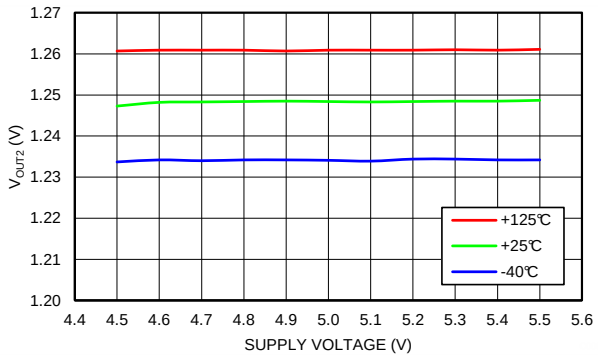


Figure 6. Buck2 Line Regulation with 1.25-V Setting

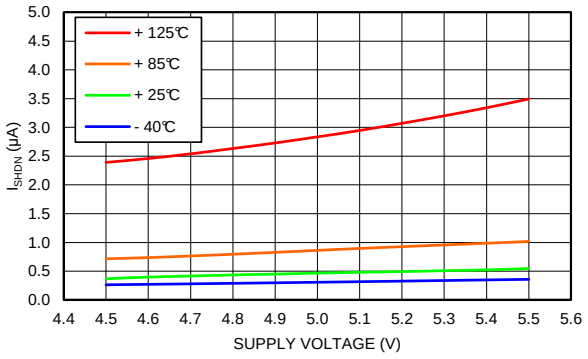


Figure 7. Shutdown Current Consumption

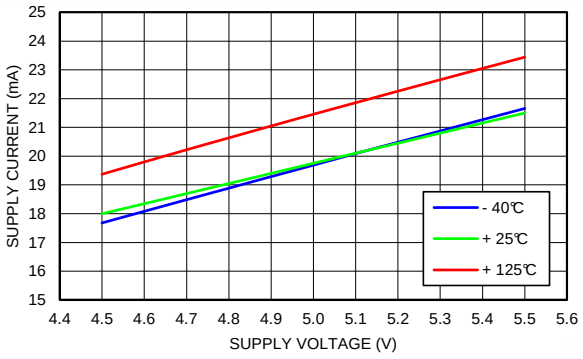


Figure 8. Active Mode Current Consumption (All Bucks Active)

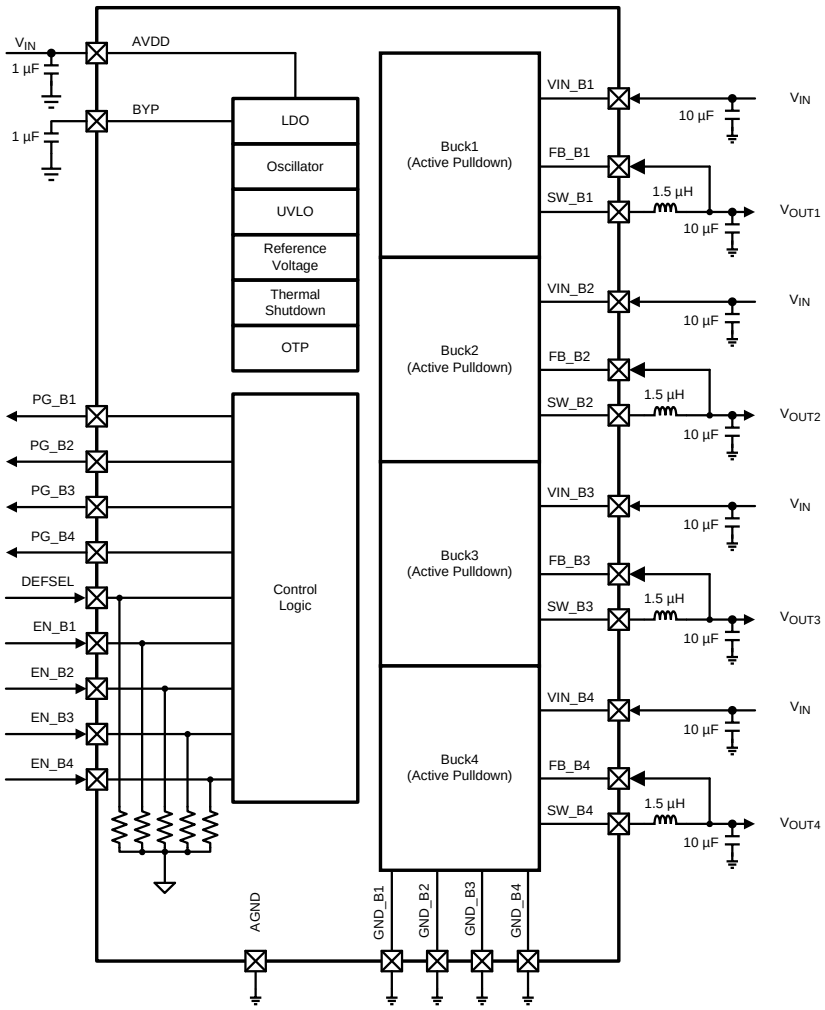
7 Detailed Description

7.1 Overview

The LP8728 has four integrated high-efficiency buck converters. Each buck converter has individual enable input and power good output pins. When the first enable pin is pulled high there is a 420-µs start-up delay when the device wakes up from shutdown mode and all internal reference blocks are started up. Once reference blocks have settled, the corresponding buck converter turns on. Buck cores utilize the soft-start feature to limit the inrush current during start-up. Once a buck output reaches 96% (typ.) of the desired output voltage, the power-good pin is pulled high (see Figure 9). When at least one buck core is active, the remaining buck converters will start up without any start-up delay.

If the output voltage drops below 93% (typ.) of desired voltage due to, for example, an overload condition, the corresponding power-good pin is pulled low. The power-good signal is always held low for at least 50 ms. When the enable pin is pulled low, the corresponding buck converter's power good signals are set low, and the buck converter is instantly shut down. An output capacitor is then discharged through an internal 70-Ω (typ.) pull-down resistor. The pull-down resistor is connected between buck feedback pin and ground and is only active when the enable pin is set low. When all enable signals are pulled low, the LP8728-Q1 enters a low-current shutdown mode.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Buck Information

The buck converters are operated in forced PWM mode. Even with light load a minimum switching pulse is generated with every switching cycle. Each buck converter's high-side switch turn-on time is phase shifted to minimize the input current ripple (see Figure 20).

7.3.1.1 Features

The following features are supported for all converters:

- Synchronous rectification
- Current mode feedback loop with PI compensator
- Forced PWM operation
- Soft start
- Power-good output
- Overvoltage comparator

In addition to the aforementioned features, buck3 output voltage can be selected with the DEFSEL pin. If the DEFSEL pin is pulled low, V_{OUT3} is set to 1.8 V. If DEFSEL is pulled high, V_{OUT3} is set to 2.65 V.

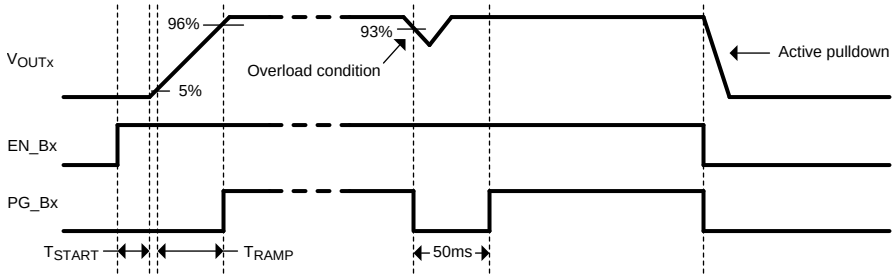


Figure 9. Buck Converter Start-up And Shutdown

7.3.2 Thermal Shutdown (TSD)

Thermal shutdown function shuts down all buck regulators if the device's junction temperature T_J rises above 150°C (typ.). All power-good signals are pulled low 5 ms before buck regulators are shut down. Once T_J falls below 130°C (typical), the LP8728 will automatically start up the buck regulators. There is a 2-second safety delay included in the restart function. Buck regulators are not restarted until 2 seconds have elapsed after T_J falls below 130°C (typical). To minimize the inrush current during restarting, regulators are started in a buck1 → buck2 → buck3 → buck4 sequence. A 500-µs delay is included between each buck start-up.

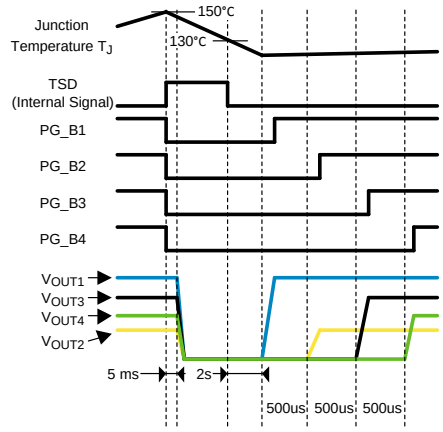


Figure 10. TSD Timing Diagram

Feature Description (continued)

7.3.3 Undervoltage Lockout (UVLO)

Undervoltage lockout pulls the PG_Bx pins low if the input voltage drops below 4.35 V (typical) (Figure 11). PG_Bx pins are always held low for at least 50 ms. Once an undervoltage condition has lasted for 5 ms, all buck converters are shut down. Buck converters are restarted once the input voltage rises above UVLO level.

If an undervoltage condition has lasted more than 5 ms, but less than 50 ms, PG_Bx pins are released high once 50 ms has elapsed and corresponding output voltage has settled. If an overvoltage condition has lasted more than 50 ms, power-good signals are released high once corresponding output voltage has settled. If an under-voltage condition lasts less than 5 ms, the buck converters are not shut down. Even in this case PG_Bx pins are held low for 50 ms.

Regulators are always restarted in a buck1 → buck2 → buck3 → buck4 sequence. A 500-µs delay is included between each buck start-up.

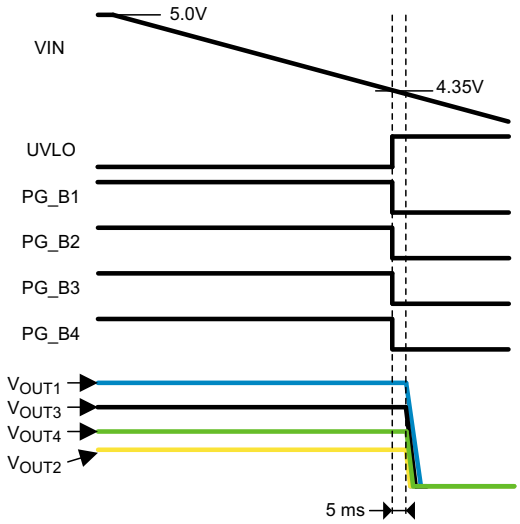


Figure 11. UVLO Operation

7.3.4 Overvoltage Protection (OVP)

Overvoltage protection protects the device in case of an overvoltage condition. If input voltage exceeds 5.7 V (typical), all PG_Bx pins are pulled low. PG_Bx pins are always held low for at least 50 ms. Once the PG_Bx pins are pulled low, the system has 5 ms time to power down. After over-voltage condition has lasted for 5 ms, all buck converters are shut down. Buck converters are restarted once input voltage falls below 5.62 V (typical). Regulators are started in a buck1 → buck2 → buck3 → buck4 sequence. A 500-µs delay is included between each buck start-up.

If an overvoltage condition lasted more than 5 ms, but less than 50 ms, the PG_Bx pins are released high once 50 ms has elapsed and corresponding output voltage has settled (Figure 12).

Feature Description (continued)

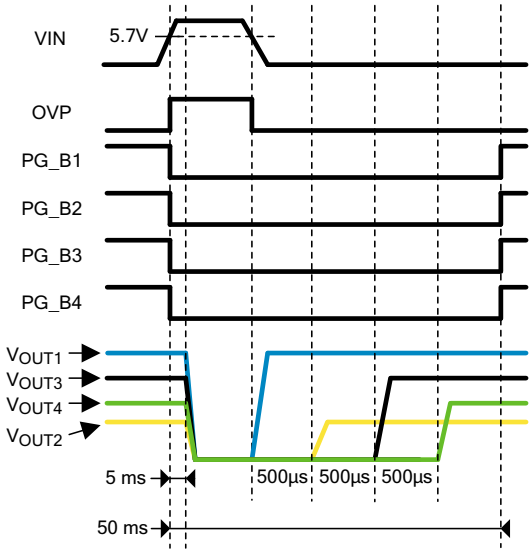


Figure 12. OVP Duration Less Than 50 ms

If an overvoltage condition has lasted more than 50 ms, power-good signals are released high once corresponding output voltage has settled. Regulators are started in a buck1 → buck2 → buck3 → buck4 sequence. A 500-µs delay is included between each buck start-up (Figure 13). If an overvoltage condition has lasted less than 5 ms, buck converters are not shut down. Even in this case the PG_Bx pins are held low for 50 ms.

NOTE

Since regulators are allowed to operate for 5 ms during overvoltage condition it is the system designer's responsibility to verify that input voltage doesn't exceed limits stated in *Absolute Maximum Ratings*. Exceeding these limits may cause permanent damage to the device.

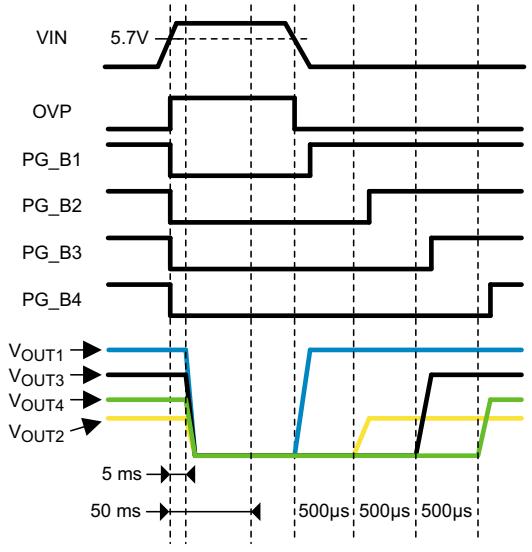


Figure 13. OVP Duration More Than 50 ms

7.4 Device Functional Modes

7.4.1 Shutdown Mode

When all EN_Bx inputs are low device is in Shutdown mode. This is a low-power mode when all buck-regulators and all internal blocks are disabled.

7.4.2 Active Mode

When the first enable pin is pulled high there is a 420-µs start-up delay when the device wakes up from Shutdown Mode and all internal reference blocks are started up. Once reference blocks have settled, the corresponding buck converter turns on. Buck cores utilize the soft-start feature to limit the inrush current during start-up. Once a buck output reaches 96% (typ.) of the desired output voltage, the power-good pin is pulled high. When at least one buck converter is active device is in Active Mode. When device is in Active Mode, the remaining buck converters will start up without any start-up delay when EN_Bx pin is pulled high. When EN_Bx pin is set low the corresponding buck converter will shut down. When all EN_Bx pins are set low LP8728 shuts down all internal reference blocks and enters Shutdown Mode.

If output voltage of a buck regulator falls below 93% (typ.) of desired voltage due to, for example, an overload condition, the corresponding power good pin is pulled low. Once output voltage rises back above 96% (typ.) of desired voltage power good pin is set back high. Power good signal is held low for at least 50 ms.

If UVLO, OVP or TSD fault occurs during normal operation, all power good pins are pulled low. Once fault condition has lasted for 5 ms all buck converters are shut down. Once fault condition has ended buck converters are restarted in a buck1 → buck2 → buck3 → buck4 power-up sequence. A 500-µs delay is included between each buck start-up. In case of TSD fault there is a 2 second safety delay before power up sequence.

Device Functional Modes (continued)

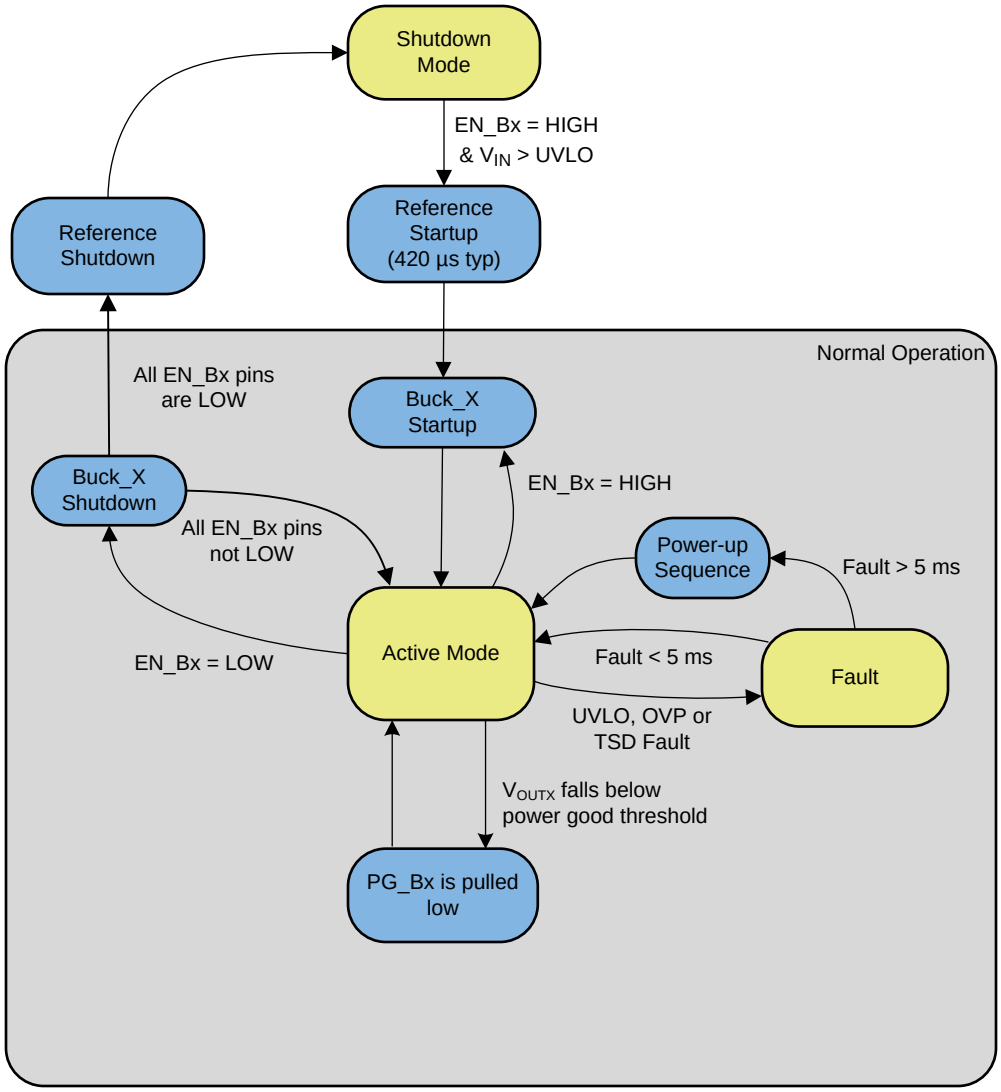


Figure 14. Device Functional Modes

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP8728-Q1 is a quad-output Power Management Unit (PMU), optimized for low-power FPGAs, microprocessors, and DSPs.

8.2 Typical Application

Figure 15 shows an example of typical application. Micro controller controls each buck converter with separated enable signal. All four power good signals are connected to micro controller with a separated pull-up resistors. If only one master power good signal is required all power good signals can be connected in parallel and pulled up with a single pull-up resistor. V_{OUT3} voltage can be selected with DEFSEL input. If V_{OUT3} control is not required during operation output voltage can be selected by connecting DEFSEL pin to VDDIO or to GND.

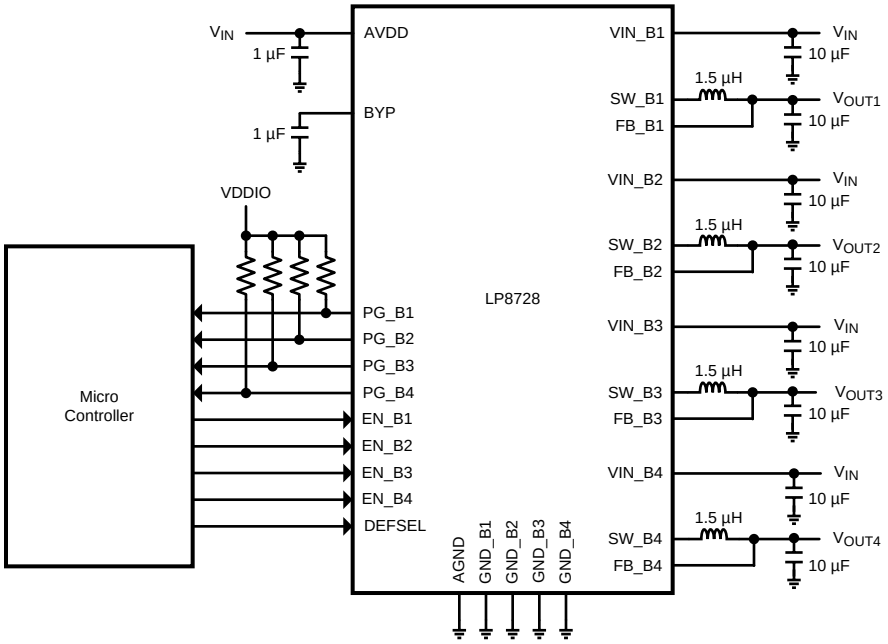


Figure 15. LP8728-Q1 Typical Application

Typical Application (continued)

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range (V_{IN})	4.5 V to 5.5 V
Buck converter output current	1 A maximum
Buck converter input capacitance	10 µF, 6.3 V
Buck converter output capacitance	10 µF, 6.3 V
Buck converter inductor	1.5 µH, 1.5 A
AVDD pin bypass capacitor	1 µF, 6.3 V
BYP pin bypass capacitor	1 µF, 6.3 V

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor

The four converters operate with 1.5-µH inductors. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductor directly influences the efficiency of the converter. Therefore, an inductor with the lowest possible DC resistance should be selected for the highest efficiency. The inductor should have a saturation current rating equal or higher than the high-side switch current limit (1500 mA). To minimize radiated noise shielded inductor should be used. The inductor should be connected to the SW pin as close to the IC as possible.

8.2.2.2 Input and Output Capacitors

Because buck converters have a discontinuous input current, a low ESR input capacitor is required for best input-voltage filtering and minimizing interference with other circuits caused by high input voltage spikes. Each DC-DC converter requires a 10-µF ceramic input capacitor on its input pin VIN_Bx. The input capacitor capacitance can be increased without any limit for better input voltage filtering. A small 100-nF capacitor can be used in parallel to minimize high-frequency interferences. Input capacitors should be placed as close to VIN_Bx pins as possible. Routing from input capacitor to VIN_Bx pins should be done on top layer without using any vias.

An output capacitor with a typical value of 10 µF is recommended for each converter. Ceramic capacitors with low ESR value have lowest output voltage ripple and are recommended.

Some ceramic capacitors, especially those in small packages, exhibit a strong capacitance reduction with the increased applied DC voltage (DC bias effect). The capacitance value can fall below half of the nominal capacitance. This needs to be taken into consideration and, if necessary, use a capacitor with higher value or higher voltage rating.

Table 1. Recommended External Components

COMPONENT	DESCRIPTION	VALUE	TYPE	EXAMPLE
$C_{IN\_B1,2,3,4}$	Buck regulator input capacitor	10 µF	Ceramic, 10 V, X7R	MuRata, GRM21BR71A106KE51L
$C_{OUT\_B1,2,3,4}$	Buck regulator output capacitor	10 µF	Ceramic, 10 V, X7R	MuRata, GRM21BR71A106KE51L
C_{AVDD}	AVDD pin input capacitor	1 µF	Ceramic, 10 V, X7R	MuRata, GRM188R71A105KA61D
C_{BYP}	Internal LDO bypass capacitor	1 µF	Ceramic, 10 V, X7R	MuRata, GRM188R71A105KA61D
$L_{SW1,2,3\ 4}$	Buck regulator inductor	1.5 µH	I_{SAT} >1.5 A, DCR < 100 mΩ	TOKO MDT2520-CN1R5M

8.2.3 Application Curves

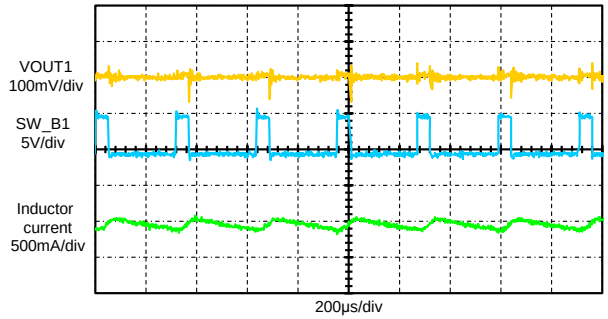


Figure 16. Short-Circuit Waveforms

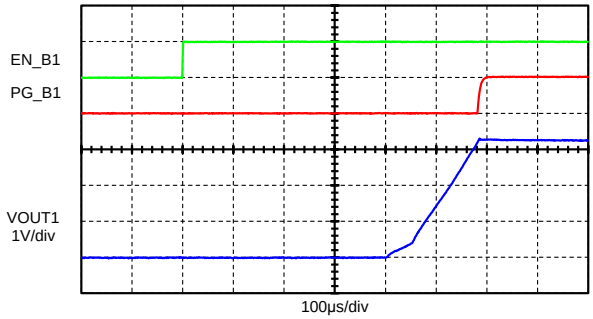
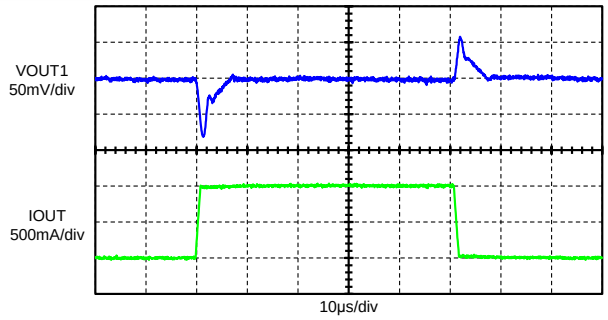
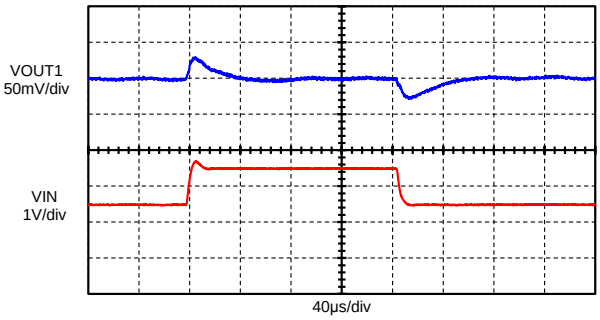


Figure 17. Start-up Delay



I_{OUT} from 0 mA to 1A

Figure 18. Load Transient Response



V_{IN} from 4.5 V To 5.5 V

Figure 19. Line Transient Response

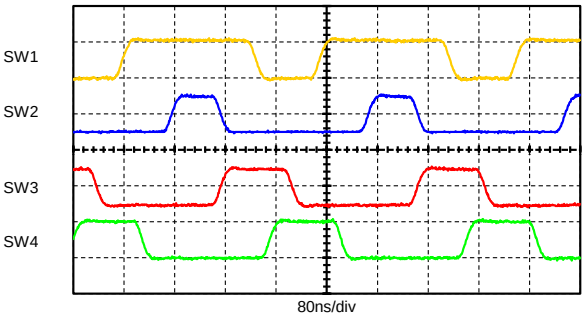


Figure 20. Switch Turnon Phase Shifting

9 Power Supply Recommendations

The LP8728-Q1 is designed to operate from an input voltage supply range between 4.5 V and 5.5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LP8728-Q1 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

- AVDD and BYP pins must by bypassed to ground. 1-µF ceramic capacitor is recommended. Place the capacitor close to AVDD, BYP and AGND pins.
- AGND pin must bo be tied to the PCB ground plane. Use multiple vias to minimize the inductance.
- AVDD pin must be connected to PCB VIN plane. Use multiple vias to minimize the inductance.
- Place the buck converter input capacitors as close to buck input voltage and buck ground pins as possible.
- Place the buck converter output capacitors and inductors so that the buck converter switching loops can be routed on top layer. Try to minimize the area of the switching loops.
- Keep the trace width from switch pin to inductor wide enough to withstand the switching currents. Avoid any excess copper on the switch pin to minimize switch pin capacitance.
- Connect the exposed thermal pad to ground plane with multiple thermal vias.
- Avoid routing digital signals directly under the switching loops to avoid interferences.

10.2 Layout Example

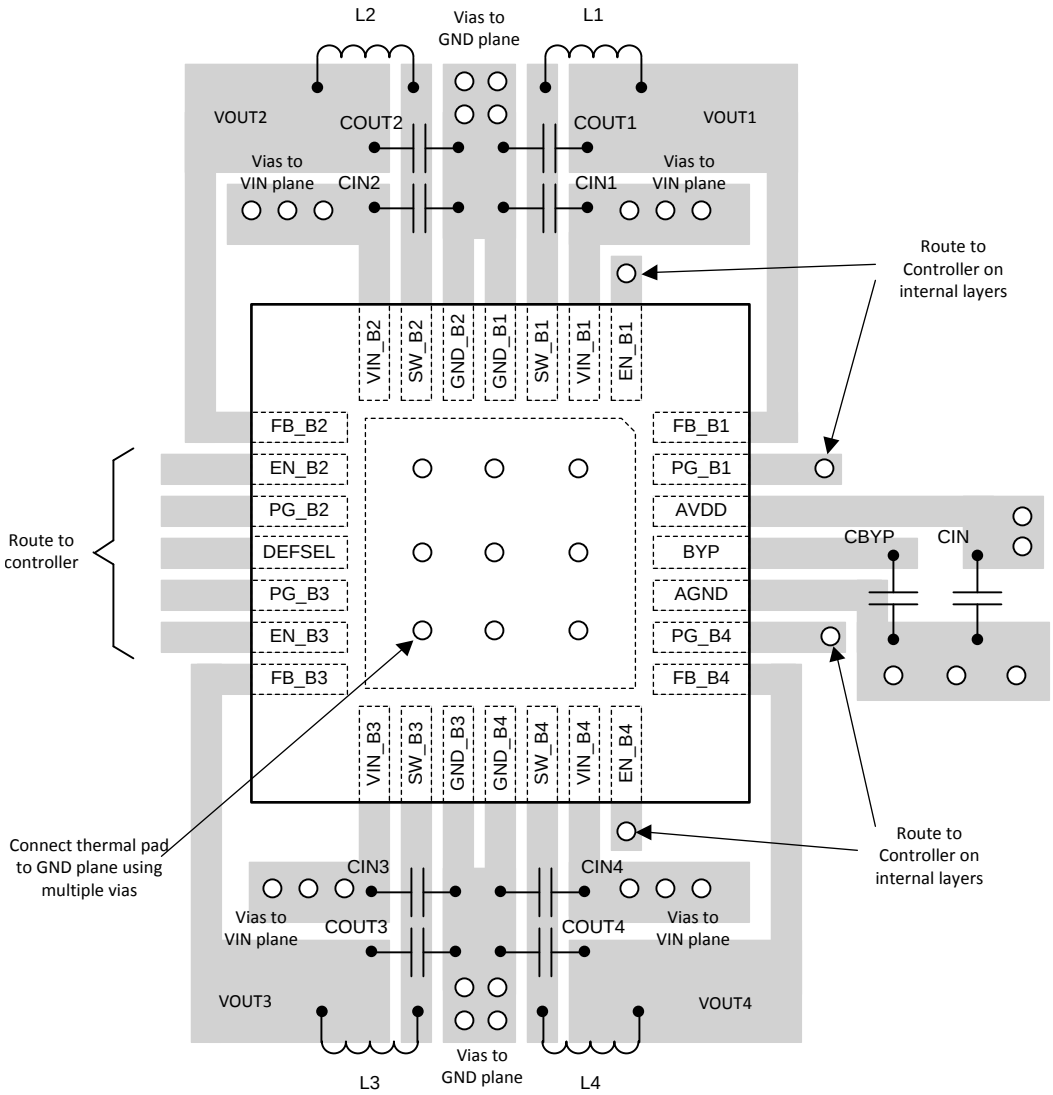


Figure 21. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Related Documentation

Texas Instruments Application Note 1187 *Leadless Leadframe Package (LLP)* (SNOA401).

See *Using the LP8728EVM Evaluation Module* (SNVU231) for more information about LP8728 evaluation module.

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8728QSQE-A/NOPB	ACTIVE	WQFN	RSG	28	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	8728Q-A	Samples
LP8728QSQX-A/NOPB	ACTIVE	WQFN	RSG	28	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	8728Q-A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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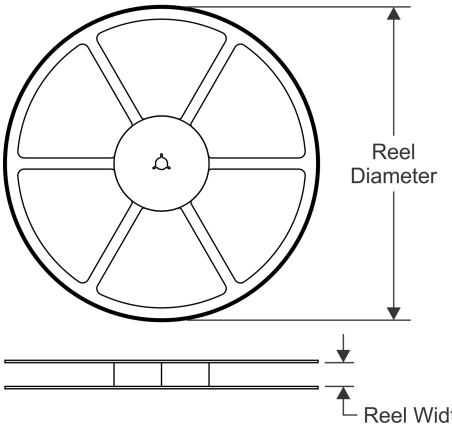
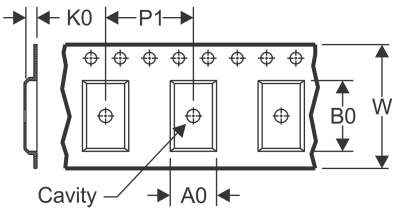
REEL DIMENSIONS

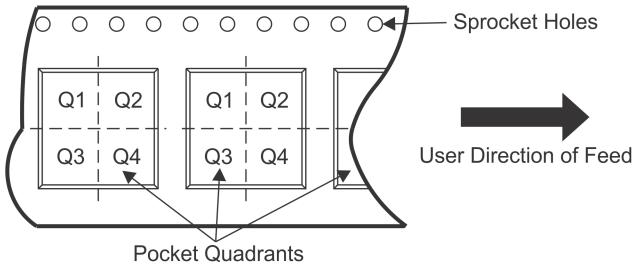


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

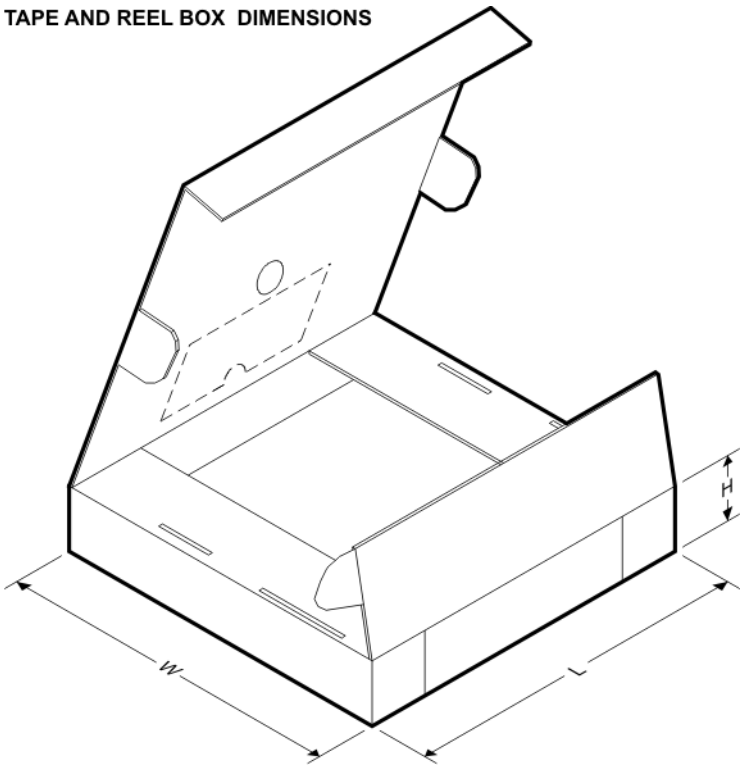
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8728QSQE-A/NOPB	WQFN	RSG	28	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LP8728QSQX-A/NOPB	WQFN	RSG	28	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8728QSQE-A/NOPB	WQFN	RSG	28	250	210.0	185.0	35.0
LP8728QSQX-A/NOPB	WQFN	RSG	28	4500	367.0	367.0	35.0

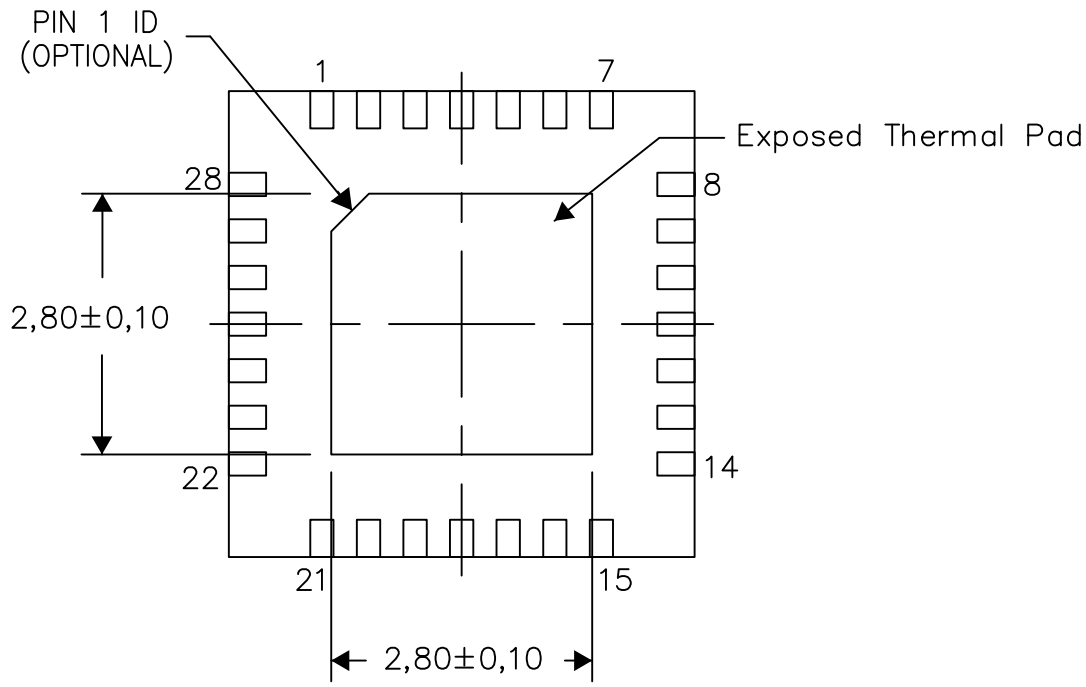
RSG (S–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4221534–3/A 05/14

NOTE: All linear dimensions are in millimeters

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