8Kx8 SoftStore nvSRAM

FEATURES

- **25, 35, 45, and 55 ns Read Access & R/W Cycle Times**
- **Unlimited Read/Write Endurance**
- **Pin compatible with Industry Standard SRAMs**
- **Software-initiated Non-Volatile *STORE***
- **Automatic *RECALL* to SRAM on Power Up**
- **Unlimited RECALL cycles**
- **1 Million *STORE* Cycles**
- **100-Year Non-volatile Data Retention**
- **Single 5V ± 10% Operation**
- **Commercial, Industrial, and Military Temperatures**
- **28-pin 330 mil SOIC (RoHS-Compatible)**
- **28-pin CDIP and LCC packages**

DESCRIPTION

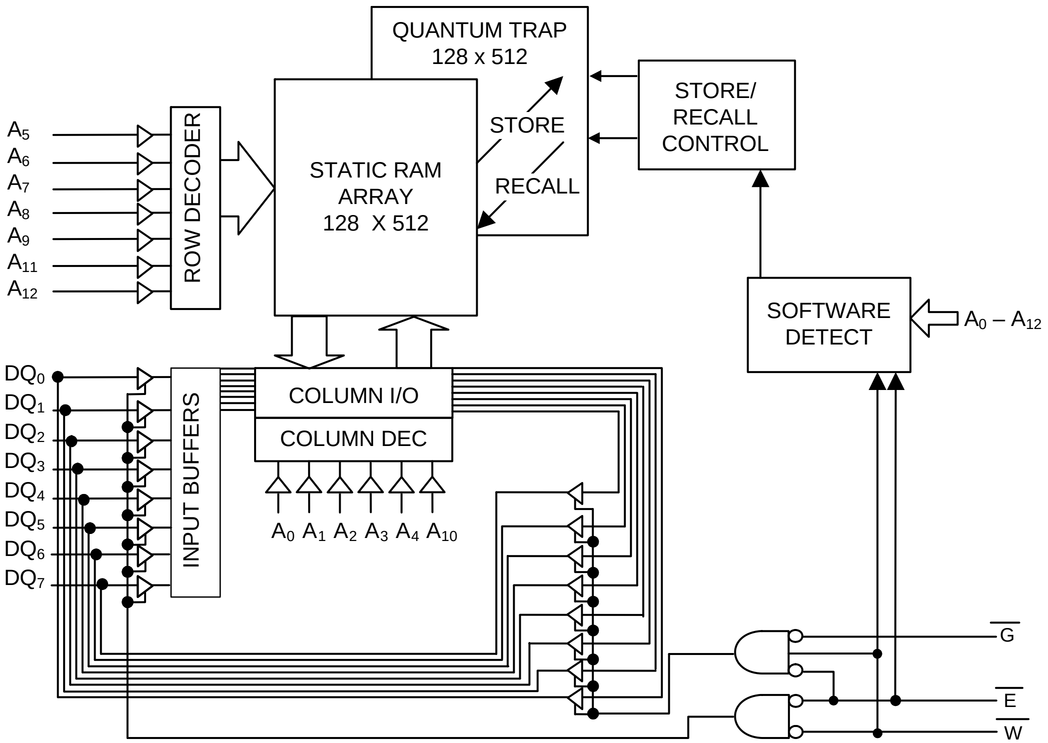
The Simtek STK11C68 is a 64Kb fast static RAM with a nonvolatile Quantum Trap storage element included with each memory cell.

The SRAM provides the fast access & cycle times, ease of use, and unlimited read & write endurance of a normal SRAM.

Data transfers under software control to the non-volatile storage cells (the *STORE* operation). On power-up, data is automatically restored to the SRAM (the *RECALL* operation). RECALL operations are also available under software control.

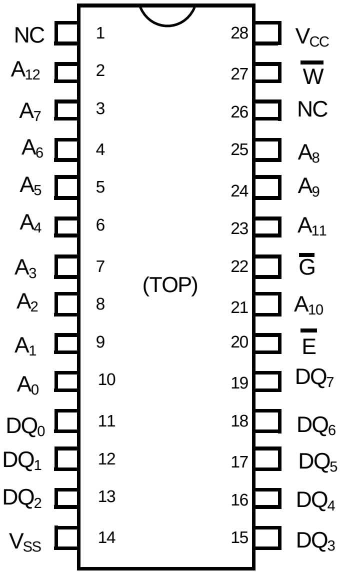
The Simtek nvSRAM is the first monolithic non-volatile memory to offer unlimited writes and reads. It is the highest performance, most reliable non-volatile memory available.

BLOCK DIAGRAM



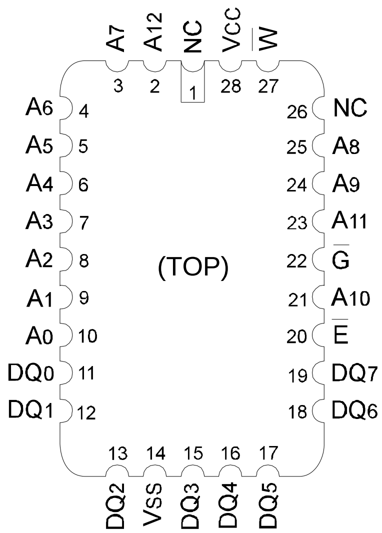
This product conforms to specifications per the terms of Simtek standard warranty. The product has completed Simtek internal qualification testing and has reached production status.

PIN CONFIGURATIONS



28-Pin DIP

28-Pin SOIC



28-Pin LCC

PIN DESCRIPTIONS

Pin Name	I/O	Description
A_{12}-A_0	Input	Address: The 13 address inputs select one of 8,192 bytes in the nvSRAM array
DQ_7-DQ_0	I/O	Data: Bi-directional 8-bit data bus for accessing the nvSRAM
$\overline{E}$	Input	Chip Enable: The active low $\overline{E}$ input selects the device
$\overline{W}$	Input	Write Enable: The active low $\overline{W}$ enables data on the DQ pins to be written to the address location latched by the falling edge of $\overline{E}$
$\overline{G}$	Input	Output Enable: The active low $\overline{G}$ input enables the data output buffers during read cycles. De-asserting $\overline{G}$ high caused the DQ pins to tri-state.
V_{CC}	Power Supply	Power: 5.0V, ±10%
V_{SS}	Power Supply	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on Input Relative to Ground . . . . –0.5V to 7.0V
Voltage on Input Relative to V_{SS} . . . . –0.6V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under Bias . . . . –55°C to 125°C
Storage Temperature . . . . –65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Package Thermal Characteristics - See Website at http://www.simtek.com

DC CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL/ MILITARY		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}[b]	Average V_{CC} Current		90 75 65 N/A		90 75 65 55	mA mA mA mA	t_{AVAV} = 25ns (commercial and industrial only) t_{AVAV} = 35ns t_{AVAV} = 45ns t_{AVAV} = 55ns
I_{CC_2}[c]	Average V_{CC} Current during *STORE*		3		3	mA	All Inputs Don’t Care, V_{CC} = max
I_{CC_3}[b]	Average V_{CC} Current at t_{AVAV} = 200ns 5V, 25°C, Typical		10		10	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I_{SB_1}[d]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		27 23 20 N/A		28 24 21 20	mA mA mA mA	t_{AVAV} = 25ns, $\overline{E} \geq V_{IH}$ (commercial and industrial only) t_{AVAV} = 35ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 45ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 55ns, $\overline{E} \geq V_{IH}$
I_{SB_2}[d]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		750		1500	µA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±5		±5	µA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic “1” Voltage	2.2	V_{CC} + .5	2.2	V_{CC} + .5	V	All Inputs
V_{IL}	Input Logic “0” Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Output Logic “1” Voltage	2.4		2.4		V	I_{OUT} = – 4mA
V_{OL}	Output Logic “0” Voltage		0.4		0.4	V	I_{OUT} = 8mA
T_A	Operating Temperature	0	70	–40	85	°C	

Note b: I_{CC_1} and I_{CC_3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: I_{CC_2} is the average current required for the duration of the *STORE* cycle (t_{STORE}) .
Note d: $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input Pulse Levels . . . . 0V to 3V
Input Rise and Fall Times . . . . ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . See Figure 1

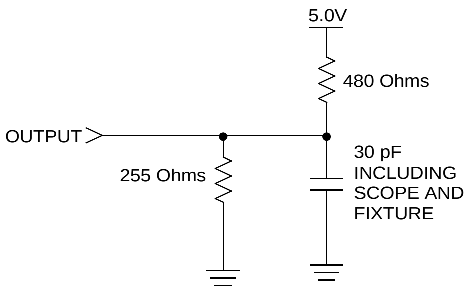


Figure 1: AC Output Loading

CAPACITANCE[e] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input capacitance	8	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note e: These parameters are guaranteed but not tested.

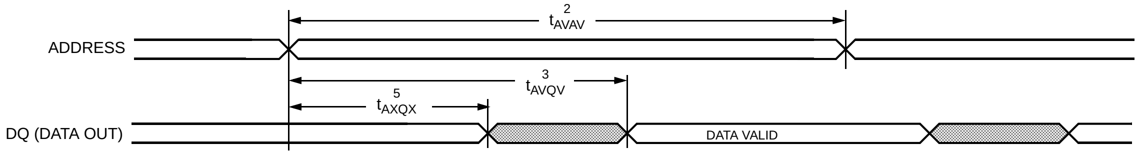
SRAM READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

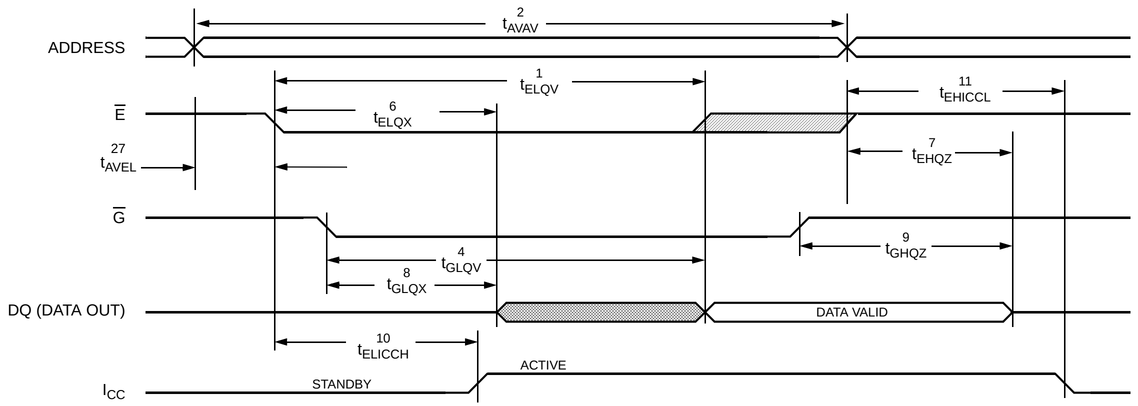
NO.	SYMBOLS #1, #2	SYMBOLS Alt.	PARAMETER	STK11C68-25 MIN	STK11C68-25 MAX	STK11C68-35 MIN	STK11C68-35 MAX	STK11C68-45 MIN	STK11C68-45 MAX	STK11C68-55 MIN	STK11C68-55 MAX	UNITS
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45		55	ns
2	t_{AVAV}[f], t_{ELEH}[f]	t_{RC}	Read Cycle Time	25		35		45		55		ns
3	t_{AVQV}[g]	t_{AA}	Address Access Time		25		35		45		55	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20		25	ns
5	t_{AXQX}[g]	t_{OH}	Output Hold after Address Change	5		5		5		5		ns
6	t_{ELQX}	t_{LZ}	Address Change or Chip Enable to Output Active	5		5		5		5		ns
7	t_{EHQZ}[h]	t_{HZ}	Address Change or Chip Disable to Output Inactive		10		13		15		25	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		0		ns
9	t_{GHQZ}[h]	t_{OHZ}	Output Disable to Output Inactive		10		13		15		25	ns
10	t_{ELICCH}[e]	t_{PA}	Chip Enable to Power Active	0		0		0		0		ns
11	t_{EHICCL}[d, e]	t_{PS}	Chip Disable to Power Standby		25		35		45		55	ns

Note f: $\overline{W}$ must be high during SRAM READ cycles and low during SRAM WRITE cycles.
Note g: I/O state assumes $\overline{E}$, $\overline{G}$ < V_{IL} and $\overline{W}$ > V_{IH}; device is continuously selected.
Note h: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled[f, g]



SRAM READ CYCLE #2: $\overline{E}$ and $\overline{G}$ Controlled[f]

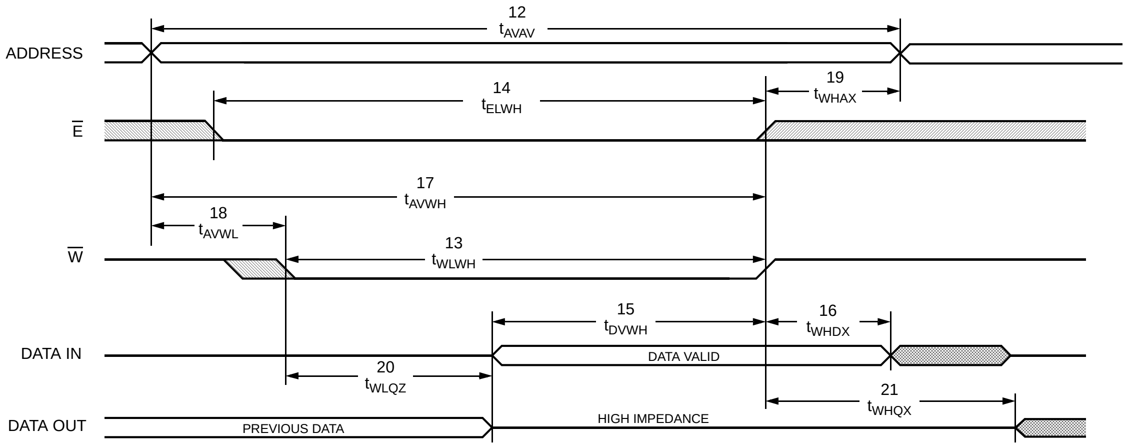


SRAM WRITE CYCLES #1 & #2 (V_{CC} = 5.0V ± 10%)

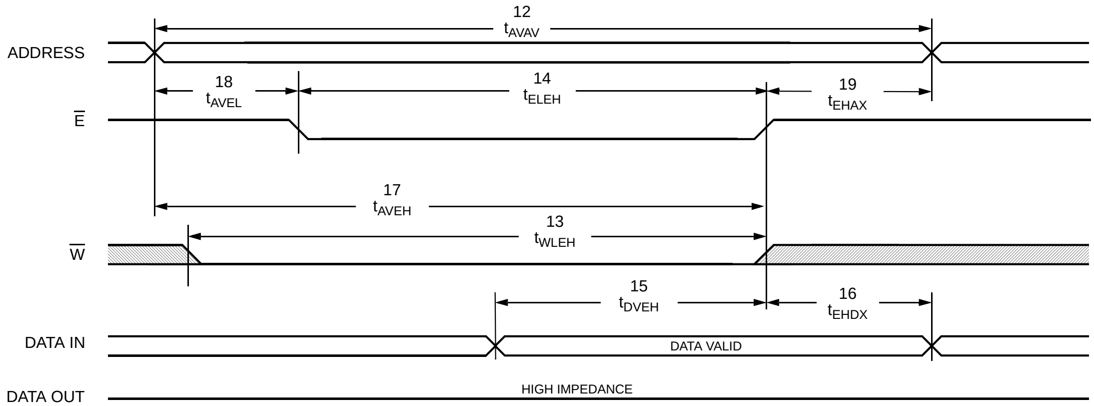
NO.	SYMBOLS #1	SYMBOLS #2	SYMBOLS Alt.	PARAMETER	STK11C68-25 MIN	STK11C68-25 MAX	STK11C68-35 MIN	STK11C68-35 MAX	STK11C68-45 MIN	STK11C68-45 MAX	STK11C68-55 MIN	STK11C68-55 MAX	UNITS
12	t_{AVAV}	t_{ELEH}	t_{WC}	Write Cycle Time	25		35		45		55		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		45		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		45		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		30		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		45		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		0		ns
20	$t_{WLQZ}^{h,\,i}$		t_{WZ}	Write Enable to Output Disable		10		13		15		35	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	5		5		5		5		ns

Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
Note j: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[j]



SRAM WRITE CYCLE #2: $\overline{E}$ and $\overline{G}$ Controlled[j]

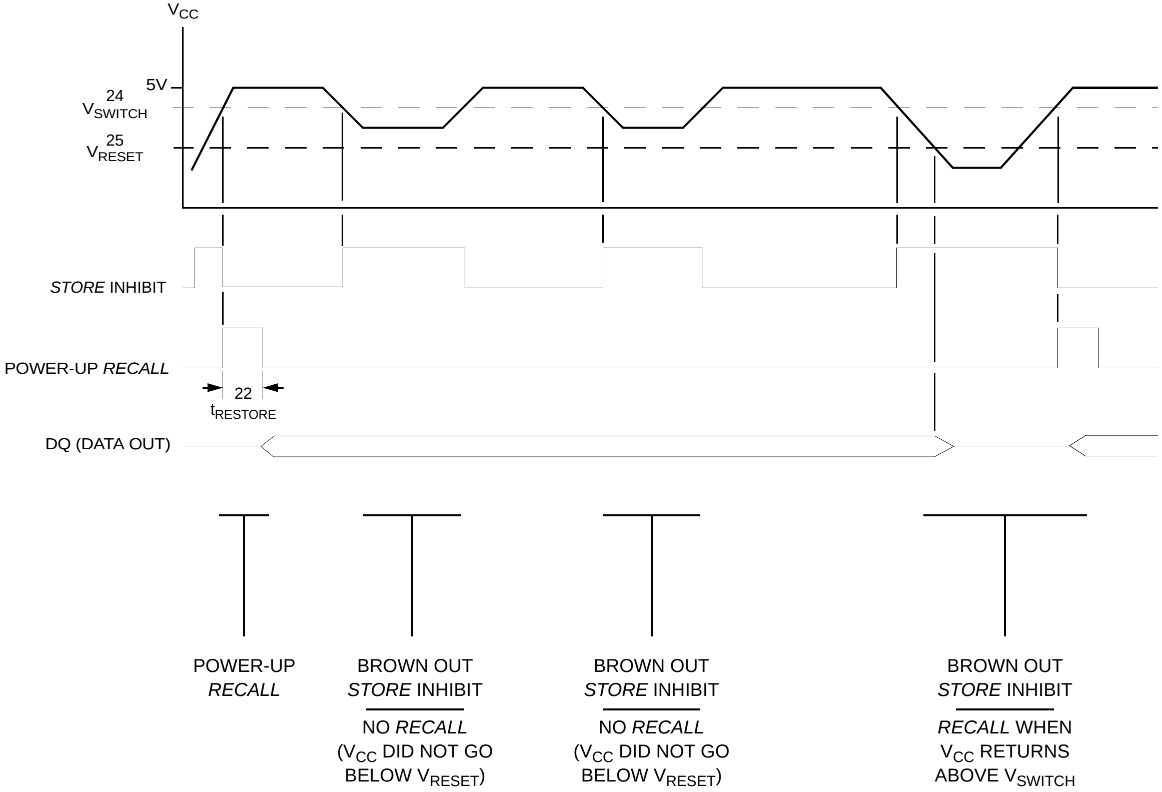


AutoStore™ INHIBIT/POWER-UP *RECALL* (V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS	PARAMETER	STK11C68		UNITS	NOTES
	Standard		MIN	MAX		
22	$t_{RESTORE}$	Power-up *RECALL* Duration		550	μs	k
23	t_{STORE}	*STORE* Cycle Duration		10	ms	
24	V_{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V	
25	V_{RESET}	Low Voltage Reset Level		3.6	V	

Note k: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.

AutoStore™ INHIBIT/POWER-UP *RECALL*



SOFTWARE *STORE/RECALL* MODE SELECTION

$\overline{E}$	$\overline{W}$	A_{12} - A_0 (hex)	MODE	I/O	NOTES
L	H	0000 1555 0AAA 1FFF 10F0 0F0F	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile *STORE*	Output Data Output Data Output Data Output Data Output Data Output High Z	l
L	H	0000 1555 0AAA 1FFF 10F0 0F0E	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile *RECALL*	Output Data Output Data Output Data Output Data Output Data Output High Z	l

Note l: The six consecutive addresses must be in the order listed. $\overline{W}$ must be high during all six consecutive $\overline{E}$ controlled cycles to enable a nonvolatile cycle.

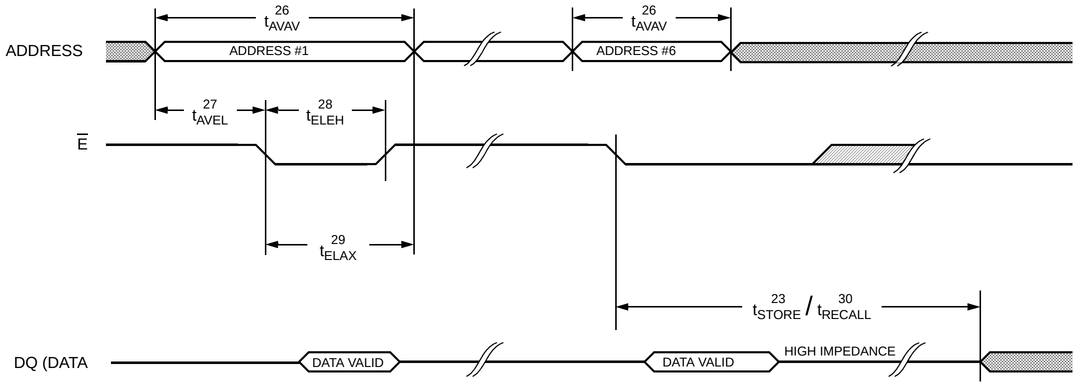
SOFTWARE *STORE/RECALL* CYCLE$^{m, n}$ (V_{CC} = 5.0V $\pm$ 10%)

NO.	SYMBOLS	PARAMETER	STK11C68-25		STK11C68-35		STK11C68-45		STK11C68-55		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
26	t_{AVAV}	*STORE/RECALL* Initiation Cycle Time	25		35		45		55		ns
27	t_{AVEL}^{m}	Address Set-up Time	0		0		0		0		ns
28	t_{ELEH}^{m}	Clock Pulse Width	20		25		30		35		ns
29	t_{ELAX}^{m}	Address Hold Time	20		20		20		20		ns
30	t_{RECALL}^{m}	*RECALL* Duration		20		20		20		20	μs

Note m: The software sequence is clocked on the falling edge of $\overline{E}$ controlled READs without involving $\overline{G}$ (double clocking will abort the sequence). See application note: MA0002 http://www.simtek.com/attachments/AppNote02.pdf

Note n: The six consecutive addresses must be in the order listed in the Software *STORE/RECALL* Mode Selection Table: (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a *STORE* cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE *STORE/RECALL* CYCLE: $\overline{E}$ Controlled^{n}



DEVICE OPERATION

The STK11C68 is a versatile memory chip that provides several modes of operation. The STK11C68 can operate as a standard 8K x 8 SRAM. It has an 8K x 8 Nonvolatile Elements shadow to which the SRAM information can be copied or from which the SRAM can be updated in nonvolatile mode.

NOISE CONSIDERATIONS

Note that the STK11C68 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK11C68 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ is high. The address specified on pins A_{0-12} determines which of the 8,192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

SOFTWARE NONVOLATILE *STORE*

The STK11C68 software *STORE* cycle is initiated by executing sequential READ cycles from six specific address locations. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0F (hex)	Initiate *STORE* cycle

The software sequence must be clocked with $\overline{E}$ controlled READs.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE *RECALL*

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of READ operations must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0E (hex)	Initiate *RECALL* cycle

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the Nonvolatile Elements. The nonvolatile data can be recalled an unlimited number of times.

POWER-UP *RECALL*

During power up, or after any low-power condition ($V_{CC} < V_{RESET}$), an internal *RECALL* request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

If the STK11C68 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between $\overline{W}$ and system V_{CC} or between $\overline{E}$ and system V_{CC}.

HARDWARE PROTECT

The STK11C68 offers hardware protection against inadvertent *STORE* operation during low-voltage conditions. When $V_{CC} < V_{SWITCH}$, software *STORE* operations are inhibited.

LOW AVERAGE ACTIVE POWER

The STK11C68 draws significantly less current when it is cycled at times longer than 50ns. Figure 2 shows the relationship between I_{CC} and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 5.5V, 100% duty cycle on chip enable). Figure 3 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK11C68 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READs to WRITEs; 5) the operating temperature; 6) the V_{cc} level; and 7) I/O loading.

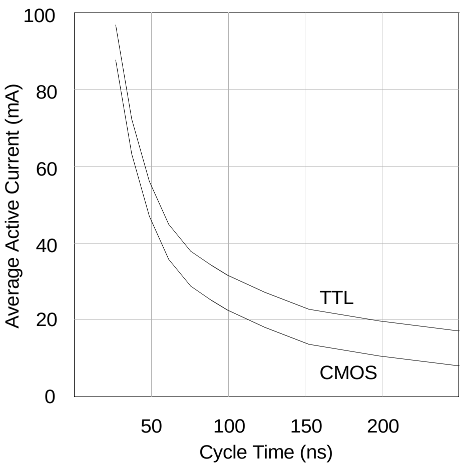


Figure 2: I_{CC} (max) Reads

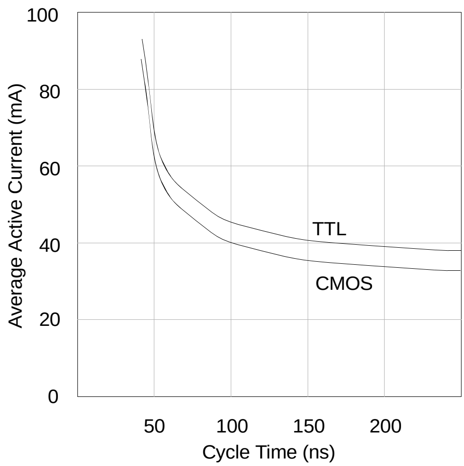


Figure 3: I_{CC} (max) Writes

BEST PRACTICES

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The non-volatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites will sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, etc. should always program a unique NV pattern (e.g., complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, etc.).

COMMERCIAL AND INDUSTRIAL ORDERING INFORMATION

STK11C68 - S F 45 I TR

Temperature Range
- Blank = Tube
- TR = Tape and Reel

Temperature Range
- Blank = Commercial (0 to 70°C)
- I = Industrial (–40 to 85°C)

Access Time
- 25 = 25ns
- 35 = 35ns
- 45 = 45ns

Lead Finish
- F = 100% Sn (Matte Tin)

Package
- S = Plastic 28-pin 330 mil SOIC
- C = Ceramic 28-pin 300 mil DIP
- L = Ceramic 28-pin 350 mil LCC

MILITARY ORDERING INFORMATION

STK11C68 - 5 C 45 M

Temperature Range

M = Military (–55 to 125°C)

Access Time

35 = 35ns

45 = 45ns

55 = 55ns

Package

C = Ceramic 28-pin 300 mil DIP (gold lead finish)

K = Ceramic 28-pin 300 mil DIP (solder dip finish)

L = Ceramic 28 pin LCC

Retention / Endurance

5 = Military (10 years/10^5cycles)

SMD5962-92324 04 MX X

Lead Finish

A = Solder DIP lead finish

C = Gold lead DIP finish

X = Lead finish “A” or “C” is acceptable

Package

MX = Ceramic 28 pin 300-mil DIP

MY = Ceramic 28 pin LCC

Device Class Indication—Class M

Access Time

04 = 55ns

05 = 45ns

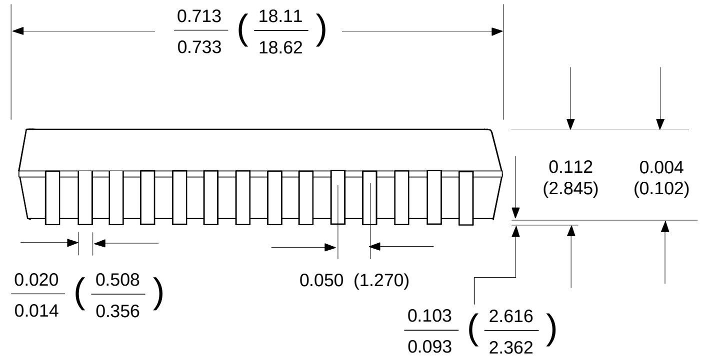
06 = 35ns

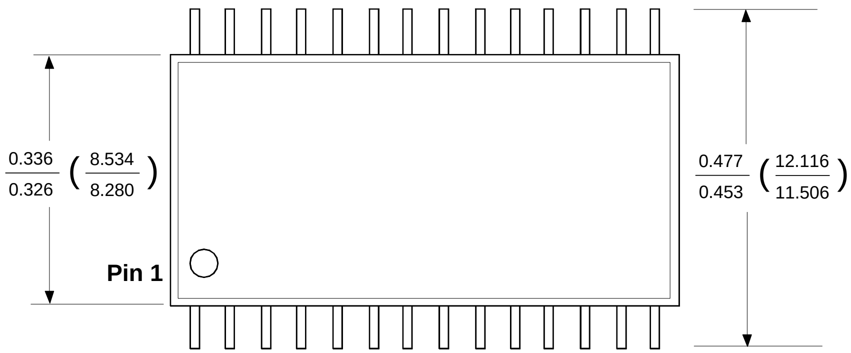
ORDERING CODES

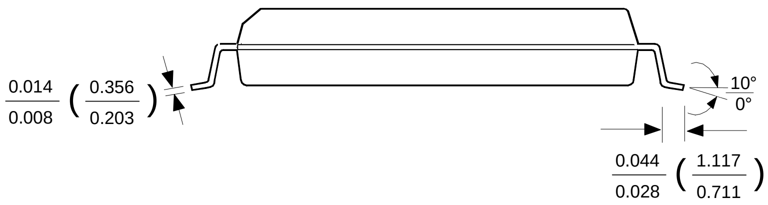
Part Number	Description	Access Time	Temperature
STK11C68-SF25	5V 64K-8b SoftStore nvSRAM SOP28-330	25 ns access time	Commercial
STK11C68-SF35	5V 64K-8b SoftStore nvSRAM SOP28-330	35 ns access time	Commercial
STK11C68-SF45	5V 64K-8b SoftStore nvSRAM SOP28-330	45 ns access time	Commercial
STK11C68-SF25TR	5V 64K-8b SoftStore nvSRAM SOP28-330	25 ns access time	Commercial
STK11C68-SF35TR	5V 64K-8b SoftStore nvSRAM SOP28-330	35 ns access time	Commercial
STK11C68-SF45TR	5V 64K-8b SoftStore nvSRAM SOP28-330	45 ns access time	Commercial
STK11C68-L35	5V 64K-8b SoftStore nvSRAM CLCC28	35 ns access time	Commercial
STK11C68-L45	5V 64K-8b SoftStore nvSRAM CLCC28	45 ns access time	Commercial
STK11C68-C35	5V 64K-8b SoftStore nvSRAM CDIP28-300	35 ns access time	Commercial
STK11C68-C45	5V 64K-8b SoftStore nvSRAM CDIP28-300	45 ns access time	Commercial
STK11C68-SF25I	5V 64K-8b SoftStore nvSRAM SOP28-330	25 ns access time	Industrial
STK11C68-SF35I	5V 64K-8b SoftStore nvSRAM SOP28-330	35 ns access time	Industrial
STK11C68-SF45I	5V 64K-8b SoftStore nvSRAM SOP28-330	45 ns access time	Industrial
STK11C68-SF25ITR	5V 64K-8b SoftStore nvSRAM SOP28-330	25 ns access time	Industrial
STK11C68-SF35ITR	5V 64K-8b SoftStore nvSRAM SOP28-330	35 ns access time	Industrial
STK11C68-SF45ITR	5V 64K-8b SoftStore nvSRAM SOP28-330	45 ns access time	Industrial
STK11C68-L35I	5V 64K-8b SoftStore nvSRAM CLCC28	35 ns access time	Industrial
STK11C68-L45I	5V 64K-8b SoftStore nvSRAM CLCC28	45 ns access time	Industrial
STK11C68-C35I	5V 64K-8b SoftStore nvSRAM CDIP28-300	35 ns access time	Industrial
STK11C68-C45I	5V 64K-8b SoftStore nvSRAM CDIP28-300	45 ns access time	Industrial
STK11C68-5L35M	5V 64K-8b SoftStore nvSRAM CLCC28	35 ns access time	Military
STK11C68-5L45M	5V 64K-8b SoftStore nvSRAM CLCC28	45 ns access time	Military
STK11C68-5L55M	5V 64K-8b SoftStore nvSRAM CLCC28	55 ns access time	Military
STK11C68-5C35M	5V 64K-8b SoftStore nvSRAM CDIP28-300	35 ns access time	Military
STK11C68-5C45M	5V 64K-8b SoftStore nvSRAM CDIP28-300	45 ns access time	Military
STK11C68-5C55M	5V 64K-8b SoftStore nvSRAM CDIP28-300	55 ns access time	Military
STK11C68-5K35M	5V 64K-8b SoftStore nvSRAM CDIP28-300	35 ns access time	Military

Package Diagrams

28 Pin 330 mil SOIC



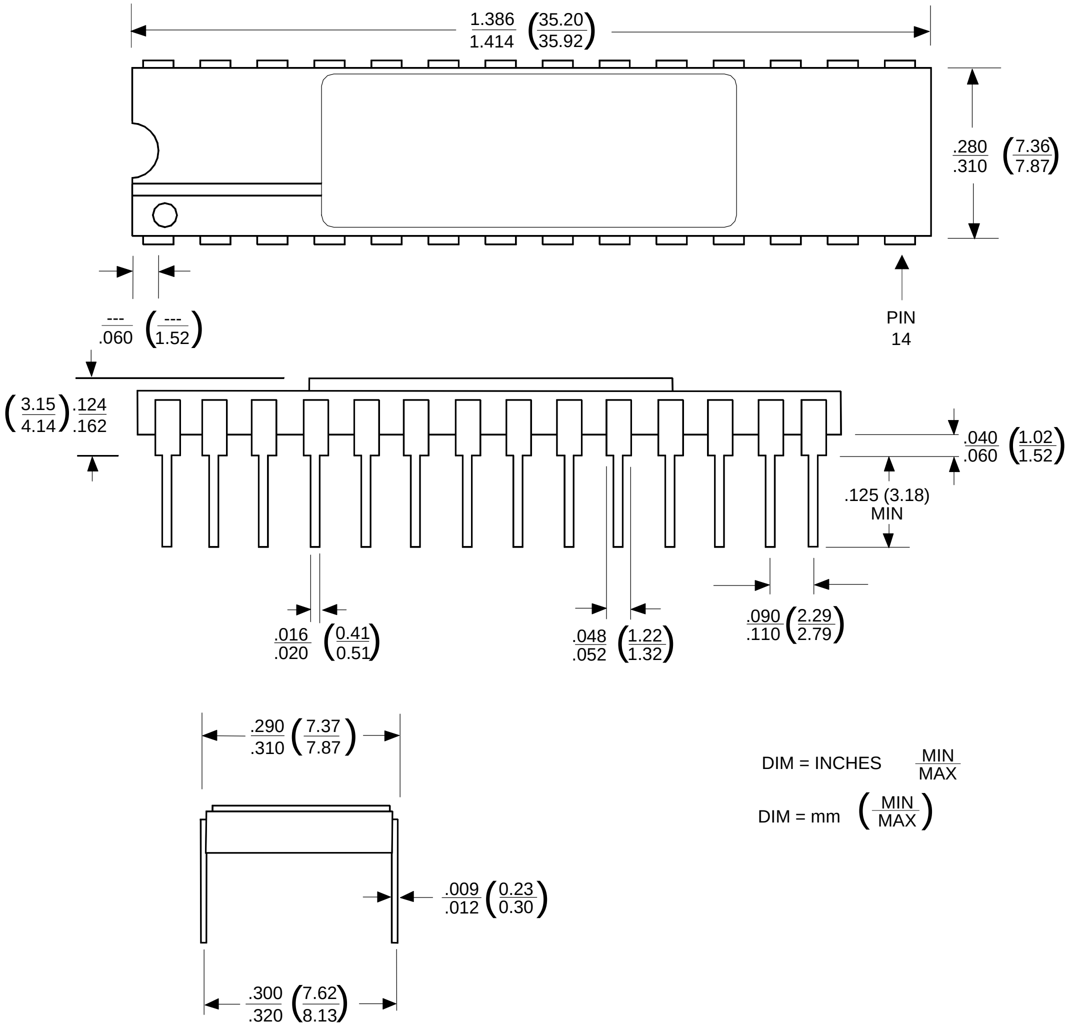




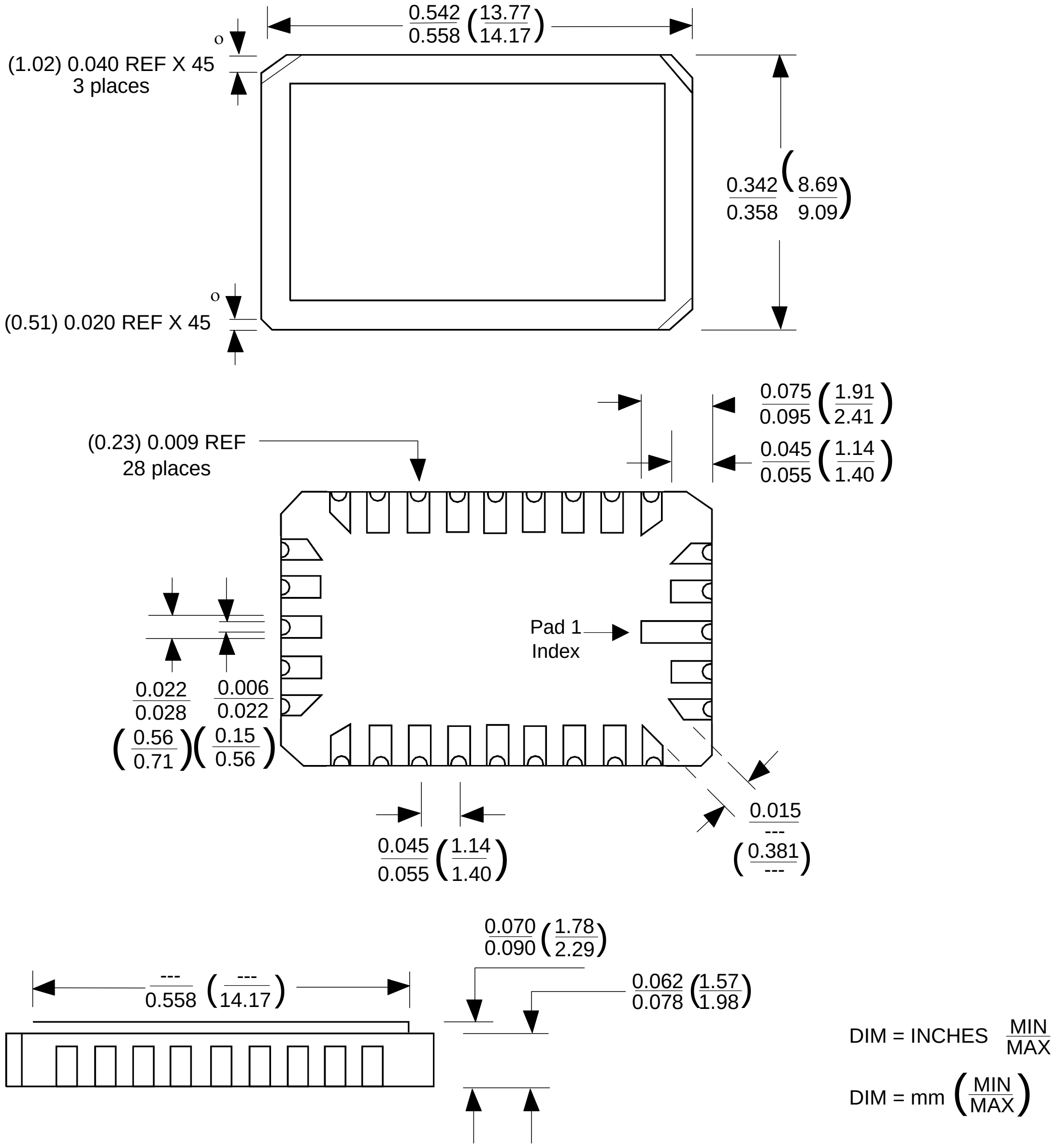
DIM = INCHES $\frac{\text{MIN}}{\text{MAX}}$

DIM = mm $\left(\frac{\text{MIN}}{\text{MAX}}\right)$

28 Pin 300 mil SP DIL Sidebraze



28 Pin 350 mil LCC



Document Revision History

Revision	Date	Summary
0.0	December 2002	Combined commercial, industrial and military data sheets. Removed 20 nsec device.
0.1	September 2003	Added lead-free lead finish
0.2	March 2006	Removed leaded lead finish for all Commercial/Industrial Parts, Removed “P” package.
0.3	February 2007	Add fast power-down slew RSK information Restore Comm/Ind C & L Package Options Add Tape Reel Ordering Options Add Product Ordering Code Listing Add Package Outline Drawings Reformat Entire Document
0.4	July 2007	extend definition of t_{HZ} (#7) update fig. SRAM READ CYCLE #2, SRAM WRITE CYCLE #1, Note l and Note m to clarify product usage
2.0	June 2008	Added STK-11C68-5 part number to header. Page 3: in the DC characteristics table, identified access times valid for commercial and industrial applications only. Also, referred users to Website for package thermal characteristics. Page 4, in SRAM Read Cycles #1 & #2 table, revised description for t_{ELQX} and t_{EHQZ} and changed Symbol #2 to ^{t}ELEH for Read Cycle Time; updated SRAM Read Cycle #2 timing diagram and changed title to add $\overline{G}$ controlled. Page 12: added access time column to ordering information table.