National Semiconductor

74BCT652
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

This device consists of a bus transceiver circuit with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

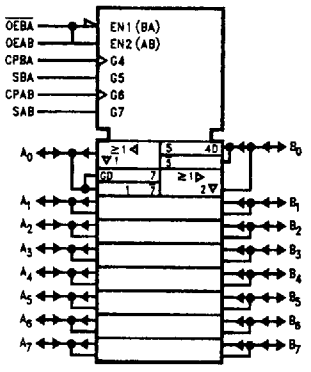
Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})
- TRI-STATE® outputs drive bus lines

Ordering Code: See Section 11

Logic Symbols

IEEE/IEC



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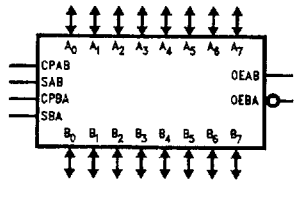

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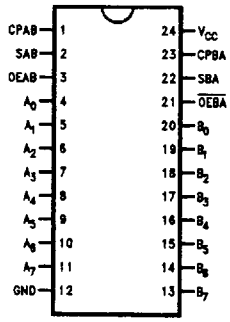
Connection Diagram

Pin Assignment
DIP and SOIC



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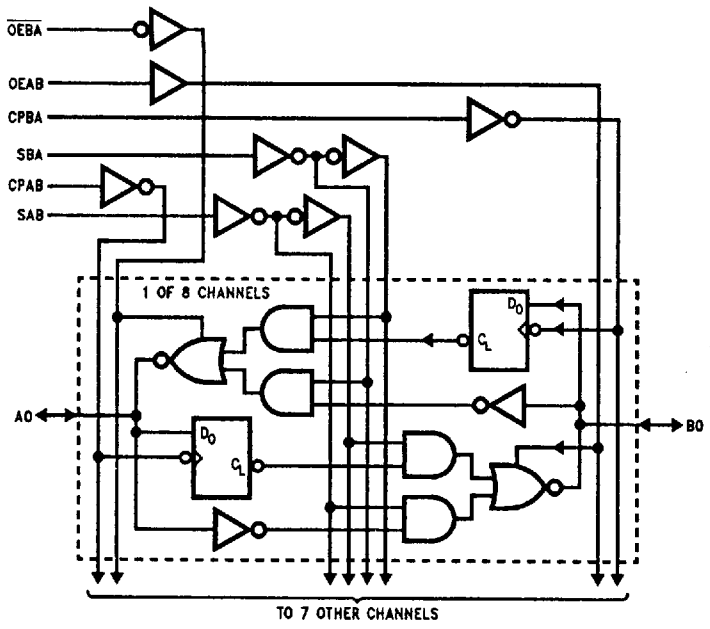
Pin Names	Description
A_0–A_7, B_0–B_7	A and B Inputs/ TRI-STATE® Outputs
CPAB, CPBA	Clock Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

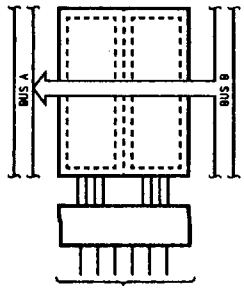
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with this device.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Note A: Real-Time Transfer Bus B to Bus A



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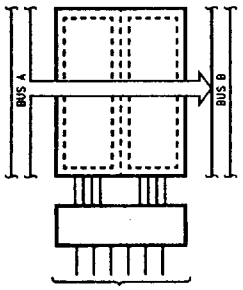
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Note B: Real-Time Transfer Bus A to Bus B



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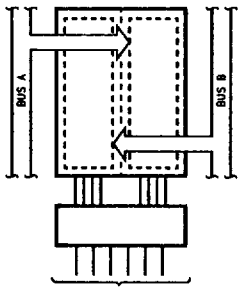
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

Note C: Storage



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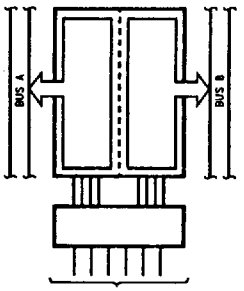
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	↗	X	X	X
L	X	X	↗	X	X
L	H	↗	↗	X	X

Note D: Transfer Storage Data to A or B



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OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	X

FIGURE 1

Inputs						Inputs/Outputs (Note 1)		Operating Mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↗	↗	X	X			Store A and B Data
X	H	↗	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↗	↗	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↗	X	X	Not Specified	Input	Hold A, Store B
L	L	↗	↗	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW to HIGH Clock Transition

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5.0	μA	Max	V_{IN} = 2.7V (Non I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V_{IN} = 7.0V (Non I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V (Non I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current			−225	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.25V (A_n, B_n)
I_{CCH}	Power Supply Current		15	22	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		40	49	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		15	22	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			74BCT $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max		
f_{max}	Max. Clock Frequency	90	172		90		MHz	8-1
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.8 2.8	5.9 5.1	8.8 8.8	2.8 2.8	9.9 9.9	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.7 2.4	4.6 5.8	7.5 9.2	1.7 2.4	8.9 9.8	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay SBA to A or SAB to B	3.0 2.4	7.0 6.6	11.0 11.0	3.0 2.4	11.3 11.3	ns	8-3
t_{PZH} t_{PZL}	Enable Time *OEBA to A	2.5 3.2	5.5 6.3	8.9 10.1	2.5 3.2	10.6 10.6	ns	8-5
t_{PHZ} t_{PLZ}	Disable Time *OEBA to A	1.8 2.4	5.4 5.4	8.6 8.6	1.8 2.4	9.5 9.5		
t_{PZH} t_{PZL}	Enable Time OEAB to B	1.5 2.3	4.6 5.2	7.1 8.1	1.5 2.3	8.1 8.1		
t_{PHZ} t_{PLZ}	Disable Time OEAB to B	2.2 2.2	5.2 5.2	9.1 8.0	2.2 2.2	9.1 8.0	ns	8-5

AC Operating Requirements: See Section 8 for Waveforms

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$		74BCT $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW, Bus to Clock	5.0 5.0		5.0 5.0		ns	8-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW, Bus to Clock	1.0 1.0		1.0 1.0		ns	8-6
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	5.0 5.0		5.0 5.0		ns	8-4

Extended AC Electrical Characteristics

Symbol	Parameter	74BCT T_A = Com, V_{CC} = Com, C_L = 50 pF, 8 Outputs Switching (Note 1)		74BCT T_A = Com, V_{CC} = Com, C_L = 250 pF, 1 Output Switching (Note 2)		74BCT T_A = Com, V_{CC} = Com, C_L = 250 pF, 8 Outputs Switching (Notes 1, 2)		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	2.8	10.5	3.0	12.0	4.0	15.6	ns
t_{PHL}	Clock to Bus	2.8	10.5	3.0	12.0	4.0	15.6	
t_{PLH}	Propagation Delay	2.0	9.5	2.5	10.9	4.0	15.0	ns
t_{PHL}	Bus to Bus	3.0	11.0	3.0	11.5	4.0	15.0	
t_{PLH}	Propagation Delay							
t_{PHL}	SBA to A or	3.0	12.5	3.0	14.2	4.0	18.1	ns
	SAB to B	3.0	12.5	3.0	14.2	4.0	18.1	

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitor the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	6.0	pF	V_{CC} = 5.0V (Control Inputs)
$C_{I/O}$	Input/Output Pin Capacitance	12.5	pF	V_{CC} = 5.0V (A_n, B_n)