DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4514
4-to-16 line decoder/demultiplexer with input latches

Product specification
File under Integrated Circuits, IC06

September 1993

Philips Semiconductors

PHILIPS

4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514

FEATURES

- Non-inverting outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4514 are high-speed Si-gate CMOS devices and are pin compatible with “4514” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4514 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs (A_0 to A_3), with latches, a latch enable input (LE), and an active LOW enable input ($\overline{E}$). The 16 outputs (Q_0 to Q_{15}) are mutually exclusive active HIGH. When LE is HIGH, the selected output is determined by the data on A_n. When LE goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\overline{E}$ is LOW, the selected output, determined by the contents of the latch, is HIGH. At $\overline{E}$ HIGH, all outputs are LOW. The enable input ($\overline{E}$) does not affect the state of the latch.

When the “4514” is used as a demultiplexer, $\overline{E}$ is the data input and A_0 to A_3 are the address inputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay A_n to Q_n	C_L = 15 pF; V_{CC} = 5 V	23	26	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	44	45	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LE	latch enable input (active HIGH)
2, 3, 21, 22	A_0 to A_3	address inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	Q_0 to Q_{15}	multiplexer outputs (active HIGH)
12	GND	ground (0 V)
23	$\overline{E}$	enable input (active LOW)
24	V_{CC}	positive supply voltage

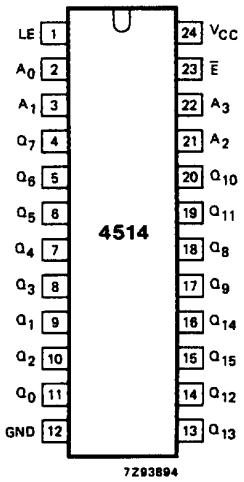

Fig.1 Pin configuration.

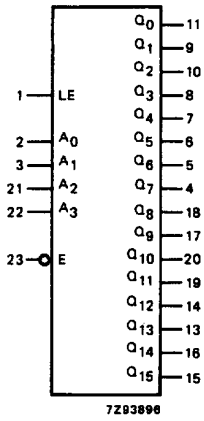

Fig.2 Logic symbol.

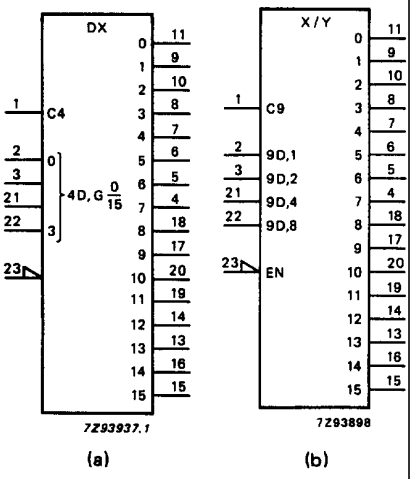

Fig.3 IEC logic symbol.

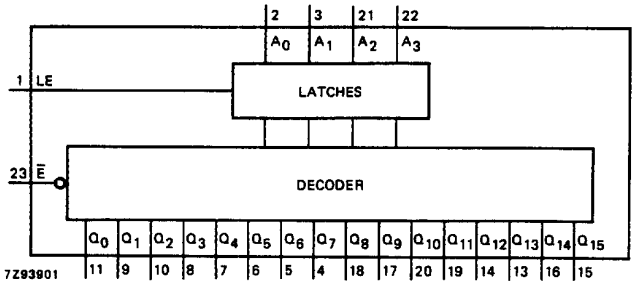

Fig.4 Functional diagram.

APPLICATIONS

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding

FUNCTION TABLE

INPUTS					OUTPUTS														
$\overline{E}$	A_0	A_1	A_2	A_3	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{14}	Q_{15}
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
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L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
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L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

Notes

1. LE = HIGH
   H = HIGH voltage level
   L = LOW voltage level
   X = don't care

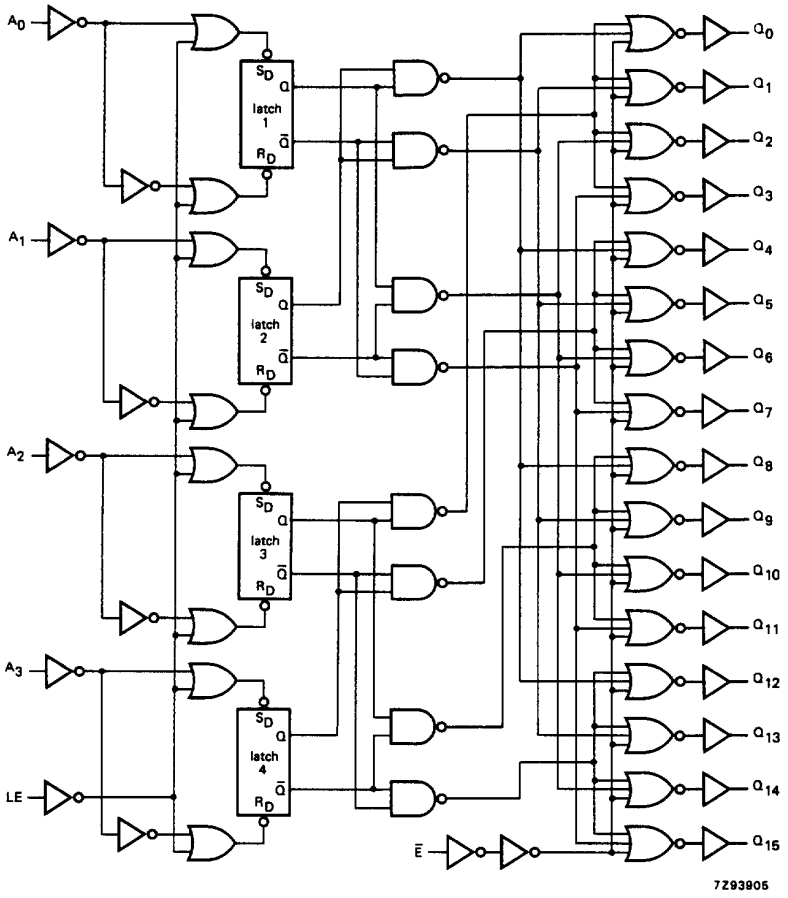


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to Q_n		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay LE to Q_n		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}$ to Q_n		41 15 12	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t_W	latch enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time A_n to LE	90 18 15	25 9 7		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig.7
t_h	hold time A_n to LE	1 1 1	–11 –4 –3		1 1 1		1 1 1		ns	2.0 4.5 6.0	Fig.7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

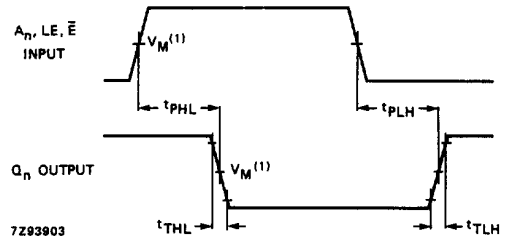
INPUT	UNIT LOAD COEFFICIENT
A_n	0.65
LE	1.40
$\overline{E}$	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

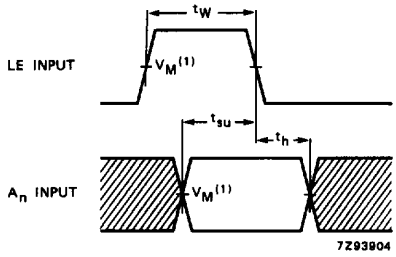
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to Q_n		30	55		69		83	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay LE to Q_n		29	50		63		75	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}$ to Q_n		17	40		50		60	ns	4.5	Fig.6
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6
t_W	latch enable pulse width HIGH	16	4		20		24		ns	4.5	Fig.7
t_{su}	set-up time A_n to LE	18	9		23		27		ns	4.5	Fig.7
t_h	hold time A_n to LE	3	−3		3		3		ns	4.5	Fig.7

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the input (A_n, LE, $\overline{E}$) to output (Q_n) propagation delays and the output transition times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the minimum pulse width of the latch enable input (LE) and the set-up and hold times for LE to A_n. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

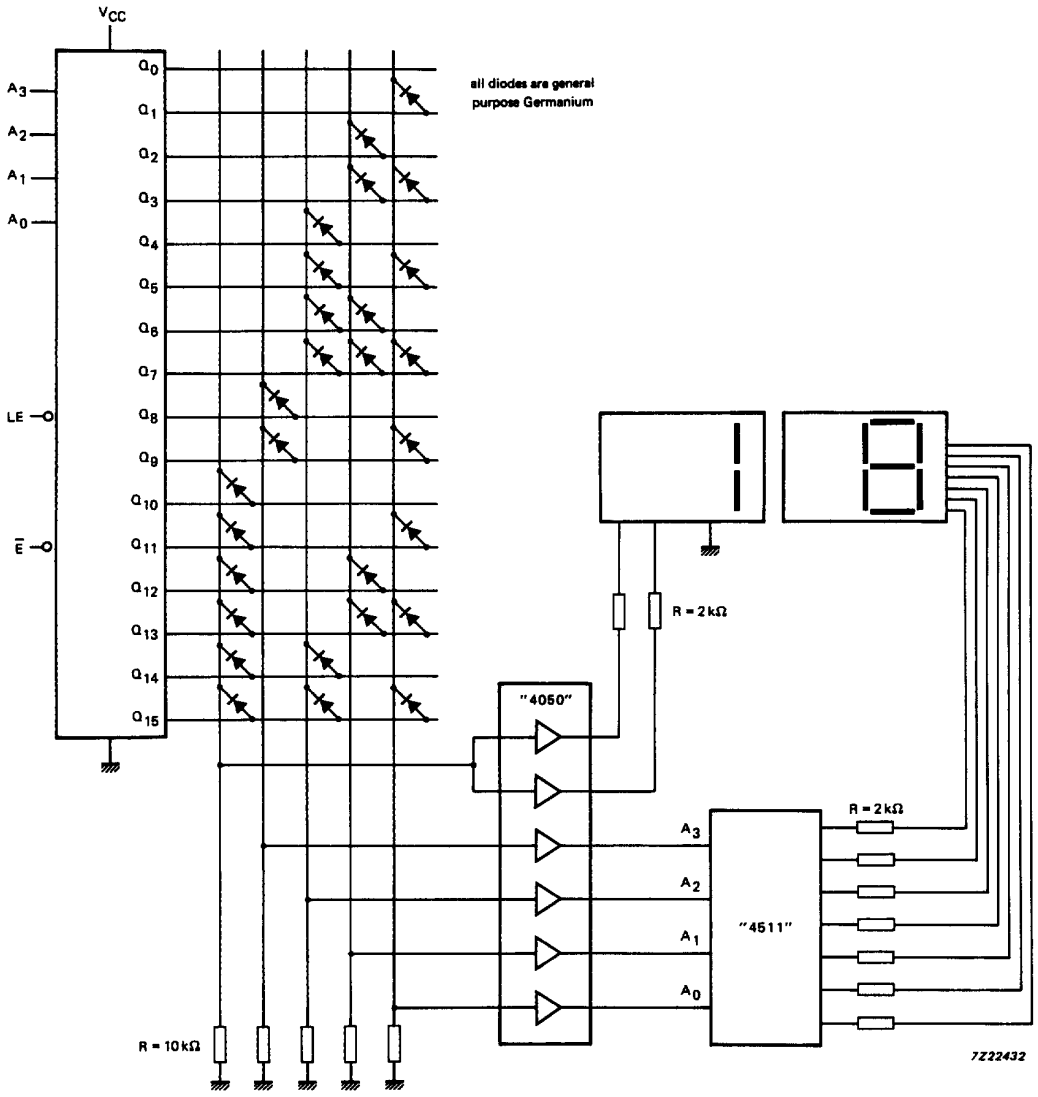


Fig.8 Code-to-code conversion; hexadecimal to BCD.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

Product Information

74HC/HCT4514; 4-to-16 line decoder/demultiplexer with input latches

Information as of 2002-11-28

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General description

The 74HC/HCT4514 are high-speed Si-gate CMOS devices and are pin compatible with '4514' of the '4000B' series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4514 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs (A_0 to A_3), with latches, a latch enable input (LE), and an active LOW enable input (E). The 16 outputs (Q_0 to Q_{15}) are mutually exclusive active HIGH. When LE is HIGH, the selected output is determined by the data on A_n. When LE goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When E is LOW, the selected output, determined by the contents of the latch, is HIGH. At E HIGH, all outputs are LOW. The enable input (E) does not affect the state of the latch.

When the '4514' is used as a demultiplexer, E is the data input and A_0 to A_3 are the address inputs.

Features

- Non-inverting outputs
- Output capability: standard
- I_{CC} category: MSI

Datasheet

Type number	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
74HC/HCT4514	4-to-16 line decoder/demultiplexer with input latches	01-Sep-93	Product specification	9	74	PDF Download

Additional datasheet info

To complete the device datasheet with package and family information, also download the following PDF files. The "Logic Package Information" document is required to determine in which package(s) this device is available.

	Document	Description
1	PDF HCT_FAMILY_SPECIFICATIONS	HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications

2	PDF HCT_PACKAGE_INFO	HC/T Package Info, The IC06 74HC/HCT/HCMOS Logic Package Information
3	PDF HCT_PACKAGE_OUTLINES	HC/T Package Outlines, The IC06 74HC/HCT/HCMOS Logic Package Outlines

Parametrics

Type number	Package	Description	Propagation Delay(ns)	Voltage	No. of Pins	Power Dissipation Considerations	Logic Switching Levels	Output Drive Capability
74HC4514D	SOT137 (SO24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HC4514DB	SOT340-1 (SSOP24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HC4514N	SOT101-1 (DIP24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HC4514PW	SOT355-1 (TSSOP24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HC4514U	uncased die	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HCT4514D	SOT137 (SO24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low
74HCT4514DB	SOT340-1 (SSOP24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low
74HCT4514N	SOT101-1 (DIP24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low

74HCT4514PW	SOT355-1 (TSSOP24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low
74HCT4514U	uncased die	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low

Products, packages, availability and ordering

Type number	North American type number	Ordering code (12NC)	Marking/Packing PDF Discretes packing info	Package	Device status	Buy online
74HC4514D	74HC4514D	9337 156 70652	Standard Marking * Bulk Pack, CECC	SOT137 (SO24)	Full production	BUY ONLINE
	74HC4514D-T	9337 156 70653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT137 (SO24)	Full production	BUY ONLINE
74HC4514DB	74HC4514DB	9351 900 90112	Standard Marking * Bulk Pack	SOT340-1 (SSOP24)	Full production	BUY ONLINE
	74HC4514DB-T	9351 900 90118	Standard Marking * Reel Pack, SMD, 13"	SOT340-1 (SSOP24)	Full production	BUY ONLINE
74HC4514N	74HC4514N	9336 710 40652	Standard Marking * Bulk Pack, CECC	SOT101-1 (DIP24)	Full production	BUY ONLINE
74HC4514PW	74HC4514PW	9352 624 15112	Standard Marking * Bulk Pack	SOT355-1 (TSSOP24)	Full production	BUY ONLINE
	74HC4514PW-T	9352 624 15118	Standard Marking * Reel Pack, SMD, 13"	SOT355-1 (TSSOP24)	Full production	BUY ONLINE
74HC4514U		9338 396 30005	No Marking * Chips on Wafer, Pre-Sawn, On FFC	NAU000	Full production	-
74HCT4514D	74HCT4514D	9337 156 90652	Standard Marking * Bulk Pack, CECC	SOT137 (SO24)	Full production	BUY ONLINE
	74HCT4514D-T	9337 156 90653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT137 (SO24)	Full production	BUY ONLINE
74HCT4514DB	74HCT4514DB	9351 900 80112	Standard Marking * Bulk Pack	SOT340-1 (SSOP24)	Full production	BUY ONLINE
	74HCT4514DB-T	9351 900 80118	Standard Marking * Reel Pack, SMD, 13"	SOT340-1 (SSOP24)	Full production	BUY ONLINE
74HCT4514N	74HCT4514N	9336 710 70652	Standard Marking * Bulk Pack, CECC	SOT101-1 (DIP24)	Full production	BUY ONLINE

74HCT4514PW	74HCT4514PW	9352 624 14112	Standard Marking * Bulk Pack	SOT355-1 (TSSOP24)	Full production	BUY ONLINE
	74HCT4514PW-T	9352 624 14118	Standard Marking * Reel Pack, SMD, 13"	SOT355-1 (TSSOP24)	Full production	BUY ONLINE
74HCT4514U		9338 396 40005	No Marking * Chips on Wafer, Pre-Sawn, On FFC	NAU000	Full production	-

Products in the above table are all in production. Some variants are discontinued; click here for information on these variants.

Similar products

MORE 74HC/HCT4514 links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

Support & tools

PDF HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications (date 01-Mar-98)
PDF HC/T User Guide (date 01-Nov-97)

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