

# 74F153

# Dual 4-Input Multiplexer

The F153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the F153 can generate any two functions of three variables.

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Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

# **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.



April 1988 Revised September 2000

# 74F153 Dual 4-Input Multiplexer

#### **General Description**

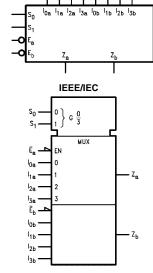
The F153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the F153 can generate any two functions of three variables.

#### **Ordering Code:**

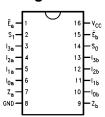
Order Number	Package Number	Package Description					
74F153SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow					
74F153SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide					
74F153PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide					

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### **Logic Symbols**



#### **Connection Diagram**



#### **Unit Loading/Fan Out**

Pin Names	Description	U.L.	Input I <sub>IH</sub> /I <sub>IL</sub>	
Pin Names	Description	HIGH/LOW	Output I <sub>OH</sub> /I <sub>OL</sub>	
I <sub>0a</sub> –I <sub>3a</sub>	Side A Data Inputs	1.0/1.0	20 μA/-0.6 mA	
I <sub>0b</sub> –I <sub>3b</sub>	Side B Data Inputs	1.0/1.0	20 μA/-0.6 mA	
S <sub>0</sub> , S <sub>1</sub>	Common Select Inputs	1.0/1.0	20 μA/-0.6 mA	
E <sub>a</sub> E <sub>b</sub>	Side A Enable Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA	
E <sub>b</sub>	Side B Enable Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA	
Z <sub>a</sub>	Side A Output	50/33.3	−1 mA/20 mA	
Z <sub>b</sub>	Side B Output	50/33.3	−1 mA/20 mA	

#### **Truth Table**

Select	Inputs		Output				
S <sub>0</sub>	S <sub>1</sub>	Ē	I <sub>0</sub>	I <sub>1</sub>	l <sub>2</sub>	I <sub>3</sub>	z
Χ	Χ	Н	Х	Х	Χ	Χ	L
L	L	L	L	Χ	Χ	Χ	L
L	L	L	Н	Χ	Х	Χ	Н
Н	L	L	Х	L	Χ	Χ	L
Н	L	L	Х	Н	Χ	Χ	Н
L	Н	L	Х	Χ	L	Χ	L
L	Н	L	Х	Χ	Н	Χ	Н
Н	Н	L	Х	Χ	Χ	L	L
Н	Н	L	Х	Х	Х	Н	Н

H = HIGH Voltage Level

L = LOW

X = Immaterial

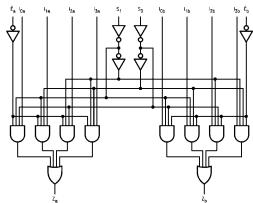
#### **Functional Description**

The F153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs  $(S_0,\,S_1).$  The two 4-input multiplexer circuits have individual active LOW Enables  $(\overline{E}_a,\,\overline{E}_b)$  which can be used to strobe the outputs independently. When the Enables  $(\overline{E}_a,\,\overline{E}_b)$  are HIGH, the corresponding outputs  $(Z_a,\,Z_b)$  are forced LOW. The F153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are as follows:

$$\begin{split} Z_{a} &= \overline{E}_{a} \bullet (I_{0a} \bullet \overline{S}_{1} \bullet \overline{S}_{0} + I_{1a} \bullet \overline{S}_{1} \bullet S_{0} + \\ I_{2a} \bullet S_{1} \bullet \overline{S}_{0} + I_{3a} \bullet S_{1} \bullet S_{0} + \\ Z_{b} &= \overline{E}_{b} \bullet (I_{0b} \bullet \overline{S}_{1} \bullet \overline{S}_{0} + I_{1b} \bullet \overline{S}_{1} \bullet S_{0} + \\ I_{2b} \bullet S_{1} \bullet \overline{S}_{0} + I_{3b} \bullet S_{1} \bullet S_{0}) \end{split}$$

The F153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The F153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

0°C to +70°C

+4.5V to +5.5V

# Absolute Maximum Ratings(Note 1)

# Recommended Operating Conditions

Free Air Ambient Temperature

Supply Voltage

 $\begin{array}{ll} \mbox{Storage Temperature} & -65^{\circ}\mbox{C to } +150^{\circ}\mbox{C} \\ \mbox{Ambient Temperature under Bias} & -55^{\circ}\mbox{C to } +125^{\circ}\mbox{C} \\ \end{array}$ 

 $\begin{array}{ll} \mbox{Ambient Temperature under Bias} & -55^{\circ}\mbox{C to } +125^{\circ}\mbox{C} \\ \mbox{Junction Temperature under Bias} & -55^{\circ}\mbox{C to } +150^{\circ}\mbox{C} \\ \end{array}$ 

 $V_{\rm CC}$  Pin Potential to Ground Pin  $-0.5 {\rm V}$  to  $+7.0 {\rm V}$  Input Voltage (Note 2)  $-0.5 {\rm V}$  to  $+7.0 {\rm V}$  Input Current (Note 2) -30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with  $V_{CC} = 0V$ ) Standard Output -0.5V t

3-STATE Output -0.5V to +5.5V Current Applied to Output

in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

 $\textbf{Note 2:} \ \textbf{Either voltage limit or current limit is sufficient to protect inputs.}$ 

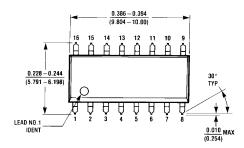
#### **DC Electrical Characteristics**

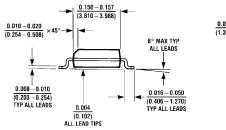
Symbol	Paramete	r	Min	Тур	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18 \text{ mA}$
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = -1 mA
		5% V <sub>CC</sub>	2.7			V	IVIIII	$I_{OH} = -1 \text{ mA}$
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current				5.0	μΑ	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test				7.0	μΑ	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output High Leakage Current				50	μΑ	Max	$V_{OUT} = V_{CC}$
V <sub>ID</sub>	Input Leakage Test		4.75			V	0.0	$I_{ID} = 1.9 \mu A$
			4.75			•	0.0	All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current				3.75	μΑ	0.0	V <sub>IOD</sub> = 150 mV
								All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$
Ios	Output Short-Circuit Current		-60		-150	mA	Max	$V_{OUT} = 0V$
I <sub>CCL</sub>	Power Supply Current			12	20	mA	Max	$V_O = LOW$

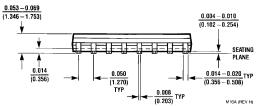
#### **AC Electrical Characteristics**

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_{A} = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = +5.0V$ $C_{L} = 50 \text{ pF}$		Units	
		Min	Тур	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	4.5	8.1	10.5	4.5	12.0	ns	
t <sub>PHL</sub>	S <sub>n</sub> to Z <sub>n</sub>	3.5	7.0	9.0	3.5	10.5	115	
t <sub>PLH</sub>	Propagation Delay	4.5	7.1	9.0	4.5	10.5	ns	
t <sub>PHL</sub>	$\overline{E}_n$ to $Z_n$	3.0	5.7	7.0	2.5	8.0		
t <sub>PLH</sub>	Propagation Delay	3.0	5.3	7.0	3.0	8.0	ns	
t <sub>PHL</sub>	I <sub>n</sub> to Z <sub>n</sub>	2.5	5.1	6.5	2.5	7.5	ns	

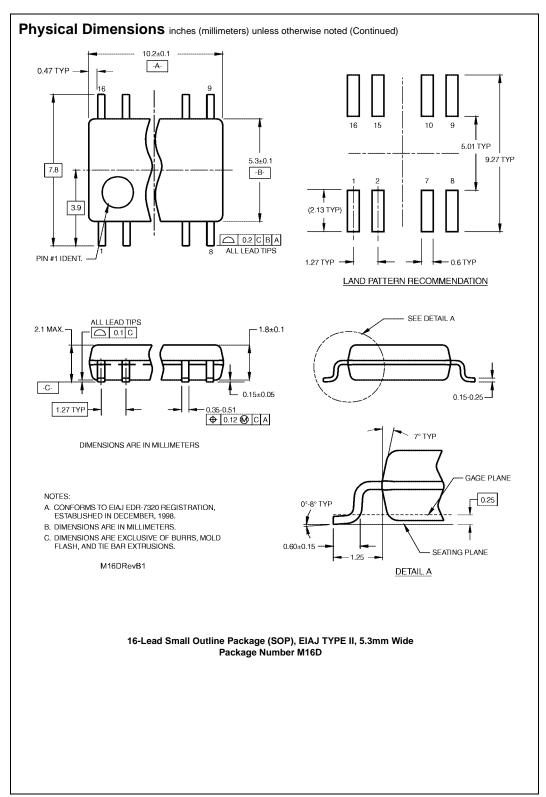
# Physical Dimensions inches (millimeters) unless otherwise noted



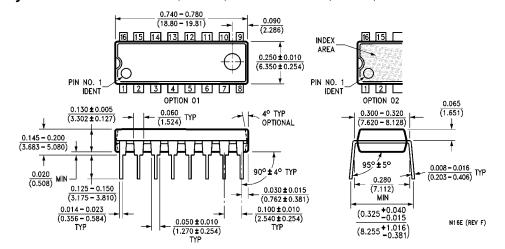




16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A



#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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