Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

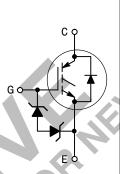
N-Channel Enhancement-Mode Silicon Gate

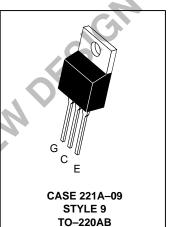
This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Its new 600 V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{\text{CE(on)}}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. Co–packaged IGBTs save space, reduce assembly time and cost. This new E–series introduces an energy efficient, ESD protected, and rugged short circuit device.

- Industry Standard TO–220 Package
- High Speed: E_{off} = 60 μJ per Amp typical at 125°C
- High Voltage Short Circuit Capability 10 μs minimum at 125°C, 400 V
- Low On-Voltage 2.0 V typical at 8.0 A
- Soft Recovery Free Wheeling Diode is included in the Package
- Robust High Voltage Termination
- ESD Protection Gate-Emitter Zener Diodes

MGP11N60ED

IGBT & DIODE IN TO-220 11 A @ 90°C 15 A @ 25°C 600 VOLTS SHORT CIRCUIT RATED LOW ON-VOLTAGE





MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V _{CES}	600	Vdc
Collector–Gate Voltage ($R_{GE} = 1.0 \text{ M}\Omega$)	V _{CGR}	600	Vdc
Gate-Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T _C = 25°C — Continuous @ T _C = 90°C — Repetitive Pulsed Current (1)	I _{C25} I _{C90} I _{CM}	15 11 22	Adc Apk
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	96 0.77	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t _{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{ heta JC} \ R_{ heta JC} \ R_{ heta JA}$	1.3 2.3 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

⁽¹⁾ Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Ch	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown V (V _{GE} = 0 Vdc, I _C = 250 µAdc)	V _{(BR)CES}	600	_	_	Vdc	
Temperature Coefficient (Positiv		_	870	_	mV/°C	
Zero Gate Voltage Collector Curre ($V_{CE} = 600 \text{ Vdc}$, $V_{GE} = 0 \text{ Vdc}$) ($V_{CE} = 600 \text{ Vdc}$, $V_{GE} = 0 \text{ Vdc}$, T	I _{CES}	_ _	_ _	10 200	μAdc	
Gate-Body Leakage Current (V _{GE}	$= \pm 20$ Vdc, $V_{CE} = 0$ Vdc)	I _{GES}	_	_	50	μAdc
ON CHARACTERISTICS (1)						•
Collector-to-Emitter On-State Voltage (V_{GE} = 15 Vdc, I_{C} = 4.0 Adc) (V_{GE} = 15 Vdc, I_{C} = 4.0 Adc, T_{J} = 125°C) (V_{GE} = 15 Vdc, I_{C} = 8.0 Adc)			_ _ _	1.6 1.5 2.0	1.9 — 2.4	Vdc
Gate Threshold Voltage $(V_{CE} = V_{GE}, I_C = 1.0 \text{ mAdc})$ Threshold Temperature Coefficient (Negative)			4.0 —	6.0 10	8.0 —	Vdc mV/°C
Forward Transconductance (V _{CE} =	= 10 Vdc, I _C = 8.0 Adc)	9 _{fe}	_	3.5	_	Mhos
DYNAMIC CHARACTERISTICS			A . \$			
Input Capacitance		C _{ies}		779	_	pF
Output Capacitance	$(V_{CE} = 25 \text{ Vdc}, V_{GE} = 0 \text{ Vdc}, f = 1.0 \text{ MHz})$	C _{oes}	TV	81	_	
Transfer Capacitance		C _{res}		13	_	
SWITCHING CHARACTERISTICS	(1)	N				
Turn-On Delay Time		t _{d(on)}	_	46	_	ns
Rise Time		t _r	_	34	_	
Turn-Off Delay Time	$(V_{CC} = 360 \text{ Vdc}, I_{C} = 8.0 \text{ Adc},$	t _{d(off)}	_	102	_	
Fall Time	$V_{GE} = 15 \text{ Vdc}, L = 300 \mu\text{H}, \\ R_{G} = 20 \Omega)$	t _f	_	226	_	
Turn-Off Switching Loss	Energy losses include "tail"	E _{off}	_	0.32	0.40	mJ
Turn-On Switching Loss		E _{on}	_	0.11	_	
Total Switching Loss		E _{ts}	_	0.43	_	
Turn-On Delay Time		t _{d(on)}	_	42	_	ns
Rise Time		t _r	_	26	_	
Turn-Off Delay Time	$(V_{CC} = 360 \text{ Vdc}, I_{C} = 8.0 \text{ Adc},$	t _{d(off)}	_	214	_	
Fall Time	$V_{GE} = 15 \text{ Vdc}, L = 300 \mu\text{H}$ $R_G = 20 \Omega, T_J = 125^{\circ}\text{C}$	t _f	_	228	_	
Turn-Off Switching Loss	Energy losses include "tail"	E _{off}	_	0.48	_	mJ
Turn-On Switching Loss	**	E _{on}	_	0.16	_	1
Total Switching Loss		E _{ts}	_	0.64	_	1
Gate Charge		Q _T	_	39.2	_	nC
	$(V_{CC} = 360 \text{ Vdc}, I_{C} = 8.0 \text{ Adc}, V_{GE} = 15 \text{ Vdc})$	Q ₁	_	8.7	_	1
	Q ₂	_	17.4	_	1	
DIODE CHARACTERISTICS		1				
Diode Forward Voltage Drop ($I_{EC} = 3.25 \text{ Adc}$) ($I_{EC} = 3.25 \text{ Adc}$, $T_{J} = 125^{\circ}\text{C}$) ($I_{EC} = 6.5 \text{ Adc}$)		V _{FEC}	_ _ 1.7	1.63 1.24 2.0	_ _ 2.3	Vdc

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — **continued** (T_J = 25°C unless otherwise noted)

Char	Symbol	Min	Тур	Max	Unit		
DIODE CHARACTERISTICS — continued							
Reverse Recovery Time		t _{rr}	_	57	_	ns	
	$(I_F = 8.0 \text{ Adc}, V_R = 360 \text{ Vdc}, \\ dI_F/dt = 200 \text{ A/}\mu\text{s})$	ta	_	18	_		
		t _b	_	39	_		
Reverse Recovery Stored Charge		Q _{RR}	_	107	_	μC	
Reverse Recovery Time		t _{rr}	_	91	_	ns	
	$(I_F = 8.0 \text{ Adc}, V_R = 360 \text{ Vdc}, \\ dI_F/dt = 200 \text{ A/}\mu\text{s}, T_J = 125^{\circ}\text{C})$	ta	_	28	_		
		t _b	_	63	_		
Reverse Recovery Stored Charge		Q _{RR}	_	275	_	μC	
NTERNAL PACKAGE INDUCTANCE							
Internal Emitter Inductance (Measured from the emitter lead 0.25" from package to emitter bond pad)		L _E	_	7.5		nH	

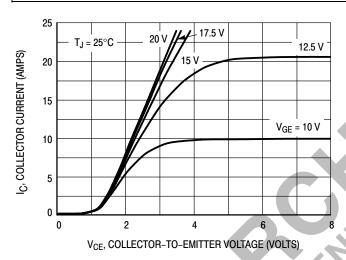


Figure 1. Output Characteristics

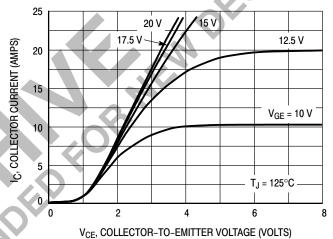


Figure 2. Output Characteristics

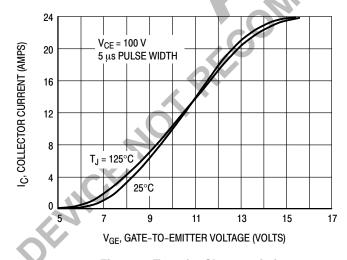


Figure 3. Transfer Characteristics

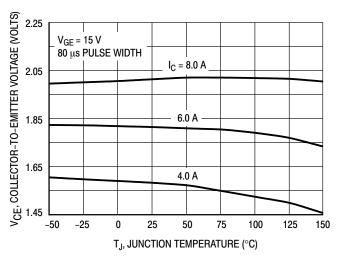


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

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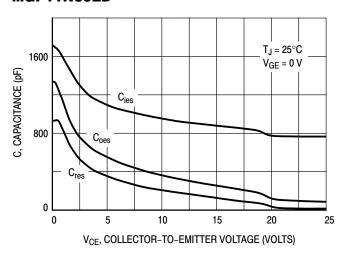


Figure 5. Capacitance Variation

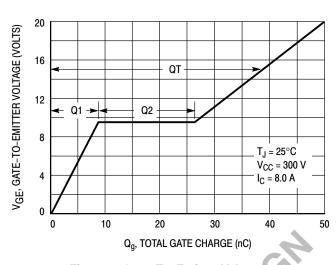


Figure 6. Gate-To-Emitter Voltage versus
Total Charge

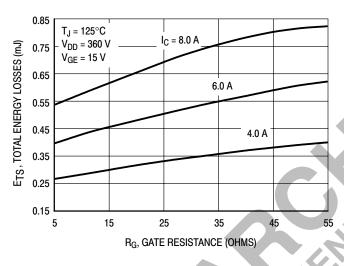


Figure 7. Total Energy Losses versus
Gate Resistance

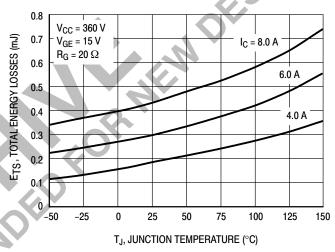


Figure 8. Total Energy Losses versus Junction Temperature

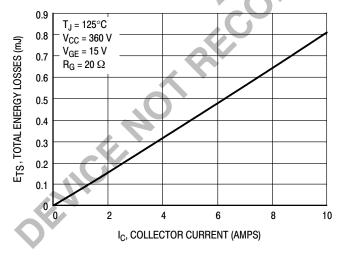


Figure 9. Total Energy Losses versus Collector Current

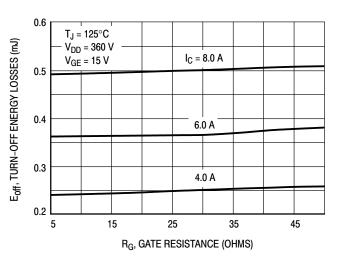


Figure 10. Turn-Off Losses versus
Gate Resistance

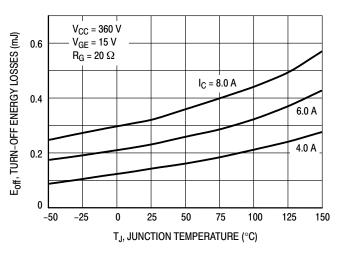


Figure 11. Turn-Off Losses versus Junction Temperature

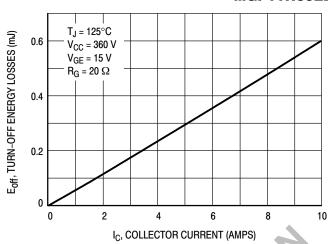


Figure 12. Turn-Off Losses versus
Collector Current

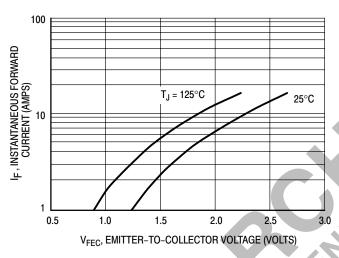


Figure 13. Forward Characteristics versus Current

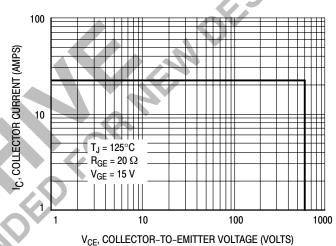
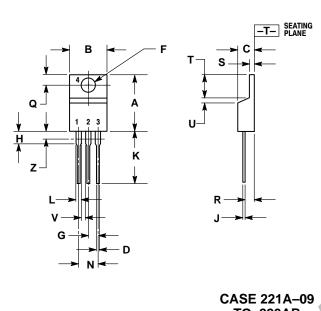


Figure 14. Reverse Biased Safe Operating Area

PACKAGE DIMENSIONS



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI
- CONTROLLING DIMENSION: INCH. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.570	0.620	14.48	15.75	
В	0.380	0.405	9.66	10.28	
С	0.160	0.190	4.07	4.82	
D	0.025	0.035	0.64	0.88	
F	0.142	0.147	3.61	3.73	
G	0.095	0.105	2.42	2.66	
Н	0.110	0.155	2.80	3.93	
J	0.018	0.025	0.46	0.64	
K	0.500	0.562	12.70	14.27	
L	0.045	0.060	1.15	1.52	
N	0.190	0.210	4.83	5.33	
Q	0.100	0.120	2.54	3.04	
R	0.080	0.110	2.04	2.79	
S	0.045	0.055	1.15	1.39	
T	0.235	0.255	5.97	6.47	
U	0.000	0.050	0.00	1.27	
٧	0.045		1.15		
Z		0.080		2 04	

- STYLE 9:
 PIN 1. GATE
 2. COLLECTOR
 2 EMITTER
 3 SCITOF

TO-220AB **ISSUE Z**

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