

# FCH35N60

## N-Channel SuperFET® MOSFET

600 V, 35 A, 98 mΩ



### Features

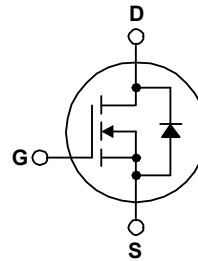
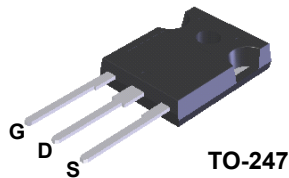
- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 79\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 139\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 340\text{ pF}$ )
- 100% Avalanche Tested

### Application

- Solar Inverter
- AC-DC Power Supply

### Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCH35N60	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	35
		- Continuous ( $T_C = 100^\circ\text{C}$ )	22.2
$I_{DM}$	Drain Current	- Pulsed (Note 1)	105
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	1455
$I_{AR}$	Avalanche Current	(Note 1)	35
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	31.25
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	20
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	312.5
		- Derate above $25^\circ\text{C}$	2.5
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\*Drain current limited by maximum junction temperature.

### Thermal Characteristics

Symbol	Parameter	FCH35N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	42	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH35N60	FCH35N60	TO-247	-	-	30

## Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 25°C	600	-	-	V
		I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150°C	-	650	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	-	0.6	-	V/°C
BV <sub>DS</sub>	Drain-Source Avalanche Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 16 A	-	700	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°C	-	-	10	
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V	-	-	±100	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 17.5 A	-	0.079	0.098	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 17.5 A	-	28.8	-	S

### Dynamic Characteristics

C <sub>iSS</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V f = 1 MHz	-	4990	6640	pF
C <sub>oss</sub>	Output Capacitance		-	2380	3170	pF
C <sub>rSS</sub>	Reverse Transfer Capacitance		-	140	-	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	-	113	-	pF
C <sub>oss eff.</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V	-	340	-	pF
Q <sub>g</sub>	Total Gate Charge at 10V	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 35 A V <sub>GS</sub> = 10 V (Note 4)	-	139	181	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		-	31	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		-	69	-	nC
ESR	Equivalent Series Resistance (G-S)		Drain Open, F = 1 MHz	-	1.4	-

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 35 A R <sub>G</sub> = 4.7 Ω (Note 4)	-	34	78	ns
t <sub>r</sub>	Turn-On Rise Time		-	120	250	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	105	220	ns
t <sub>f</sub>	Turn-Off Fall Time		-	73	155	ns

### Drain-Source Diode Characteristics

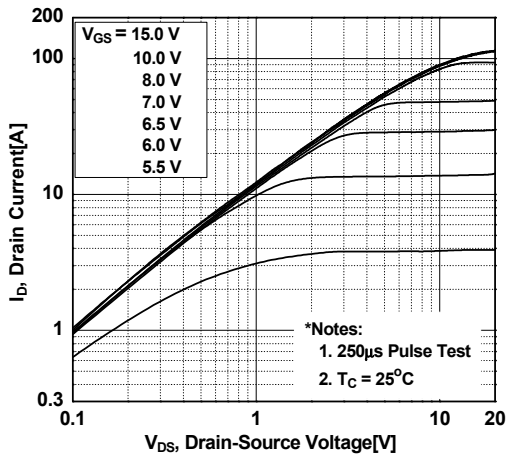
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current	-	-	35	A	
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current	-	-	105	A	
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 35 A	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 35 A	-	614	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di <sub>F</sub> /dt = 100 A/μs	-	16.3	-	μC

#### Notes:

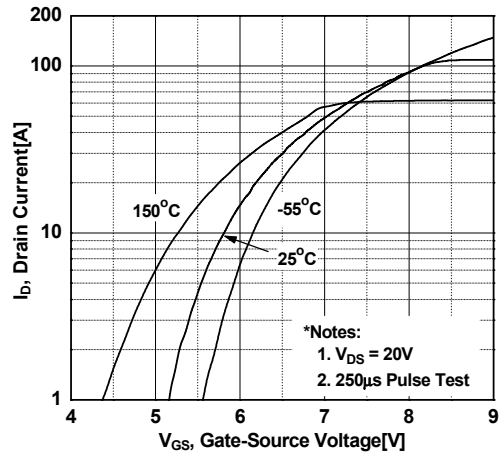
- 1: Repetitive Rating; Pulse-width limited by maximum junction temperature.
- 2: I<sub>AS</sub> = 17.5 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C
- 3: I<sub>SD</sub> ≤ 35 A, di<sub>F</sub>/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C
- 4: Essentially independent of operating temperature.

## Typical Characteristics

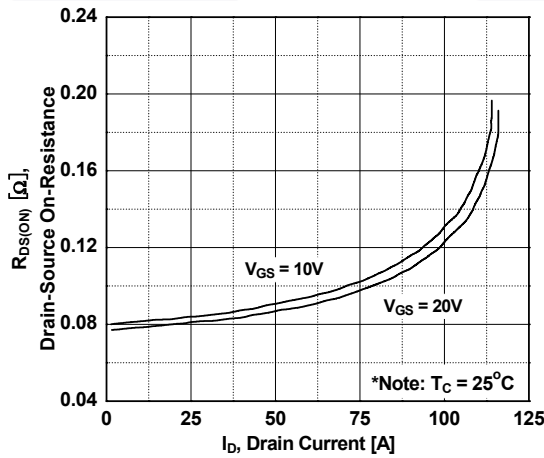
**Figure 1. On-Region Characteristics**



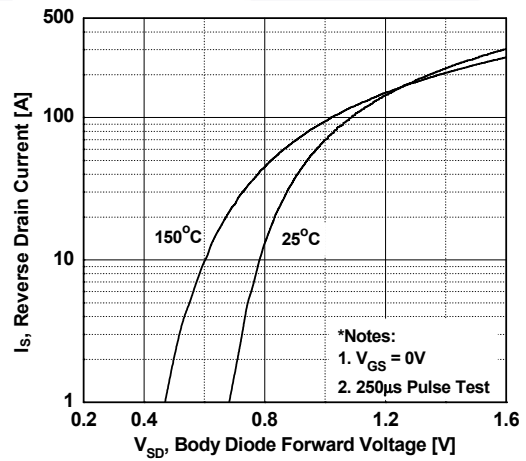
**Figure 2. Transfer Characteristics**



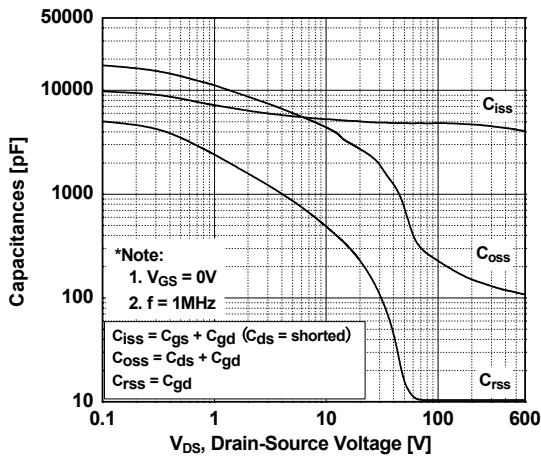
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



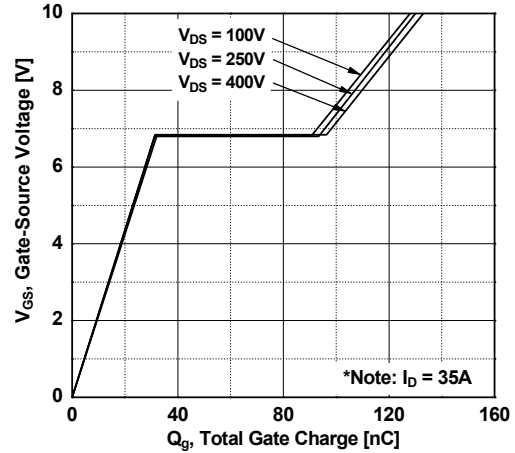
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

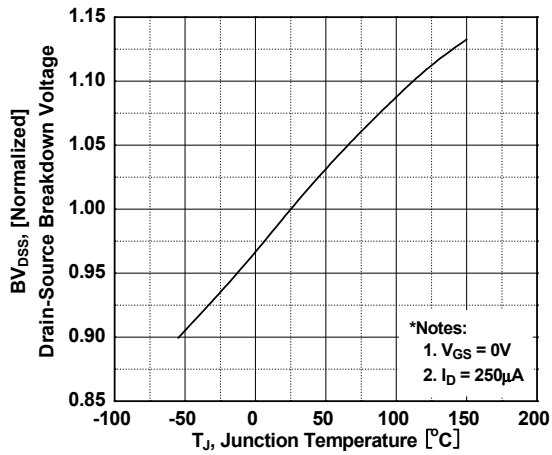


Figure 8. On-Resistance Variation vs. Temperature

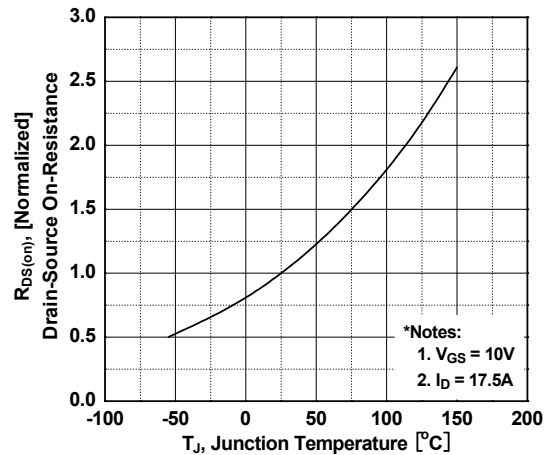


Figure 9. Maximum Safe Operating Area

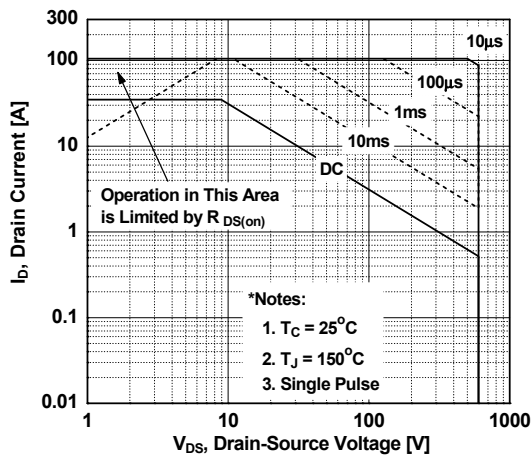


Figure 10. Maximum Drain Current vs. Case Temperature

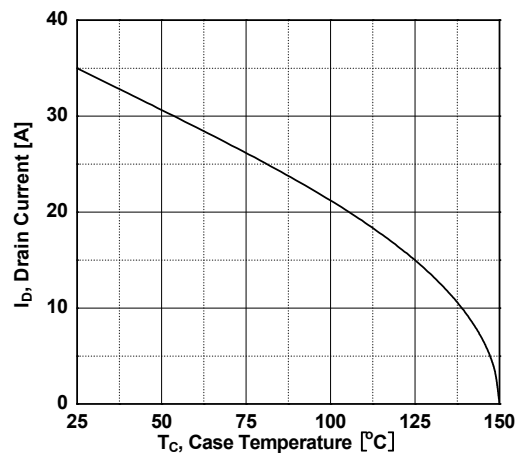


Figure 11. Transient Thermal Response Curve

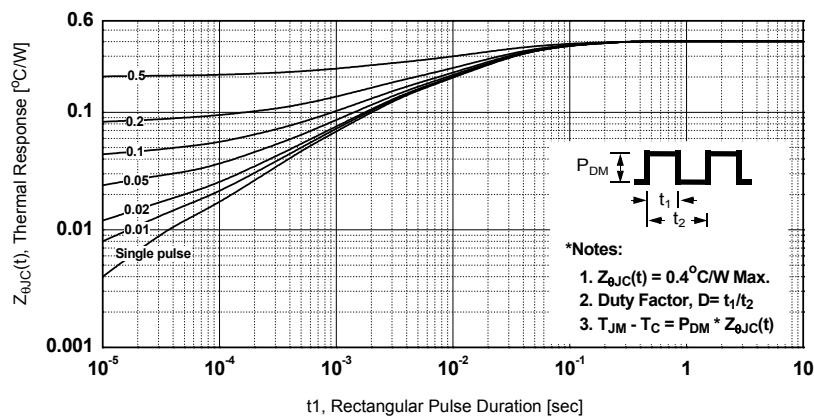


Figure 12. Gate Charge Test Circuit & Waveform

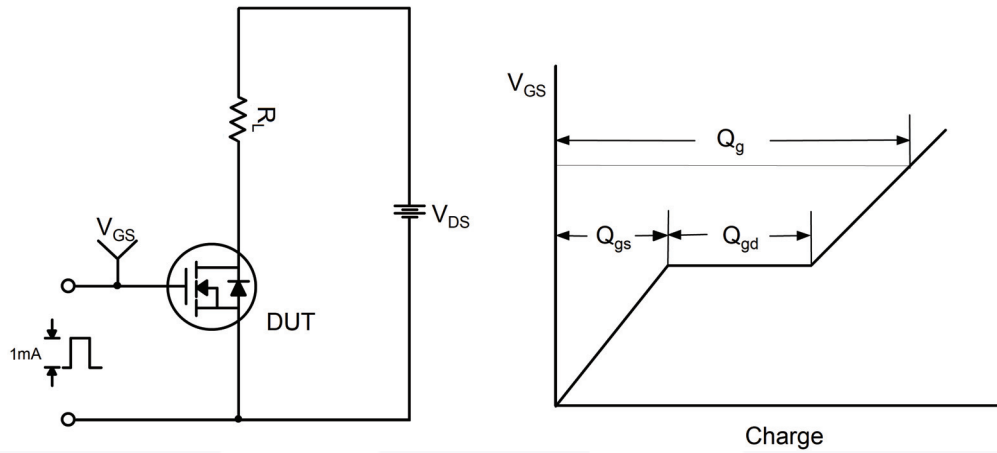


Figure 13. Resistive Switching Test Circuit & Waveforms

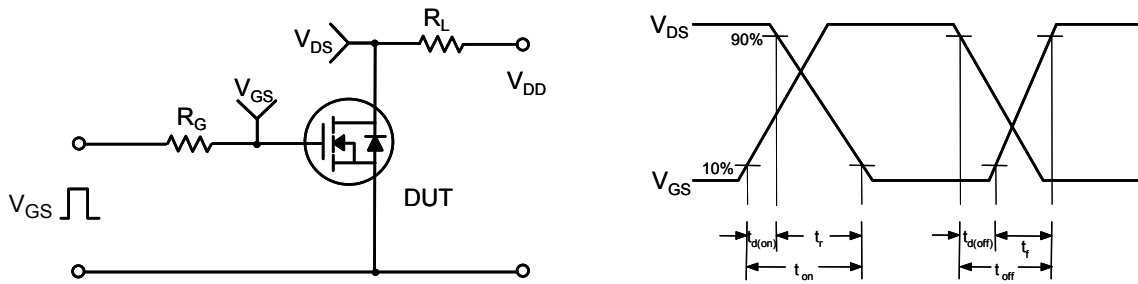


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

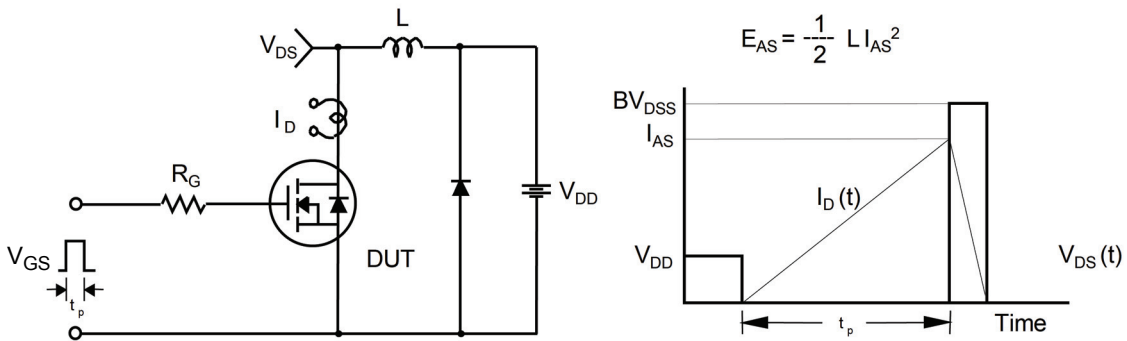
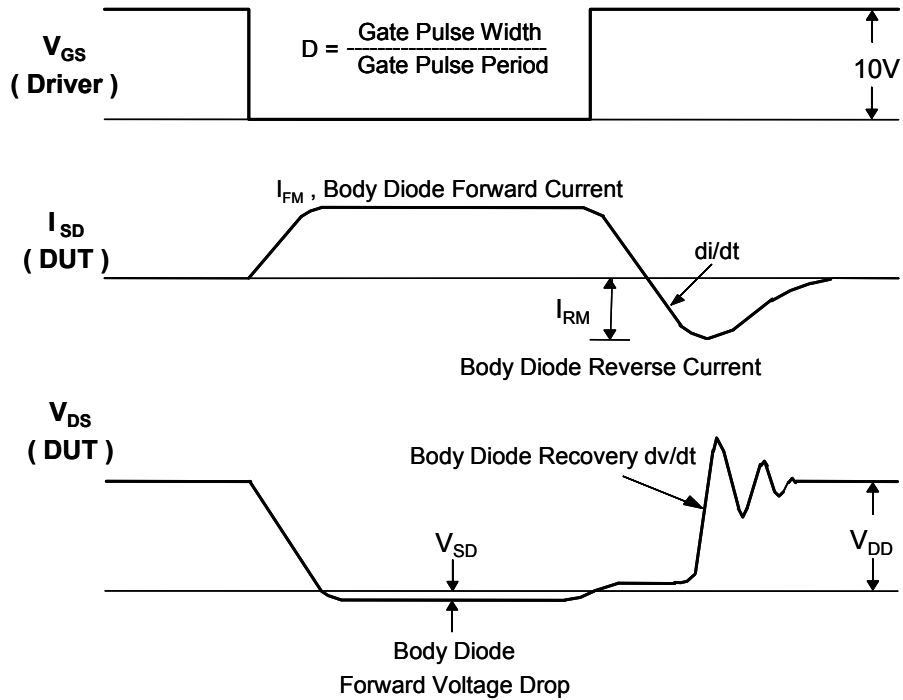
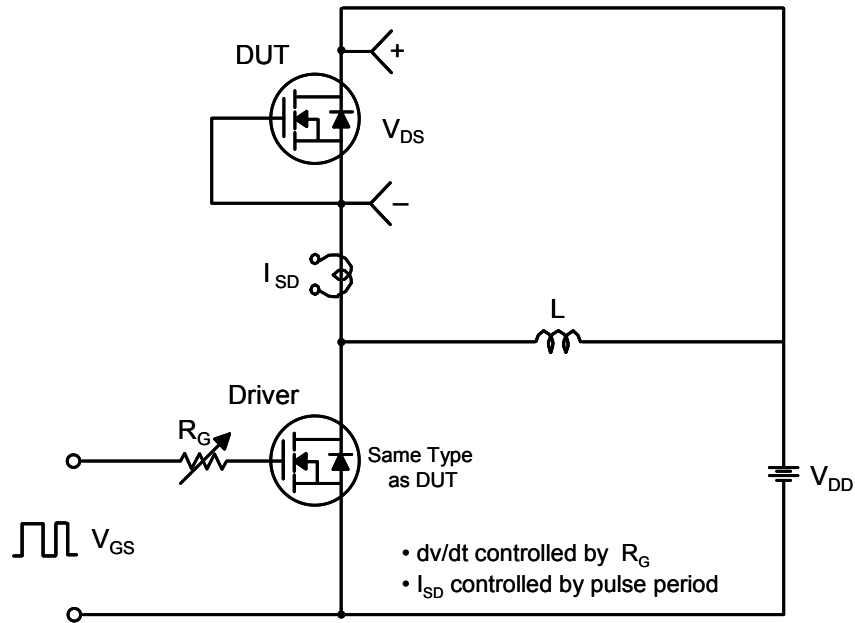
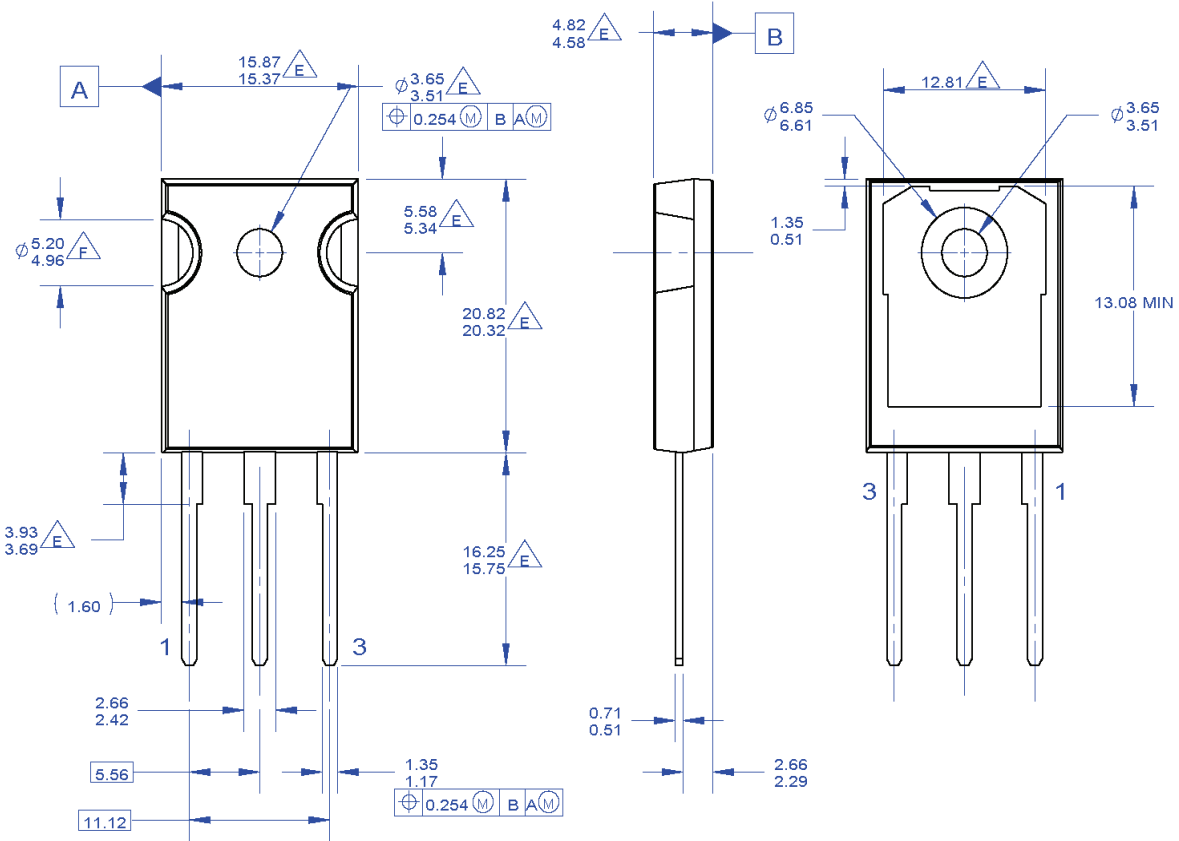


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Mechanical Dimensions

### TO-247 3L



NOTES: UNLESS OTHERWISE SPECIFIED.

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**Figure ... TO-247, Molded, 3 Lead, Jedec Variation AB**

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| CTL™                     | GTO™  | TinyPower™  |
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