Recent Additions
CD54AC299/3A
CD54ACT299/3A

8-Input Universal Shift/Storage Register with Common Parallel I/O pins

Asynchronous Reset

The RCA CD54AC299 and CD54ACT299 are 3-state, 8-input universal shift/storage registers with common parallel I/O pins. These devices utilize the new RCA ADVANCED CMOS LOGIC technology. These registers have four synchronous-operating modes controlled by the two select inputs as shown in the Mode Select (S0, S1) table. The Mode Select, the Serial Data (DS0, DS7), and the Parallel Data (I/O_0 - I/O_7) respond only to the LOW-TO-HIGH transition of the clock pulse (CP). S0, S1 and Data inputs must be present one setup time prior to the positive transition of the clock.

The Master Reset ($\overline{MR}$) is an asynchronous active-LOW input. When $\overline{MR}$ is LOW, the register is cleared regardless of the status of all other inputs. The register can be expanded by cascading same units by tying the serial output (QO) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DS0) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DS0 of the first stage.

The 3-state input/output (I/O) port has three modes of operation:

1. Both Output Enable ($\overline{OE1}$ and $\overline{OE2}$) inputs are LOW and S0 or S1 or both are LOW, the data in the register is present at the eight outputs.
2. When both S0 and S1 are HIGH, I/O terminals are in the high-impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of $\overline{OE1}$ and $\overline{OE2}$.
3. Either one of the two Output Enable inputs being HIGH will force I/O terminals to be in the off state. It is noted that each I/O terminal is a 3-state output and a CMOS buffer input.

The CD54AC299 and CD54ACT299 are supplied in 20-lead dual-in-line ceramic packages (F suffix).

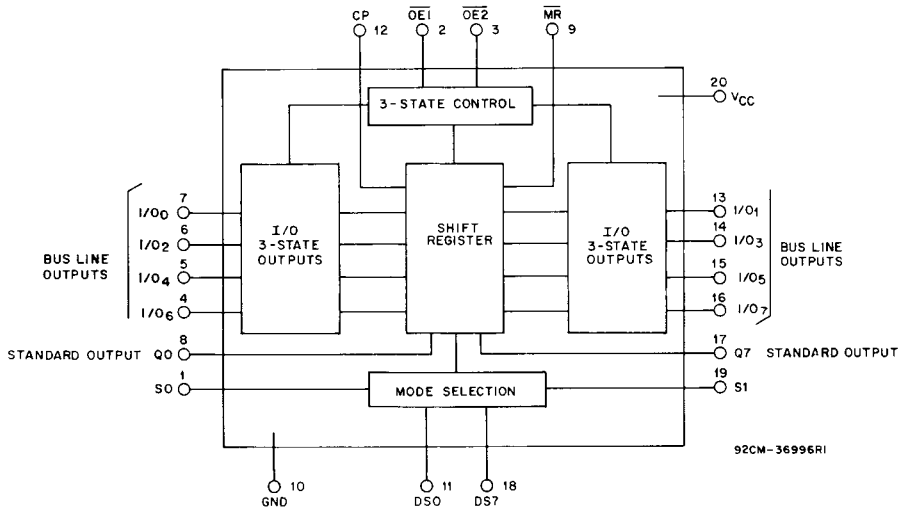

Fig. 1 - Functional diagram.

Package Specifications

(See Section 11, Fig. 13)

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CD54ACT299/3A

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				+25		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	
Quiescent Supply Current (MSI) I_{CC}	V_{CC} or GND	0	5.5	—	8•	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
S1, S2, $\overline{OE1}$, $\overline{OE2}$	0.83
SL, CP	0.67
$\overline{MR}$	1.33

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections

Identical to CD54HC/HCT299/3A, page 5-121.

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: CP to Q0, Q7	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 3.4 2.2	162 18.1 12.9•	ns
$\overline{CP}$ to (I/O)n	t_{PLH} t_{PHL}	1.5 3.3 5	— 3.5 2.3	169 18.9 13.5•	ns
$\overline{MR}$ to Q0, Q7	t_{PLH} t_{PHL}	1.5 3.3 5	— 2.9 1.9	140 15.7 11.2•	ns
$\overline{MR}$ to (I/O)n	t_{PLH} t_{PHL}	1.5 3.3 5	— 3.5 2.4	174 19.5 13.9	ns
Enable and Disable Times	t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	1.5 3.3 5	— 3.8 2.6	186 22.4 14.9•	ns
Power Dissipation Capacitance	C_{PD}§	—			pF
Input Capacitance	C_I	—	—	10	pF
3-State Output Capacitance	C_O	—	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption per function.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

(Limits with black dots (•) are tested 100%.)

Recent Additions
CD54AC299/3A
CD54ACT299/3A

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125° C		UNITS
			MIN.	MAX.	
Propagation Delays: CP to Q0, Q7	t_{PLH} t_{PHL}	5†	2.2	12.9•	ns
CP to (I/O)n	t_{PLH} t_{PHL}	5	2.5	14.5•	ns
$\overline{MR}$ to Q0, Q7	t_{PLH} t_{PHL}	5	2.1	12.2•	ns
$\overline{MR}$ to (I/O)n	t_{PLH} t_{PHL}	5	3.2	18.6	ns
Enable Disable Times	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	2.6	14.9•	ns
Power Dissipation Capacitance	C_{PD}§	—			pF
Input Capacitance	C_I	—	—	10	pF
3-State Output Capacitance	C_O	—	—	15	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

(Limits with black dots (•) are tested 100%.)

§C_{PD} is used to determine the dynamic power consumption, per function.
For ACT, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

CD54AC323/3A
CD54ACT323/3A

8-Input Universal Shift/Storage Register with Common Parallel I/O pins

Synchronous Reset

The RCA CD54AC323 and CD54ACT323 are 3-state, 8-input universal shift/storage registers with common parallel I/O pins. These devices utilize the new RCA ADVANCED CMOS LOGIC technology. These registers have four synchronous-operating modes controlled by the two select inputs as shown in the Mode Select (S0, S1) table. The Mode Select, the Serial Data (DS0, DS7), and the Parallel Data (I/O_0 - I/O_7) respond only to the LOW-TO-HIGH transition of the clock pulse (CP). S0, S1 and Data inputs must be present one setup time prior to the positive transition of the clock.

The Master Reset ($\overline{MR}$) clears the register in sync with the clock input. The register can be expanded by cascading same units by tying the serial output (QO) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DS0) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DS0 of the first stage.

The 3-state input/output (I/O) port has three modes of operation:

1. Both Output Enable ($\overline{OE1}$ and $\overline{OE2}$) inputs are LOW and S0 or S1 or both are LOW, the data in the register is present at the eight outputs.
2. When both S0 and S1 are HIGH, I/O terminals are in the high-impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of $\overline{OE1}$ and $\overline{OE2}$.
3. Either one of the two Output Enable inputs being HIGH will force I/O terminals to be in the off state. It is noted that each I/O terminal is a 3-state output and a CMOS buffer input.

The CD54AC323 and CD54ACT323 are supplied in 20-lead dual-in-line ceramic packages (F suffix).