



MPEG Clock Generator with VCXO

Features

- Integrated phase-locked loop (PLL)
- Low-jitter, high-accuracy outputs
- VCXO with analog adjust
- 3.3V operation
- Compatible with MK3727 (-1, -4, -5, -6, -7)

- Application compatibility for a wide variety of designs
- Enables design compatibility
- Advanced Features
- Serial programming interface (CY2410-3 only)
- Lower drive strength settings (CY2410-4, -6)
- Matches nonlinear MK3727A VCXO control curve (-5, -6)
- Matches nonlinear MK3727C VCXO control curve (-7)

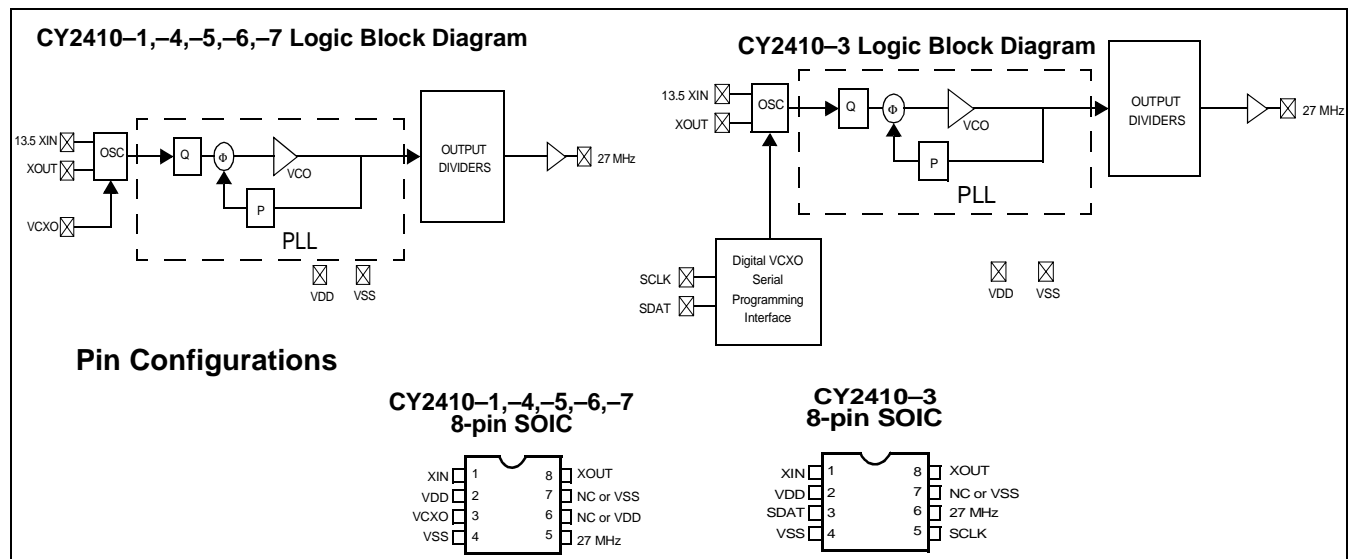
Benefits

- Highest-performance PLL tailored for multimedia applications
- Meets critical timing requirements in complex system designs
- Large ± 150 -ppm range, better linearity

Benefits

- Digital VCXO control
- Electromagnetic interference (EMI) reduction for standards compliance
- Second source for existing designs

| Part Number | Outputs | Input Frequency Range | Output Frequencies | VCXO Control Curve | Other Features |
|-------------|---------|---|--------------------|--------------------|---|
| CY2410-1 | 1 | 13.5-MHz pullable crystal input per Cypress specification | 1 copy of 27 MHz | linear | Compatible with MK3727 |
| CY2410-3 | 1 | 13.5-MHz pullable crystal input per Cypress specification | 1 copy of 27 MHz | linear | Serial programming interface |
| CY2410-4 | 1 | 13.5-MHz pullable crystal input per Cypress specification | 1 copy of 27 MHz | linear | Same as CY2410-1 except lower drive strength settings |
| CY2410-5 | 1 | 13.5-MHz pullable crystal input per Cypress specification | 1 copy of 27 MHz | nonlinear | Matches MK3727A nonlinear VCXO Control Curve |
| CY2410-6 | 1 | 13.5-MHz pullable crystal input per Cypress specification | 1 copy of 27 MHz | nonlinear | Same as CY2410-5 except lower drive strength |
| CY2410-7 | 1 | 13.5-MHz pullable crystal input per Cypress specification | 1 copy of 27 MHz | nonlinear | Matches MK3727C nonlinear VCXO control curve |



Pin Descriptions for CY2410–1, –4, –5, –6, –7

| Name | Pin Number | Description |
|---------------------------------|------------|---|
| X _{IN} | 1 | Reference crystal input |
| V _{DD} | 2 | Voltage supply |
| V _{CXO} | 3 | Input analog control for V _{CXO} |
| V _{SS} | 4 | Ground |
| 27 MHz | 5 | 27-MHz clock output |
| NC/V _{DD} | 6 | No Connect or voltage supply |
| NC/V _{SS} | 7 | No Connect or ground |
| X _{OUT} ^[1] | 8 | Reference crystal output |

Pin Description for CY2410–3

| Name | Pin Number | Description |
|---------------------------------|------------|-------------------------------------|
| X _{IN} | 1 | Reference crystal input |
| V _{DD} | 2 | Voltage supply |
| SDAT | 3 | Serial data input for DCXO control |
| V _{SS} | 4 | Ground |
| SCLK | 5 | Serial clock input for DCXO control |
| 27 MHz | 6 | 27-MHz clock output |
| NC/V _{SS} | 7 | No Connect or ground |
| X _{OUT} ^[1] | 8 | Reference crystal output |

Pullable Crystal Specifications^[2]

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|--------------------------------|--|---|------|------|------|------|
| F _{NOM} | Nominal crystal frequency | Parallel resonance, fundamental mode, AT cut | – | 13.5 | – | MHz |
| C _{LNOM} | Nominal load capacitance | | – | 14 | – | pF |
| R ₁ | Equivalent series resistance (ESR) | Fundamental mode | – | – | 25 | Ω |
| R ₃ /R ₁ | Ratio of third overtone mode ESR to fundamental mode ESR | Ratio used because typical R ₁ values are much less than the maximum spec. | 3 | – | – | |
| DL | Crystal drive level | No external series resistor assumed | – | 0.5 | 2.0 | mW |
| F _{3SEPHI} | Third overtone separation from 3*F _{NOM} | High side | 300 | – | – | ppm |
| F _{3SEPLO} | Third overtone separation from 3*F _{NOM} | Low side | – | – | –150 | ppm |
| C ₀ | Crystal shunt capacitance | | – | – | 7 | pF |
| C ₀ /C ₁ | Ratio of shunt to motional capacitance | | 180 | – | 250 | |
| C ₁ | Crystal motional capacitance | | 14.4 | 18 | 21.6 | pF |

Notes:

1. Float X_{OUT} if X_{IN} is externally driven.
2. Crystals that meet this specification includes: Ecliptek ECX-5788-13.500M, Siward XTL001050A-13.5-14-400, Raltron A-13.500-14-CL, PDI HA13500XFSA14XC.

Serial Programmable Interface Protocol

The CY2410-3 utilizes a two-wire-interface SDAT and SCLK that operates up to 400 kbits/sec in Read or Write mode. The basic Write serial format is as follows: start bit; 7-bit device address (DA); R/W bit; slave clock acknowledge (ACK); 8-bit memory address (MA); ACK; 8-bit data; ACK; 8-bit data in MA+1 if desired; ACK; 8-bit data in MA+2; ACK; etc. until stop bit, as illustrated in Figure 1.

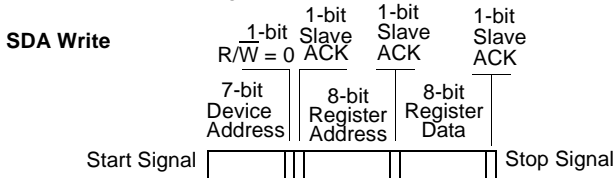


Figure 1. Data Frame Architecture

Data Valid

Data is valid when the clock is HIGH, and may only be transitioned when the clock is low as illustrated in Figure 2.

Data Frame

Every new data frame is indicated by a start and stop sequence, as illustrated in Figure 3.

Start Sequence

A start frame is indicated by SDAT going LOW when SCLK is HIGH. Every time a start signal is given, the next 8-bit data must be the device address (7 bits) and a R/W bit (0 for Write), followed by register address (8 bits) and register data (8 bits). See Figure 3.

Stop Sequence

A stop frame is indicated by SDAT going HIGH when SCLK is HIGH. A stop frame frees the bus for writing to another part on the same bus or writing to another random register address. See Figure 3.

Acknowledge Pulse

During Write mode, the CY2410-3 will respond with an ACK pulse after every 8 bits. This is accomplished by pulling the SDAT line LOW during the next clock cycle after the eighth bit is shifted in.

Device Address

The 7-bit device address is 1101001.

Register Address

The 8-bit address for the VCXO register is 00010011.

Register Data

The register data can be any value between 00H–FFH. As you increase the value, the capacitance on the X_{IN} and X_{OUT} pins will increase, thereby decreasing the xtal frequency.

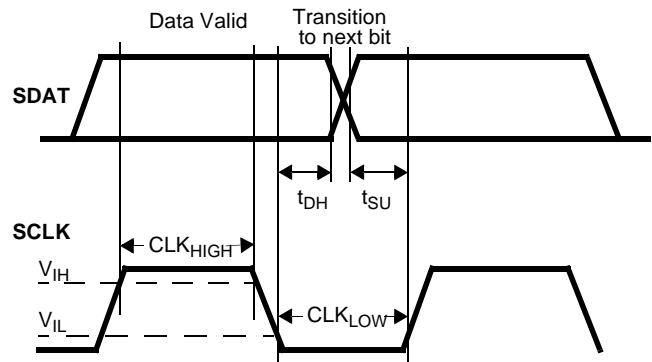


Figure 2. Data Valid and Data Transition Periods

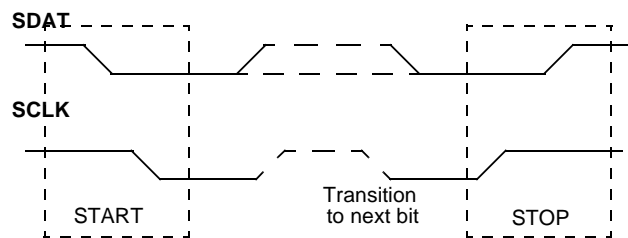


Figure 3. Start and Stop Frame

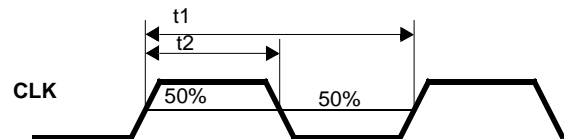


Figure 4. Duty Cycle Definition; $DC = t_2/t_1$

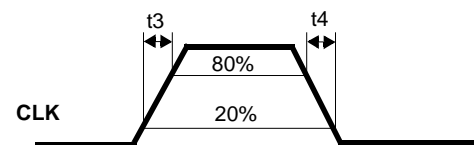


Figure 5. Rise and Fall Time Definitions: $ER = 0.6 \times V_{DD} / t_3$, $EF = 0.6 \times V_{DD} / t_4$

Absolute Maximum Conditions

| Parameter | Description | Min. | Max. | Unit |
|-----------|--------------------------------------|----------------|----------------|------|
| V_{DD} | Supply Voltage | -0.5 | 7.0 | V |
| T_S | Storage Temperature ^[3] | -65 | 125 | °C |
| T_J | Junction Temperature | - | 125 | °C |
| | Digital Inputs | $V_{SS} - 0.3$ | $V_{DD} + 0.3$ | V |
| | Digital Outputs referred to V_{DD} | $V_{SS} - 0.3$ | $V_{DD} + 0.3$ | V |
| | Electrostatic Discharge | 2000 | | V |

Recommended Operating Conditions

| Parameter | Description | Min. | Typ. | Max. | Unit |
|------------|--|-------|------|-------|------|
| V_{DD} | Operating Voltage | 3.135 | 3.3 | 3.465 | V |
| T_A | Ambient Temperature | 0 | - | 70 | °C |
| C_{LOAD} | Max. Load Capacitance | - | - | 15 | pF |
| f_{REF} | Reference Frequency | - | 13.5 | - | MHz |
| t_{PU} | Power up time for V_{DD} to reach minimum specified voltage (power ramp must be monotonic) | 0.05 | - | 500 | ms |

DC Electrical Specifications

| Parameter | Name | Description | Min. | Typ. | Max. | Unit |
|-----------------|--|--|------|------|----------|------|
| I_{OH} | Output HIGH Current -1,3,5,7 | $V_{OH} = V_{DD} - 0.5, V_{DD} = 3.3V$ | 12 | 24 | - | mA |
| I_{OL} | Output LOW Current -1,3,5,7 | $V_{OL} = 0.5, V_{DD} = 3.3V$ | 12 | 24 | - | mA |
| I_{OH} | Output HIGH Current -4,6 | $V_{OH} = V_{DD} - 0.5, V_{DD} = 3.3V$ | 6 | 18 | - | mA |
| I_{OL} | Output LOW Current -4,6 | $V_{OL} = 0.5, V_{DD} = 3.3V$ | 6 | 18 | - | mA |
| C_{IN} | Input Capacitance | | - | - | 7 | pF |
| I_{IZ} | Input Leakage Current | | - | 5 | - | μA |
| $f_{\Delta XO}$ | V_{CXO} pullability range:-1,-3,-4,-5,-6 | | ±150 | - | - | ppm |
| | V_{CXO} pullability range:-7 | | ±115 | - | - | ppm |
| V_{VCXO} | V_{CXO} input range | | 0 | - | V_{DD} | V |
| I_{VDD} | Supply Current | | - | 30 | 35 | mA |

AC Electrical Specifications ($V_{DD} = 3.3V$)^[4]

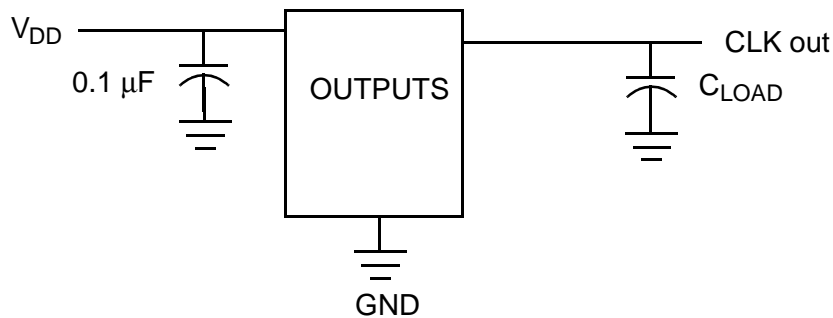
| Parameter ^[4] | Name | Description | Min. | Typ. | Max. | Unit |
|--------------------------|----------------------------------|---|------|------|------|------|
| DC | Output Duty Cycle | Duty Cycle is defined in <i>Figure 4</i> , 50% of V_{DD} | 45 | 50 | 55 | % |
| ER_{OR} | Rising Edge Rate -1, -3, -5, -7 | Output Clock Edge Rate, Measured from 20% to 80% of V_{DD} , $C_{LOAD} = 15$ pF See <i>Figure 5</i> . | 0.8 | 1.4 | - | V/ns |
| ER_{OF} | Falling Edge Rate -1, -3, -5, -7 | Output Clock Edge Rate, Measured from 80% to 20% of V_{DD} , $C_{LOAD} = 15$ pF See <i>Figure 5</i> . | 0.8 | 1.4 | - | V/ns |
| ER_{OR} | Rising Edge Rate -4, -6 | Output Clock Edge Rate, Measured from 20% to 80% of V_{DD} , $C_{LOAD} = 15$ pF See <i>Figure 5</i> . | 0.7 | 1.1 | - | V/ns |
| ER_{OF} | Falling Edge Rate -4, -6 | Output Clock Edge Rate, Measured from 80% to 20% of V_{DD} , $C_{LOAD} = 15$ pF See <i>Figure 5</i> . | 0.7 | 1.1 | - | V/ns |
| t_g | Clock Jitter -1, -3, -5, -7 | Peak-to-peak period jitter | - | 140 | - | ps |
| t_g | Clock Jitter -4, -6 | Peak-to-peak period jitter | - | 150 | - | ps |
| t_{10} | PLL Lock Time | | - | - | 3 | ms |

Notes:

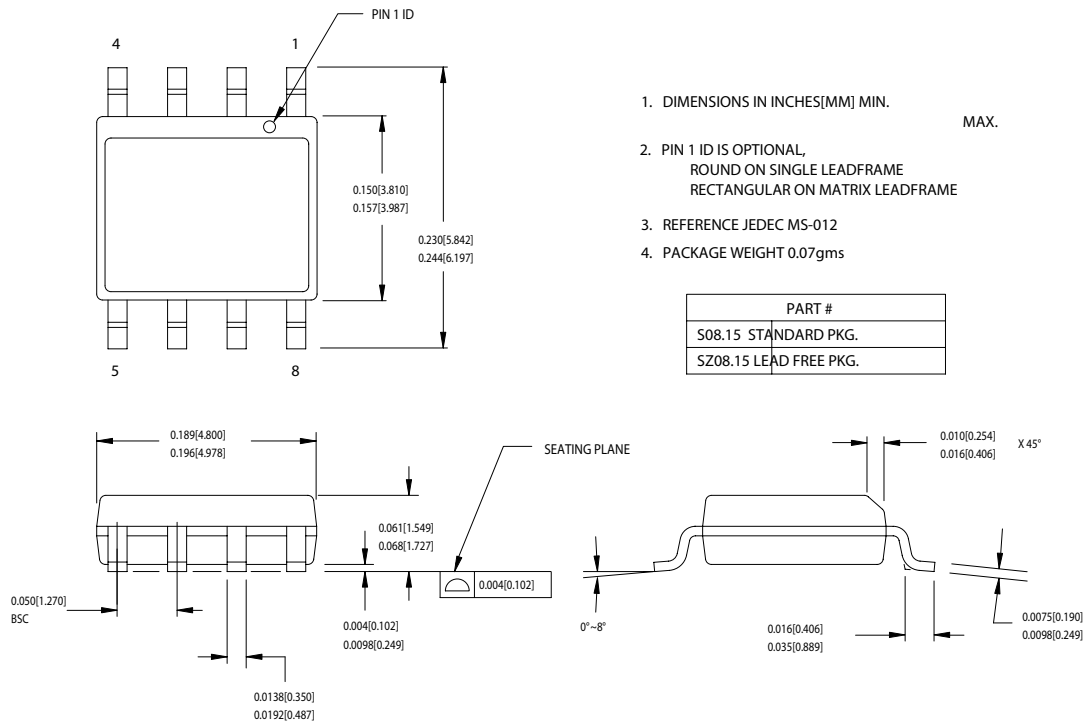
3. Rated for ten years.
4. Not 100% tested.

Serial Programming Interface Timing Specifications

| Parameter | Description | Min. | Max. | Unit |
|--------------|---|------|------|---------|
| f_{SCL} | Frequency of SCLK | | 400 | kHz |
| | Start mode time from SDAT LOW to SCLK LOW | 0.6 | | μ S |
| CLK_{LOW} | SCLK LOW period | 1.3 | | μ S |
| CLK_{HIGH} | SCLK HIGH period | 0.6 | | μ S |
| t_{SU} | Data transition to SCLK HIGH | 100 | | ns |
| t_{DH} | Data hold (SCLK LOW to data transition) | 0 | | ns |
| | Rise time of SCLK and SDAT | | 300 | ns |
| | Fall time of SCLK and SDAT | | 300 | ns |
| | Stop mode time from SCLK HIGH to SDA HIGH | 0.6 | | μ s |
| | Stop mode to start mode | 1.3 | | μ s |

Test and Measurement Set-up

Ordering Information

| Ordering Code | Package Type | Operating Range | Operating Voltage | Features |
|---------------|----------------------------|-----------------|-------------------|--|
| CY2410SC-1 | 8-pin SOIC | Commercial | 3.3V | Linear VCXO control curve |
| CY2410SC-1T | 8-pin SOIC - Tape and Reel | Commercial | 3.3V | Linear VCXO control curve |
| CY2410SC-3 | 8-pin SOIC | Commercial | 3.3V | Digital VCXO control |
| CY2410SC-3T | 8-pin SOIC - Tape and Reel | Commercial | 3.3V | Digital VCXO control |
| CY2410SC-4 | 8-pin SOIC | Commercial | 3.3V | Lower drive strength (reduced EMI) |
| CY2410SC-4T | 8-pin SOIC - Tape and Reel | Commercial | 3.3V | Lower drive strength (reduced EMI) |
| CY2410SC-5 | 8-pin SOIC | Commercial | 3.3V | Matches nonlinear MK3727A VCXO control curve |
| CY2410SC-5T | 8-pin SOIC - Tape and Reel | Commercial | 3.3V | Matches nonlinear MK3727A VCXO control curve |
| CY2410SC-6 | 8-pin SOIC | Commercial | 3.3V | Lower drive strength version of CY2410-5 |
| CY2410SC-6T | 8-pin SOIC - Tape and Reel | Commercial | 3.3V | Lower drive strength version of CY2410-5 |
| CY2410SC-7 | 8-pin SOIC | Commercial | 3.3V | Matches MK3727C nonlinear VCXO control curve |
| CY2410SC-7T | 8-pin SOIC - Tape and Reel | Commercial | 3.3V | Matches MK3727C nonlinear VCXO control curve |

Package Drawing and Dimensions
8-lead (150-Mil) SOIC S8


51-85066-°C

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Document History Page

| Document Title: CY2410 MPEG Clock Generator with VCXO | | | | |
|---|---------|------------|-----------------|---|
| Document Number: 38-07317 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 111553 | 02/12/02 | CKN | New Data Sheet |
| *A | 114937 | 09/24/02 | CKN | Added -6 to data sheet, Advance Information to Final |
| *B | 121418 | 12/06/02 | CKN | Updated the Pullable Crystal Specifications table on page 2 |
| *C | 126905 | 06/17/03 | RGL | Added -7 part to data sheet Added new parameter on the Pullable Crystal table Power-up requirements added to the operating conditions |
| *D | 131100 | 01/20/03 | RGL | Added VCXO -7 pullability range in the DC Specs with min. value of ± 115 ppm |