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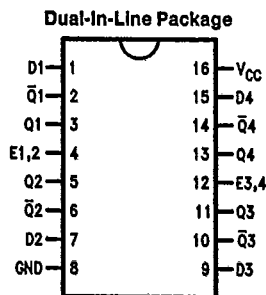
## 54LS375/DM74LS375 4-Bit Latch

### General Description

The 'LS375 is a 4-bit D-type latch for use as temporary storage for binary information between processing units and input/output or indicator units. When its Enable (E) input is HIGH, a latch is transparent, i.e., the Q output will follow the

D input each time it changes. When E is LOW a latch stores the last valid data present on the D input preceding the HIGH-to-LOW transition of E. The 'LS375 is functionally identical to the 'LS75 except for the corner power pins.

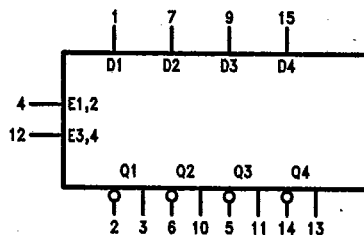
### Connection Diagram



TL/F/9830-1

Order Number 54LS375DMQB,  
54LS375FMQB, DM74LS375M or DM74LS375N  
See NS Package Number  
J16A, M16A, N16E or W16A

### Logic Symbol



TL/F/9830-2

V<sub>CC</sub> = Pin 16  
GND = Pin 8

Pin Name	Description
D1-D4	Data Inputs
E1, 2	Latches 1, 2 Enable Inputs
E3, 4	Latches 3, 4 Enable Inputs
Q1-Q4	Latch Outputs
$\bar{Q}1$ -Q4	Complementary Latch Outputs

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LS375

**Absolute Maximum Ratings** (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	-55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	54LS375			DM74LS375			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.7			0.8	V
I <sub>OH</sub>	High Level Output Current			-0.4			-0.4	mA
I <sub>OL</sub>	Low Level Output Current			4			8	mA
T <sub>A</sub>	Free Air Operating Temperature	-55		125	0		70	°C
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW D <sub>n</sub> to E <sub>n</sub>	20			20			ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time HIGH or LOW D <sub>n</sub> to E <sub>n</sub>	0			0			ns
t <sub>w</sub> (H)	E <sub>n</sub> Pulse Width HIGH	20			15			ns

**Electrical Characteristics**

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max, V <sub>IL</sub> = Max	54LS 2.5			V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max, V <sub>IH</sub> = Min	54LS		0.4	V
			DM74	0.35	0.5	
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min	DM74	0.25	0.4	
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 10V			0.1	mA
		Enable Input			0.4	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V			20	μA
		Enable Input			80	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			-0.4	mA
		Enable Input			-1.2	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	54LS	-20	-100	mA
			DM74	-20	-100	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max			12	mA

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.



**Switching Characteristics**

V<sub>CC</sub> = +5.0V, T<sub>A</sub> = +25°C (See Section 1 for waveforms and load configurations)

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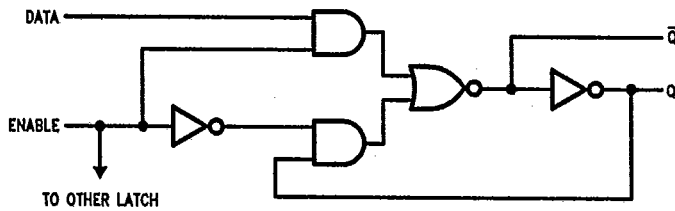
Symbol	Parameter	54LS/DM74LS		Units
		C <sub>L</sub> = 15 pF		
		Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D <sub>n</sub> to Q <sub>n</sub>		27 23	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D <sub>n</sub> to $\bar{Q}_n$		20 15	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay E <sub>n</sub> to Q <sub>n</sub>		27 25	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay E <sub>n</sub> to $\bar{Q}_n$		30 18	ns

**Truth Table** (Each Latch)

t <sub>n</sub>	t <sub>n+1</sub>
D	Q
H	H
L	L

t<sub>n</sub> = Bit time before Enable negative going transition.  
 t<sub>n+1</sub> = Bit time after Enable negative going transition.  
 H = HIGH Voltage Level  
 L = LOW Voltage Level

**Logic Diagram** (1/4 of diagram shown)



TL/F/9830-3