

DM7490A

Decade and Binary Counter

The DM7490A monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The counter has a gated zero reset and also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate Function Table. A symmetrical divide-by-ten count can be obtained from the counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A .

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY



August 1986 Revised July 2001

DM7490A Decade and Binary Counter

General Description

The DM7490A monolithic counter contains four masterslave flip-flops and additional gating to provide a divide-bytwo counter and a three-stage binary counter for which the count cycle length is divide-by-five.

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To use the maximum count length (decade or four-bit binary), the B input is connected to the \mathbf{Q}_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate Function Table. A symmetrical divide-by-ten count can be obtained from the counters by connecting the \mathbf{Q}_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output \mathbf{Q}_A .

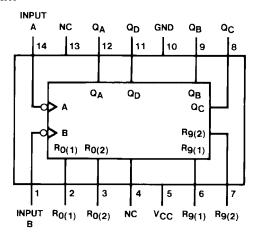
Features

- Typical power dissipation 145 mW
- Count frequency 42 MHz

Ordering Code:

Order Number	Package Number	Package Description			
DM7490AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide			

Connection Diagram



Function Tables

BCD Count Sequence (Note 1)

Count		Out	puts	
Count	Q_D	Q _C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	Н
2	L	L	Н	L
3	L	L	Н	Н
4	L	Н	L	L
5	L	Н	L	Н
6	L	Н	Н	L
7	L	Н	Н	Н
8	Н	L	L	L
9	Н	L	L	Н

BCD Bi-Quinary (5-2) (Note 2)

Count	Outputs						
Count	Q_A	Q_D	Q _C	Q _B			
0	L	L	L	L			
1	L	L	L	Н			
2	L	L	Н	L			
3	L	L	Н	Н			
4	L	Н	L	L			
5	Н	L	L	L			
6	Н	L	L	Н			
7	Н	L	Н	L			
8	Н	L	Н	Н			
9	Н	Н	L	L			

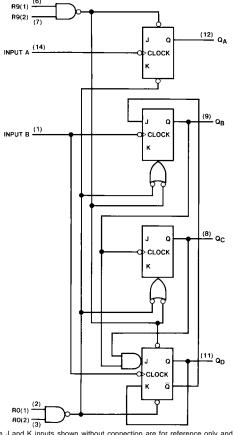
Reset/Count Function Table

Reset Inputs					Out	puts	
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q _C	QB	Q_A
Н	Н	L	Х	L	L	L	L
Н	Н	Χ	L	L	L	L	L
Х	X	Н	Н	Н	L	L	Н
Х	L	Χ	L	COUNT			
L	X	L	Χ	COUNT			
L	X	X	L	COUNT			
Х	L	L	Χ	COUNT			

Note 1: Output QA is connected to input B for BCD count.

Note 2: Output QD is connected to input A for bi-quinary count

Logic Diagram



The J and K inputs shown without connection are for reference only and are functionally at a HIGH level.

H = HIGH Level L = LOW Level X = Don't Care

Absolute Maximum Ratings(Note 3)

Supply Voltage 7V Input Voltage 5.5V Operating Free Air Temperature Range 0°C to +70°C Storage Temperature Range $-65^{\circ}\text{C to} +150^{\circ}\text{C}$

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parame	Min	Nom	Max	Units	
V _{CC}	Supply Voltage		4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltag	е	2			V
V _{IL}	LOW Level Input Voltag	е			8.0	V
I _{OH}	HIGH Level Output Current				-0.8	mA
I _{OL}	LOW Level Output Curre	ent			16	mA
f _{CLK}	Clock Frequency	Α	0		32	MHz
	(Note 4)	В	0		16	IVITZ
t _W	Pulse Width	Α	15			
	(Note 4)	В	30			ns
		Reset	15			
t _{REL}	Reset Release Time (Note 4)		25			ns
T _A	Free Air Operating Temperature		0		70	°C

Note 4: $T_A = 25^{\circ}C$ and $V_{CC} = 5V$.

DC Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -12 \text{ mA}$				-1.5	V
V _{OH}	HIGH Level	V _{CC} = Min, I _{OH} = Max		2.4	3.4		V
	Output Voltage	V _{IL} = Max, V _{IH} = Min		2.4	3.4		V
V _{OL}	LOW Level	V _{CC} = Min, I _{OL} = Max			0.2	0.4	V
	Output Voltage	V _{IH} = Min, V _{IL} = Max (Note 6)			0.2	0.4	V
l _l	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V				1	mA
I _{IH}	HIGH Level	V _{CC} = Max	A			80	
	Input Current	$V_I = 2.7V$	Reset			40	μΑ
			В			120	
I _{IL}	LOW Level	V _{CC} = Max	Α			-3.2	
	Input Current	$V_I = 0.4V$	Reset			-1.6	mA
			В			-4.8	
los	Short Circuit Output Current	V _{CC} = Max (Note 7)	•	-18		-57	mA
I _{CC}	Supply Current	V _{CC} = Max (Note 8)			29	42	mA

Note 5: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 6: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Note 7: Not more than one output should be shorted at a time.

Note 8: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

AC Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^{\circ}C$

Symbol	Parameter	From (Input)	R _L = 4000	$R_L = 400\Omega$, $C_L = 15 pF$		
Symbol		To (Output)	Min	Max	Units	
f _{MAX}	Maximum Clock	A to Q _A	32		MII-	
	Frequency	B to Q _B	16		MHz	
t _{PLH}	Propagation Delay Time	A to 0		16		
	LOW-to-HIGH Level Output	A to Q _A	16		ns	
t _{PHL}	Propagation Delay Time	A to 0		10		
	HIGH-to-LOW Level Output	A to Q _A		18	ns	
t _{PLH}	Propagation Delay Time	A to 0		48		
	LOW-to-HIGH Level Output	A to Q _D		40	ns	
t _{PHL}	Propagation Delay Time	A to Q _D		50	ne	
	HIGH-to-LOW Level Output	A to QD	50		ns	
t _{PLH}	Propagation Delay Time	D (+ 0		16	no	
	LOW-to-HIGH Level Output	B to Q _B	10		ns	
t _{PHL}	Propagation Delay Time	B to Q _B		21	no	
	HIGH-to-LOW Level Output	B to Q _B			ns	
t _{PLH}	Propagation Delay Time	B to Q _C		32	no	
	LOW-to-HIGH Level Output	B to QC		32	ns	
t _{PHL}	Propagation Delay Time	B to Q _C		25	no	
	HIGH-to-LOW Level Output	B to QC		35	ns	
t _{PLH}	Propagation Delay Time	B to Q _D		32	ns	
	LOW-to-HIGH Level Output	B to Q _D		32	115	
t _{PHL}	Propagation Delay Time	B to Q _D		35	ns	
	HIGH-to-LOW Level Output	B to Q _D		33	115	
t _{PLH}	Propagation Delay Time	SET-9 to Q _A , Q _D		30	no	
	LOW-to-HIGH Level Output	3E1-9 to QA, QD		30	ns	
t _{PHL}	Propagation Delay Time	SET-9 to Q _B , Q _C		40	ns	
	HIGH-to-LOW Level Output	3E1-9 10 AB, AC		40	115	
t _{PHL}	Propagation Delay Time	SET-0		40	ns	
	HIGH-to-LOW Level Output	Any Q		40		

Physical Dimensions inches (millimeters) unless otherwise noted 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 0.250 + 0.010 (6.350±0.254) PIN NO. 1 IDENT PIN NO. 1 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ $\frac{0.300 - 0.320}{(7.620 - 8.128)}$ 0.065 0.145 - 0.2000.060 4° TYP OPTIONAL (1.651) (1.524) (3.683 - 5.080)0.008 - 0.016 TYP 95° ± 5° 0.020 (0.203 - 0.406)(0.508) MIN 0.125 - 0.150 0.075 ± 0.015 (3.175 - 3.810) 0.280 (1.905 ± 0.381) (7.112) MIN 0.014 -- 0.023 TYP $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)} \text{ TYP}$ 0.325 ^{+0.040} -0.015 $8.255 + 1.016 \\ -0.381$ N14A (REV F)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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