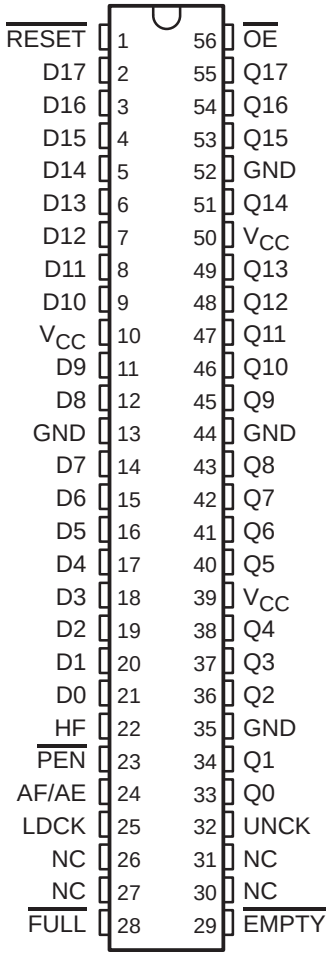
- **Member of the Texas Instruments Widebus™ Family**
- **Load Clock and Unload Clock Can Be Asynchronous or Coincident**
- **64 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Full, Empty, and Half-Full Flags**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Fast Access Times of 15 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates up to 50 MHz**
- **3-State Outputs**
- **Pin-to-Pin Compatible With SN74ACT7804 and SN74ACT7806**
- **Packaged in Shrink Small-Outline 300-mil Package Using 25-mil Center-to-Center Spacing**

DL PACKAGE
(TOP VIEW)



description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7814 is a 64-word by 18-bit FIFO for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 64. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

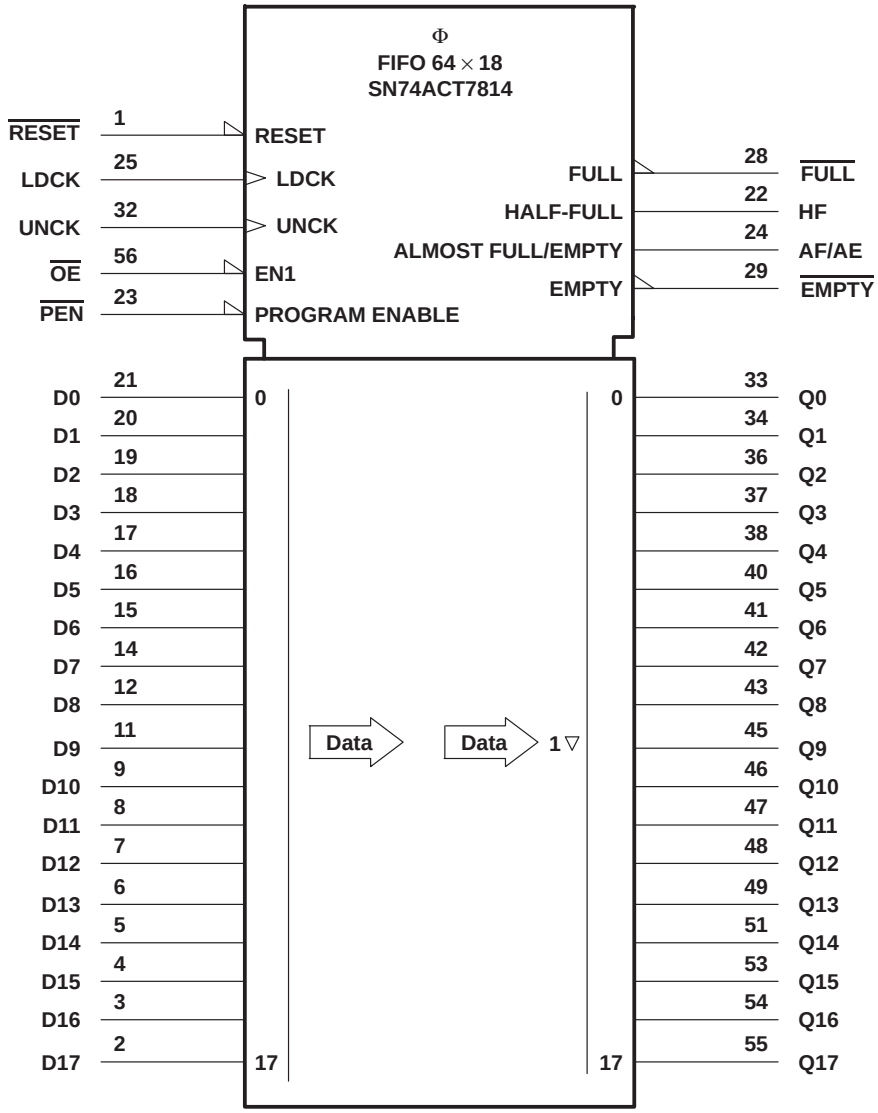
Status of the FIFO memory is monitored by the full ($\overline{\text{FULL}}$), empty ($\overline{\text{EMPTY}}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The HF output is high when the FIFO contains 32 or more words and is low when it contains 31 or fewer words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{\text{PEN}}$) is low. The AF/AE flag is high when the FIFO contains X or fewer words or (64 – Y) or more words. The AF/AE flag is low when the FIFO contains between (X + 1) and (63 – Y) words.

description (continued)

A low level on the reset ($\overline{\text{RESET}}$) input resets the internal stack pointers and sets $\overline{\text{FULL}}$ high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up. The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. The data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable ($\overline{\text{OE}}$) input is high.

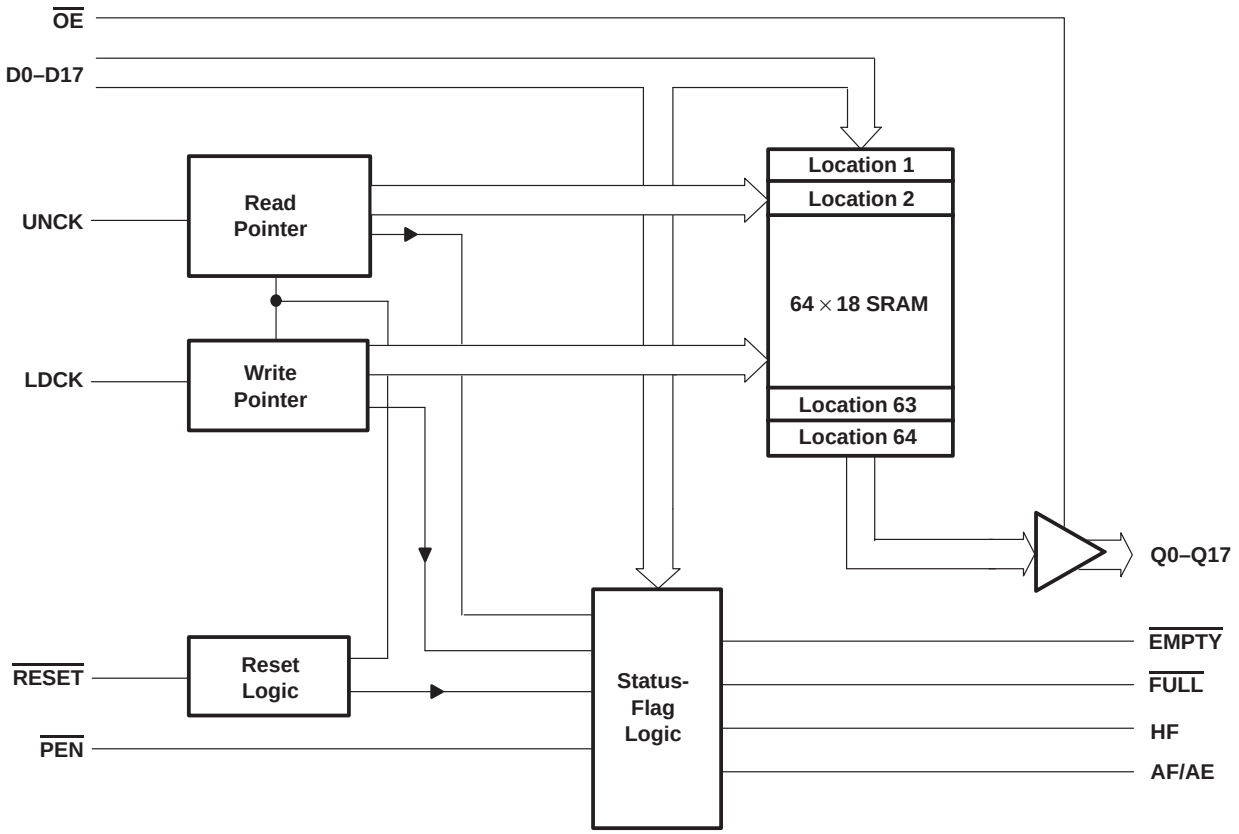
The SN74ACT7814 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth-offset values can be programmed for AF/AE, or the default value of 8 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or fewer words or (64 – Y) or more words. AF/AE is high after reset.
D0–D17	2–9, 11–12, 14–21	I	18-bit data input port
$\overline{\text{EMPTY}}$	29	O	Empty flag. $\overline{\text{EMPTY}}$ is high when the FIFO memory is not empty; $\overline{\text{EMPTY}}$ is low when the FIFO memory is empty or upon assertion of $\overline{\text{RESET}}$.
$\overline{\text{FULL}}$	28	O	Full flag. $\overline{\text{FULL}}$ is high when the FIFO memory is not full or upon assertion of $\overline{\text{RESET}}$; $\overline{\text{FULL}}$ is low when the FIFO memory is full.
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 32 or more words. HF is low after reset.
LDCK	25	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
$\overline{\text{OE}}$	56	I	Output enable. When $\overline{\text{OE}}$ is high, the data outputs are in the high-impedance state.
$\overline{\text{PEN}}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D4 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port
$\overline{\text{RESET}}$	1	I	Reset. A low level on $\overline{\text{RESET}}$ resets the FIFO and drives $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	32	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.

offset values for AF/AE

The AF/AE flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag is high when the FIFO contains X or fewer words or (64 – Y) or more words.

To program the offset values, $\overline{\text{PEN}}$ can be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0–D4 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D4 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 31 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 8, $\overline{\text{PEN}}$ must be held high.

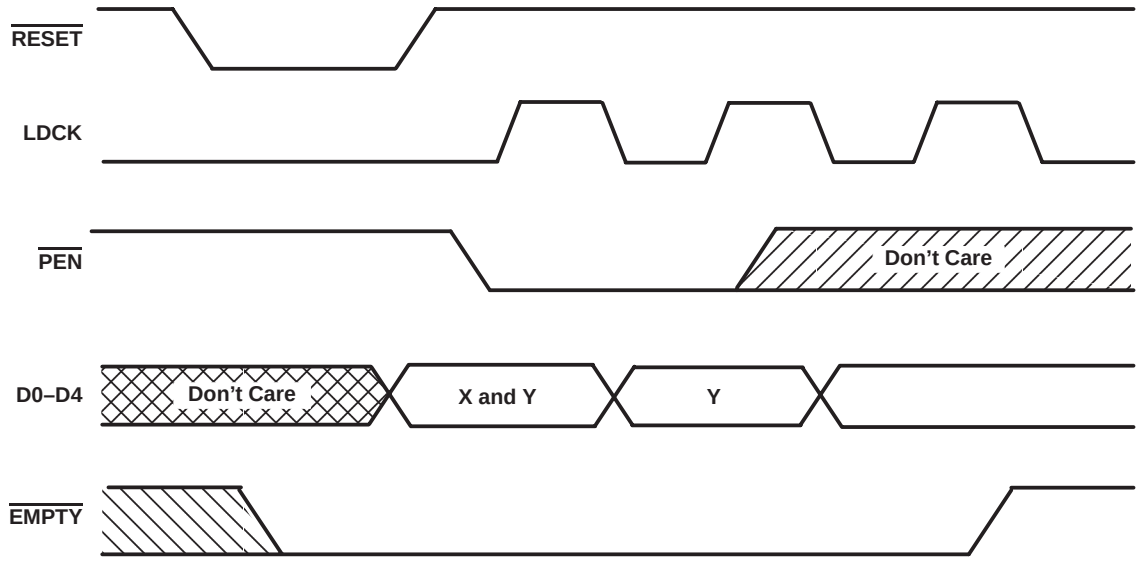


Figure 1. Programming X and Y Separately

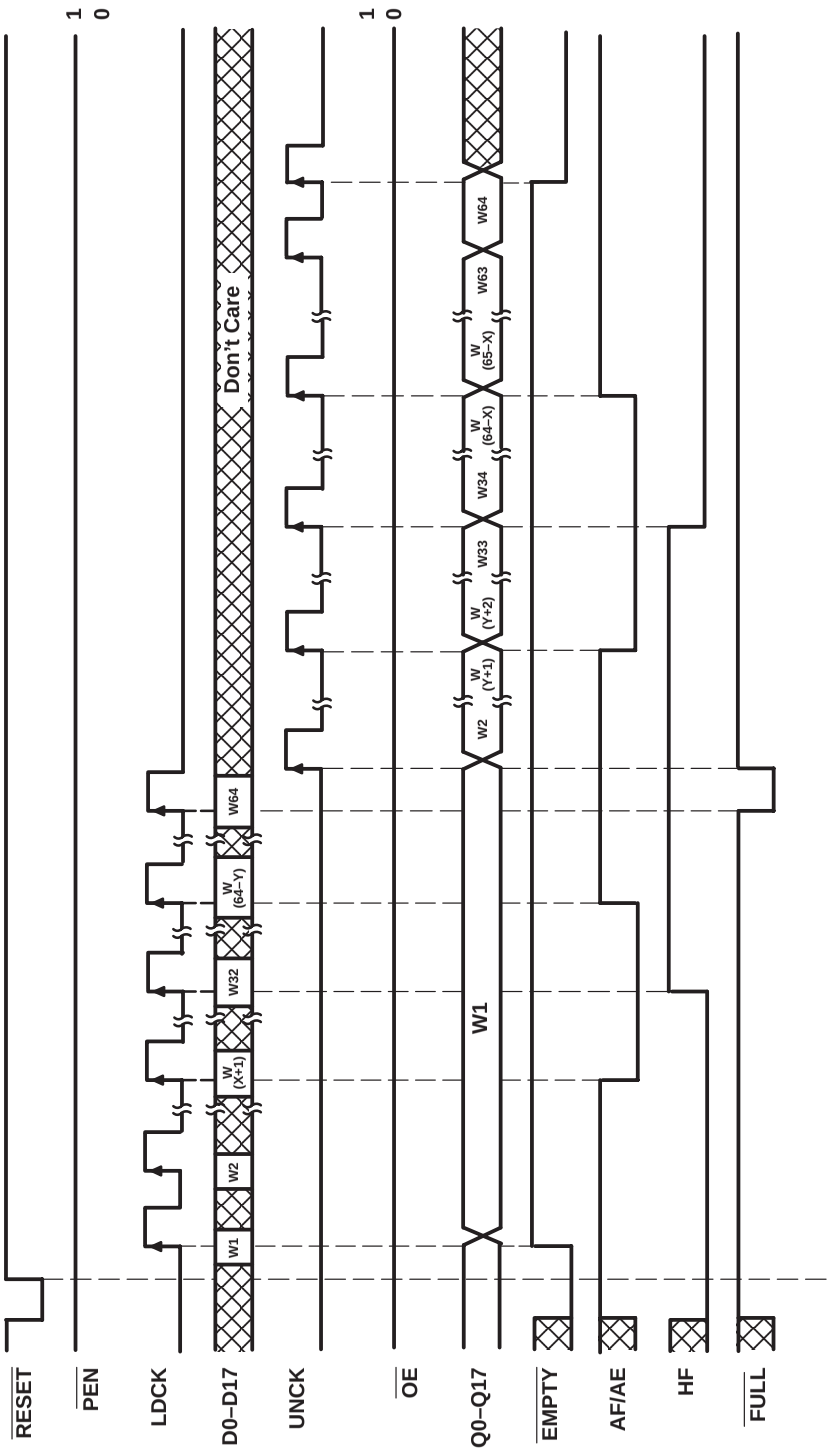


Figure 2. Write, Read, and Flag Timing Reference

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –0.5 V to 7 V
Voltage range applied to a disabled 3-state output . . . . . –0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 74°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			’ACT7814-20		’ACT7814-25		’ACT7814-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, flags		–8		–8		–8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16	mA
		Flags		8		8		8	
T_A	Operating free-air temperature		0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_I = V_{CC} – 0.2 V or 0					400	µA
ΔI_{CC}§		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or V_{CC}.

timing requirements over recommended operating conditions (see Figures 1 through 3)

			'ACT7814-20		'ACT7814-25		'ACT7814-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			50		40		25	MHz
t_w	Pulse duration	LDCK high or low	7		8		12		ns
		UNCK high or low	7		8		12		
		$\overline{PEN}$ low	7		8		12		
		$\overline{RESET}$ low	10		10		12		
t_{su}	Setup time	D0–D17 before LDCK↑	5		5		5		ns
		$\overline{PEN}$ before LDCK↑	5		5		5		
		LDCK inactive before $\overline{RESET}$ high	5		6		6		
t_h	Hold time	D0–D17 after LDCK↑	0		0		0		ns
		LDCK inactive after $\overline{RESET}$ high	5		6		6		
		$\overline{PEN}$ low after LDCK↑	3		3		3		
		$\overline{PEN}$ high after LDCK↓	0		0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 3)

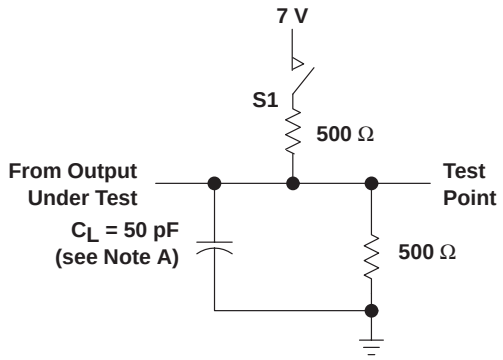
PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7814-20			'ACT7814-25		'ACT7814-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		50			40		25		MHz
t_{pd}	LDCK↑	Any Q	9		20	9	22	9	24	ns
	UNCK↑		6	11.5	15	6	18	6	20	
t_{pd}‡	UNCK↑	Any Q		10.5						ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$	6		15	6	17	6	19	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$	6		15	6	17	6	19	ns
	$\overline{RESET}$ low		4		16	4	18	4	20	
	LDCK↑	$\overline{FULL}$	6		15	6	17	6	19	
t_{PLH}	UNCK↑	$\overline{FULL}$	6		15	6	17	6	19	ns
	$\overline{RESET}$ low		4		18	4	20	4	22	
t_{pd}	LDCK↑	AF/AE	7		18	7	20	7	22	ns
	UNCK↑		7		18	7	20	7	22	
t_{PLH}	$\overline{RESET}$ low	AF/AE	2		10	2	12	2	14	ns
	LDCK↑	HF	5		18	5	20	5	22	
t_{PHL}	UNCK↑	HF	7		18	7	20	7	22	ns
	$\overline{RESET}$ low		3		12	3	14	3	16	
t_{en}	$\overline{OE}$	Any Q	2		9	2	10	2	11	ns
t_{dis}	$\overline{OE}$	Any Q	2		10	2	11	2	12	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This parameter is measured at C_L = 30 pF (see Figure 4).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

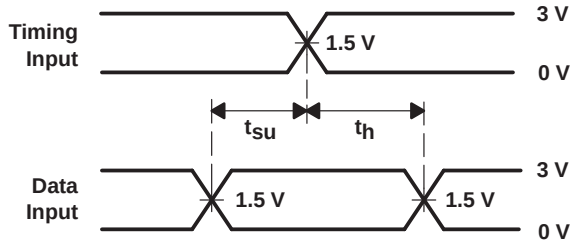
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF,	f = 5 MHz	53	pF

PARAMETER MEASUREMENT INFORMATION

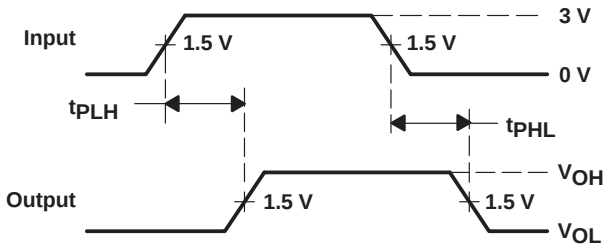


LOAD CIRCUIT

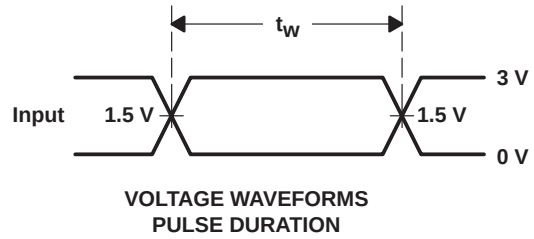
PARAMETER		S1
t_{en}	t_{PZH}	Open
	t_{PZL}	Closed
t_{dis}	t_{PHZ}	Open
	t_{PLZ}	Closed
t_{pd}	t_{PLH}	Open
	t_{PHL}	Open



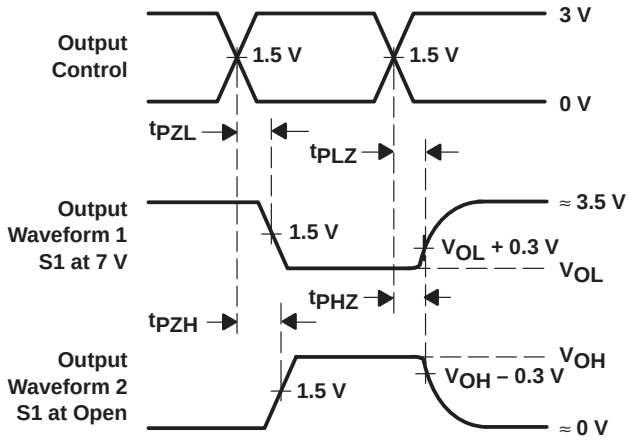
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTE A: C_L includes probe and jig capacitance.

Figure 3. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

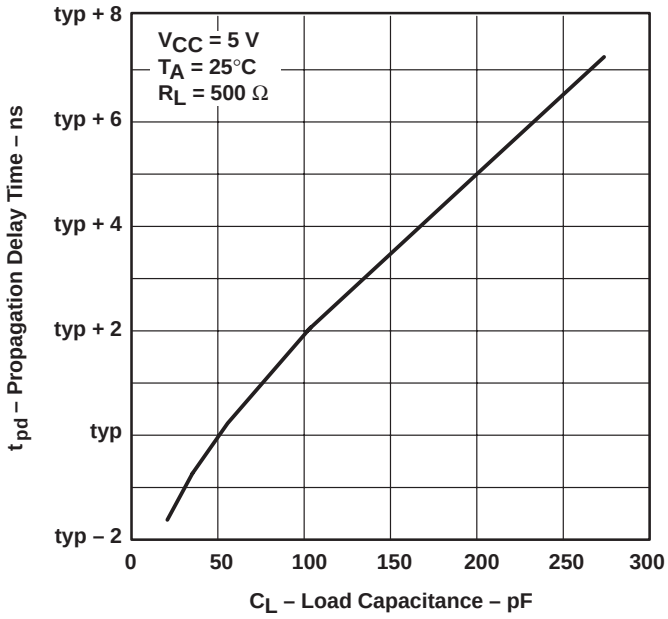


Figure 4

SUPPLY CURRENT vs CLOCK FREQUENCY

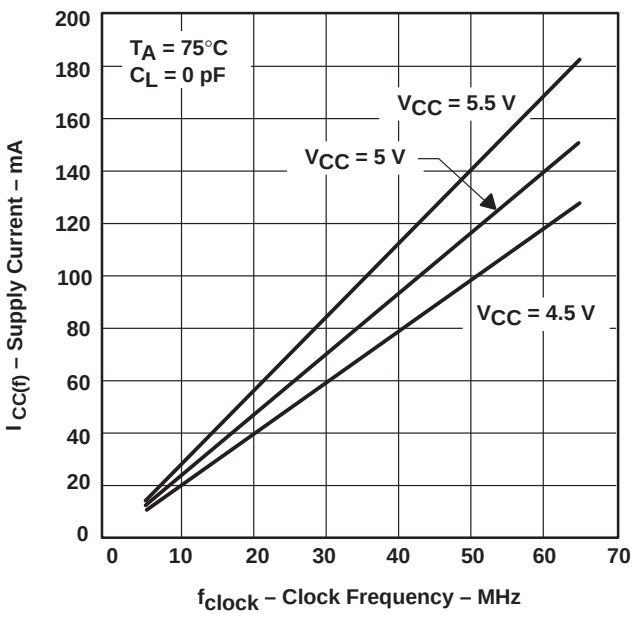


Figure 5

APPLICATION INFORMATION

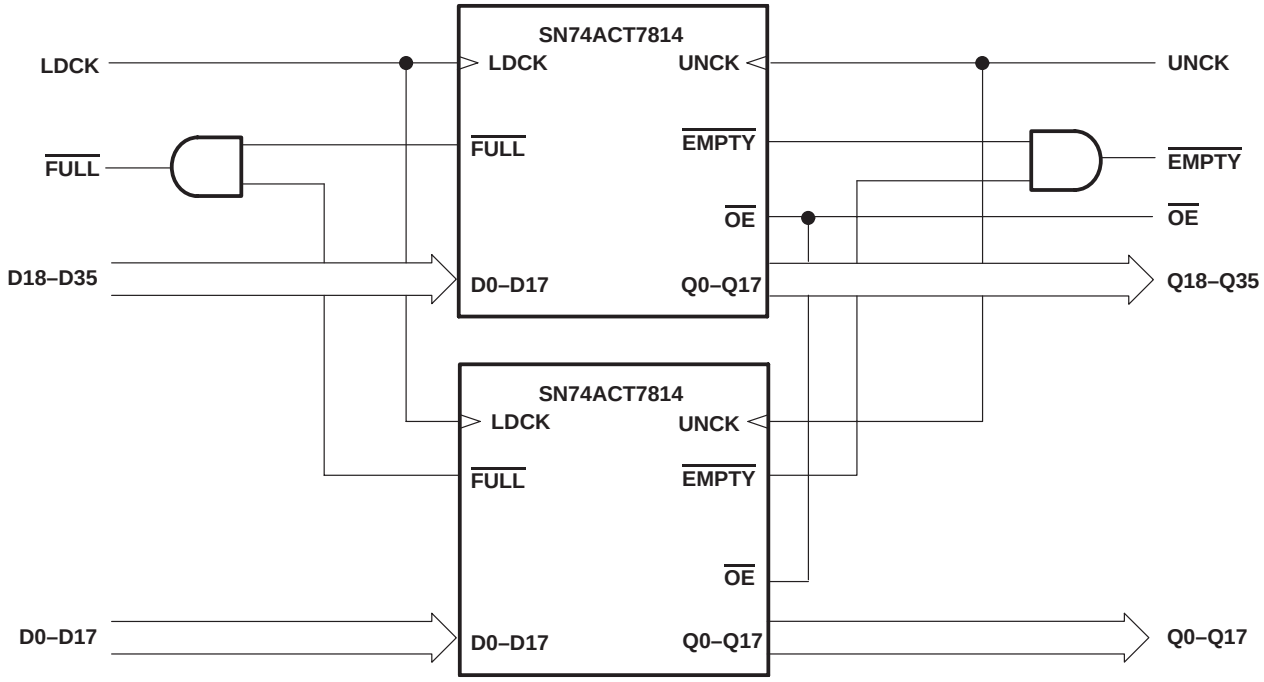


Figure 6. Word-Width Expansion: 64 × 36 Bits

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ACT7814-20DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT7814-20	Samples
SN74ACT7814-20DLR	NRND	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT7814-20	
SN74ACT7814-40DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT7814-40	Samples
SN74ACT7814-40DLR	NRND	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT7814-40	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

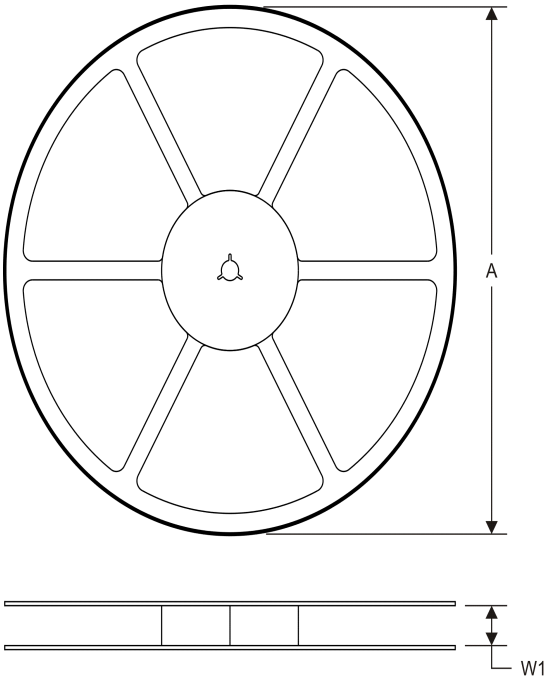
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

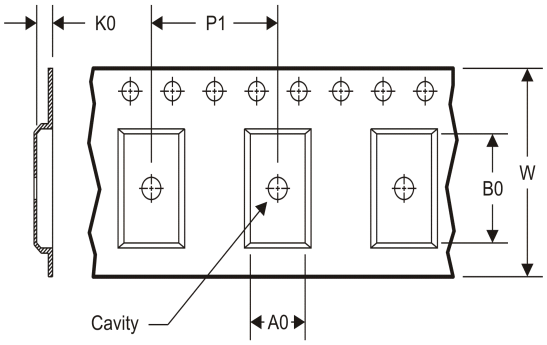
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



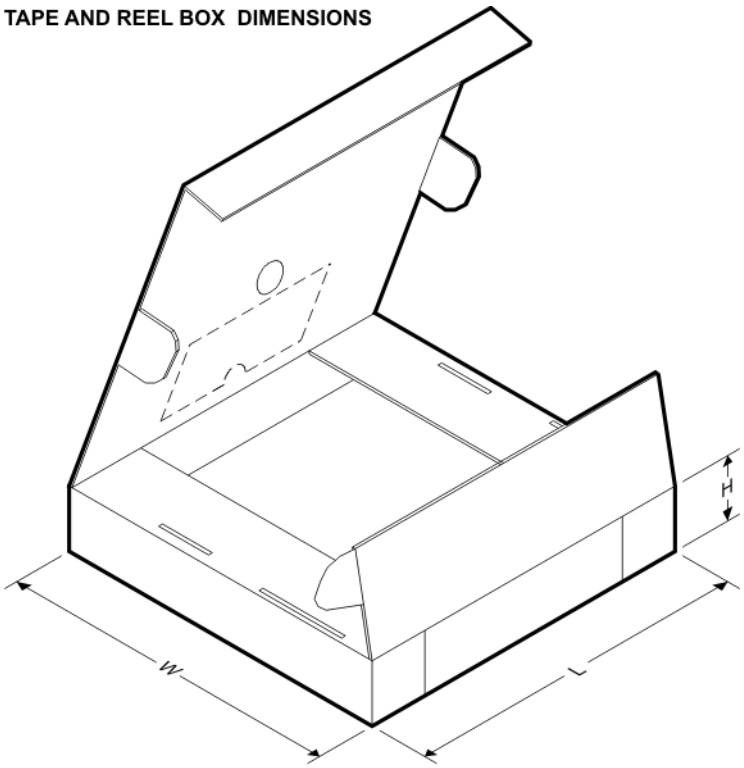
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT7814-20DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN74ACT7814-40DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

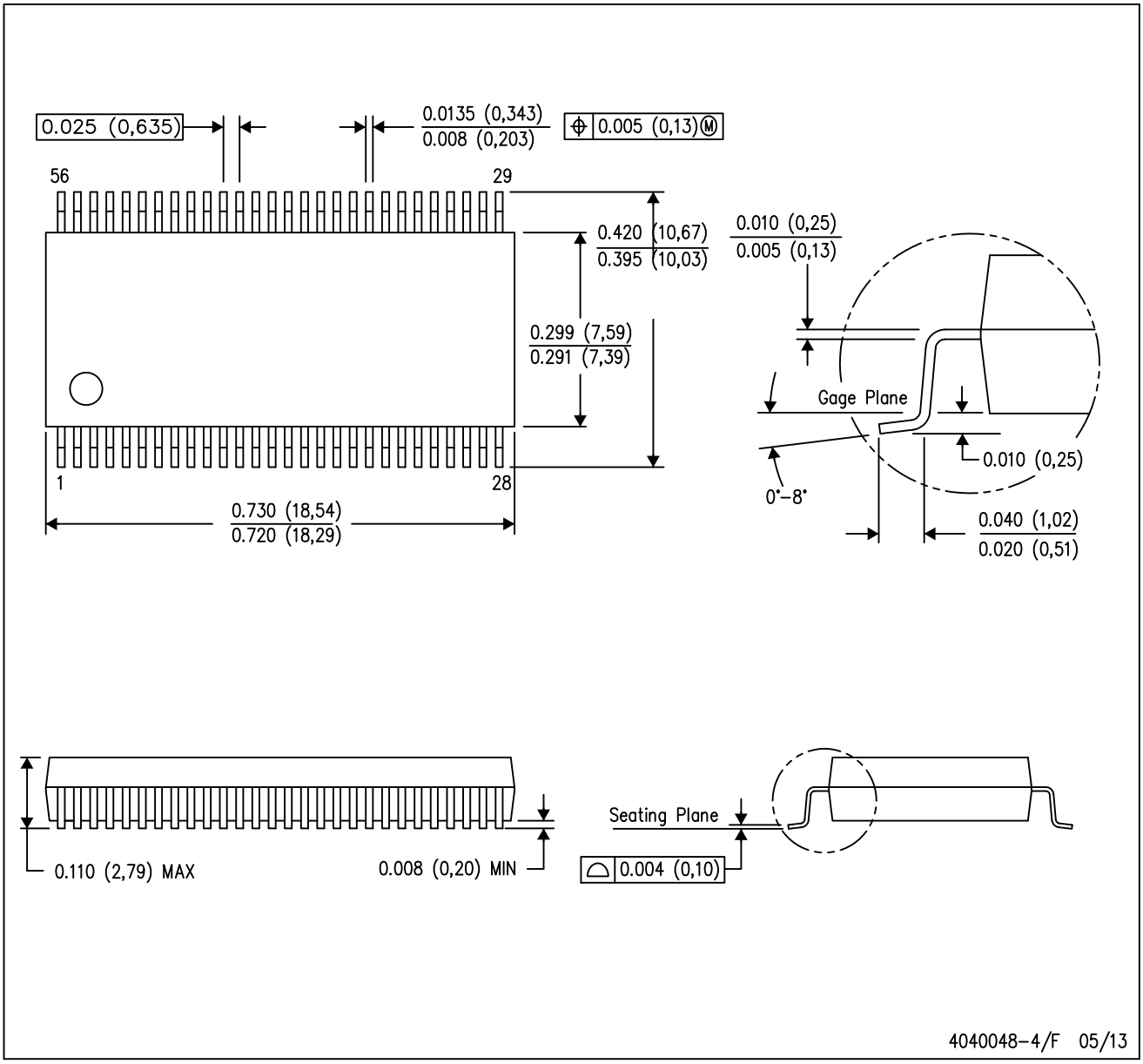
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT7814-20DLR	SSOP	DL	56	1000	367.0	367.0	55.0
SN74ACT7814-40DLR	SSOP	DL	56	1000	367.0	367.0	55.0

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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