National Semiconductor

93Z665/93Z667
8192 x 8-Bit Programmable Read Only Memory

General Description

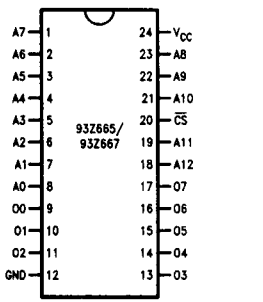
The 93Z665/93Z667 are fully decoded 65,536-bit Programmable Read Only Memories (PROMs) organized 8192 words by eight bits per word. The 93Z665 and 93Z667 are manufactured using highly reliable ISO-Z vertical fuse technology.

Features

- 93Z667 available in 300-mil side-braze DIP
- 93Z665 available in 600-mil side-braze DIP, leadless chip carrier, and Flatpak
- Commercial address access time — 35 ns, 40 ns and 45 ns max
- Military address access time — 45 ns, 50 ns and 55 ns max
- Highly reliable vertical fuses ensure high programming yields
- Power-up TRI-STATE® outputs
- Low current PNP inputs
- Complete AC/DC testability

Connection Diagrams

Dual-In-Line Package



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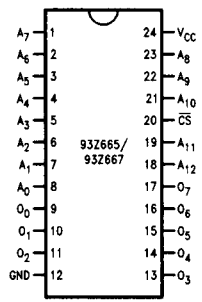
Top View

Order Number 93Z665D or 93Z667D
See NS Package Number D24H*

Flatpak



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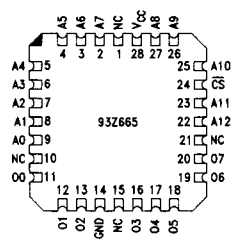
Top View

Order Number 93Z665F
See NS Package Number W24C*

Leadless Chip Carrier



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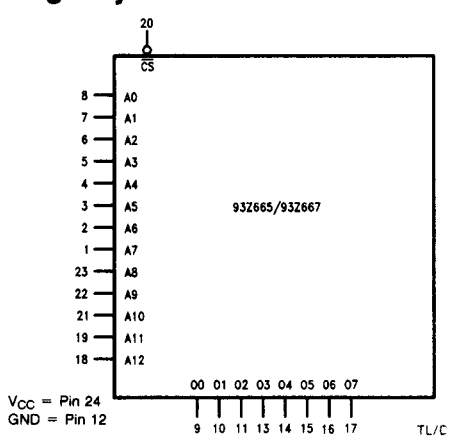
Top View

Order Number 93Z665L
See NS Package Number V28A*

*For most current package information, contact product marketing

Logic Symbol



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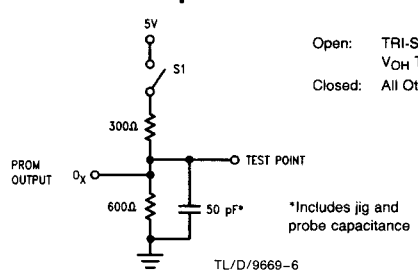
Pin Names

A0–A12	Address Inputs
$\overline{CS}$	Chip Select Input (Active LOW)
O0–O7	Data Outputs

AC Test Output Load



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Absolute Maximum Ratings Above which the useful life may be impaired

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Notes 1 & 2)	−1.5V to V_{CC}
Voltage Applied to Outputs (Output HIGH) (Notes 2 & 3)	−1.5V to +5.5V
Lead Temp. (Soldering, 10 seconds)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current per Output (10 seconds Max)	−100 mA for V_{OH} and +100 mA for V_{OL}
Output Current High Impedance	+20 mA (Max)
Input Current (DC)	−18 mA to +5.0 mA

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

Note 2: These values may be exceeded as required during PROM programming.

Note 3: Output Current limit required.

Operating Conditions

Ambient Operating Temperature	
Commercial	0°C to +70°C
Military	−55°C to +125°C
Positive Supply Voltage	
Commercial	5.0V ±5%
Military	5.0V ±10%
Maximum Low-Level Input Voltage (V_{IL})	0.8V
Minimum High-Level Input Voltage (V_{IH})	2.0V

DC Performance Characteristics: over guaranteed operating ranges unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs			0.8	V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs	2.0			V
V_{IC}	Input Clamp Diode Voltage	V_{CC} = Min, I_{IN} = −18 mA			−1.2	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.30	0.45	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −2.0 mA Address Any "1"	2.4			V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IL} = 0.45V		−10	−100	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IH} = 2.4V to V_{CC}	−40		40	μA
I_{OHZ} I_{OLZ}	Output Leakage Current for HIGH Impedance State	V_{OH} = 2.4V V_{OL} = 0.4V			40 −40	μA μA
I_{OS}	Output Short-Circuit Current	V_{CC} = Max, V_O = 0V (Note 2) Address Any "1"	−15	−80	−100	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs GND, All Outputs Open			180	mA
C_{IN}	Input Pin Capacitance	V_{CC} = 5.0V, V_{IN} = 4.0V, f = 1.0 MHz		7.0 (Note 3)	15.0	pF
C_O	Output Pin Capacitance	V_{CC} = 5.0V, V_O = 4.0V, f = 1.0 MHz		10.0 (Note 3)	15.0	pF

AC Performance Characteristics

Symbol	Parameter	Conditions	-35	-40	-45	Units
COMMERCIAL V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +75°C						
t_{AA}	Address to Output Access Time	See AC Output Load and Note 5	35	40	45	ns
t_{ACS}	Chip Select to Output Access Time	See AC Output Load and Note 5	20	20	30	ns
t_{HZ}	Chip Deselect to Output TRI-STATE	See AC Output Load and Note 4	20	20	30	ns

AC Performance Characteristics (Continued)

Symbol	Parameter	Conditions	-40	-45	-50	Units
MILITARY V_{CC} = 5.0V ±10%, GND = 0V, T_C = −55°C to +125°C						
t_{AA}	Address to Output Access Time	See AC Output Load and Note 5	45	50	55	ns
t_{ACS}	Chip Select to Output Access Time	See AC Output Load and Note 5	25	25	30	ns
t_{HZ}	Chip Deselect to Output TRI-STATE	See AC Output Load and Note 4	25	25	30	ns

Note 1: Typical values are at V_{CC} = 5.0V, +25°C and maximum loading.

Note 2: Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

Note 3: This parameter value is based on initial design qualification and is also verified on every design change. These are not tested in production.

Note 4: t_{HZ} is tested with load shown in *Figure 2*. Transition to High-Z is measured at steady state high V_{OH} level −500 mV or steady state low V_{OL} level +500 mV on the outputs from the point at which chip select crosses the 1.5V level towards its V_{IH} level.

Note 5: AC Address Access and Chip Select Access is done under the following test conditions. Input pulse levels are from 0V to 3V and input/output timing reference levels at 1.5V.

Current-Pulse Programming Specifications (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Power Supply Voltage	Typical I_{CC} at 6.5V = 250 mA	6.4	6.5	6.6	V
$t_{r\,VCC}$	Power Supply Rise Time (Note 3)		0.2	2.0		μs
$t_{f\,VCC}$	Power Supply Fall Time		0.2	2.0		μs
t_{ON}	V_{CC} ON Time	See Programming Timing Diagram	(Note 1)			
t_{OFF}	V_{CC} OFF Time		(Note 2)			
	Duty Cycle for V_{CC}	$t_{ON}/(t_{OFF} + t_{ON})$			50	%
READ STROBE (Note 5)						
t_W	Fuse Read Time	Machine Cycle		1.0		μs
t_{dRAP}	Delay to Read after Programming	Verify		3.0		μs
t_{CS}	Chip Enable		0.1	1.0		μs
OUTPUT DESELECT						
V_{OS}	Output Deselect Voltage		11.8	12	12.5	V
I_{OS}	Output Deselect Current Limit		20	50	100	mA
O_{VS}	Output Voltage Select	TTL H or L		5.0	5.5	V
t_{rod}	Output Deselect Rise Time		1.0	1.0	2.0	μs
t_{fod}	Output Deselect Fall Time		0.1	0.1	1.0	μs
t_{CSDD}	Deselect Chip to Deselect Output		0.1	1.0		μs
PROGRAMMING CURRENT-PULSE TRAIN ON CHIP SELECT						
$I_{CSp(Min)}$	Initial Current Pulse			40	60	mA
$I_{CSp(Max)}$	CS Programming Current Limit	Apply Current Pulse to Chip Select Pin 20	155	160	165	mA
$V_{CSp(Max)}$	CS Programming Voltage Limit		24	25	26	V
t_{rcsp}	Programming Pulse Rise Time		160	100	100	mA/μs
t_{dBP}	Delay to Initial Programming Pulse		2.0	3.0		μs
t_{dAP}	Delay after Programming Pulse		1.0	1.0		μs
t_{PW}	Programming Pulse Widths		6.0	7.0	9.0	μs
t_{fCSp}	Programming Pulse Fall Time (Note 3)		0.1	0.1	0.2	μs
ΔI_{CSp}	Current Pulse Step Increase		5.0	10.0	10.0	mA
	Duty Cycle for Programming Pulses	Each Successive Pulse is Increased by ΔI_{CSp}	10	50	50	%

Note 1: Total time V_{CC} is on to program fuse is equal to or greater than the sum of all the specified delays, pulse widths and rise/fall times.

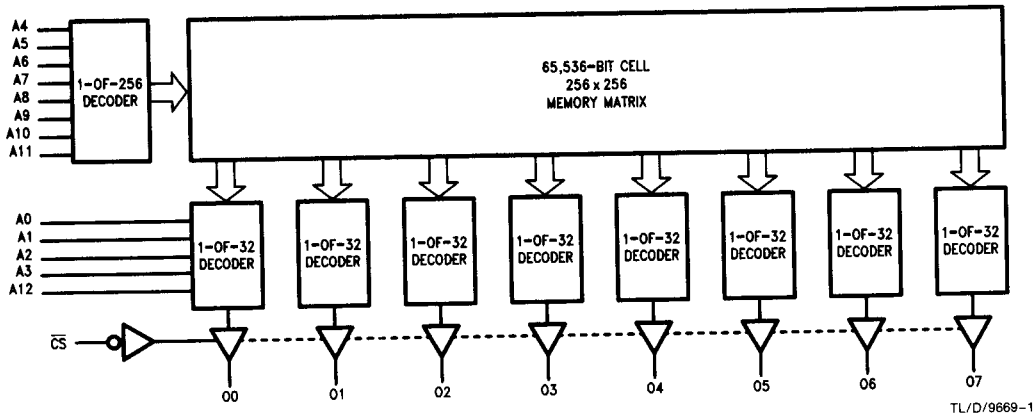
Note 2: t_{OFF} is equal to or greater than t_{ON}.

Note 3: Rise and fall times are from 10% to 90%.

Note 4: Recommended programming temp. T_C = +25°C ±10°C.

Note 5: Proceed to next address after read strobe indicates programmed cell.

Block Diagram



Note: Programmed = Low
Unprogrammed = High on the Outputs

Functional Description

The 93Z665 and 93Z667 are TTL bipolar field Programmable Read Only Memories (PROMs) organized 8192 words by eight bits per word. The 93Z665 and 93Z667 have TRI-STATE outputs which provide active pull-ups and pull-downs when enabled and high output impedence when disabled. This allows optimization of word expansion in bus organized systems.

Chip Select is provided for memory expansion without the need for additional decoding. The fast Chip Select access time permits direct address decoding without increasing overall memory access times. The device is enabled only when $\overline{CS}$ is LOW. During system power up, outputs remain in the high impedance state until DC power supply conditions are met, thereafter changing state according to the condition of $\overline{CS}$.

The devices contain internal test rows and test columns which are accessed and programmed during both wafer sort and final test. These test fuses are used to assure high programmability and to guarantee AC performance and DC parameters. PROM programmability is verified through test row and test column. PROM input levels on unprogrammed devices are also verified through testing of test row and test column.

The 93Z665 and 93Z667 use open base vertical (junction) fuse cells. Initially the unprogrammed cell is in the logic "1" state. A cell can be programmed to the logic "0" state by following the specified programming procedure which defuses aluminum through the emitter base junction of the cell transistor, thereby forming a low impedance path.

The read function is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins A0 through A12 and the chip is selected. Data is then available at the outputs after t_{AA}.

Programming

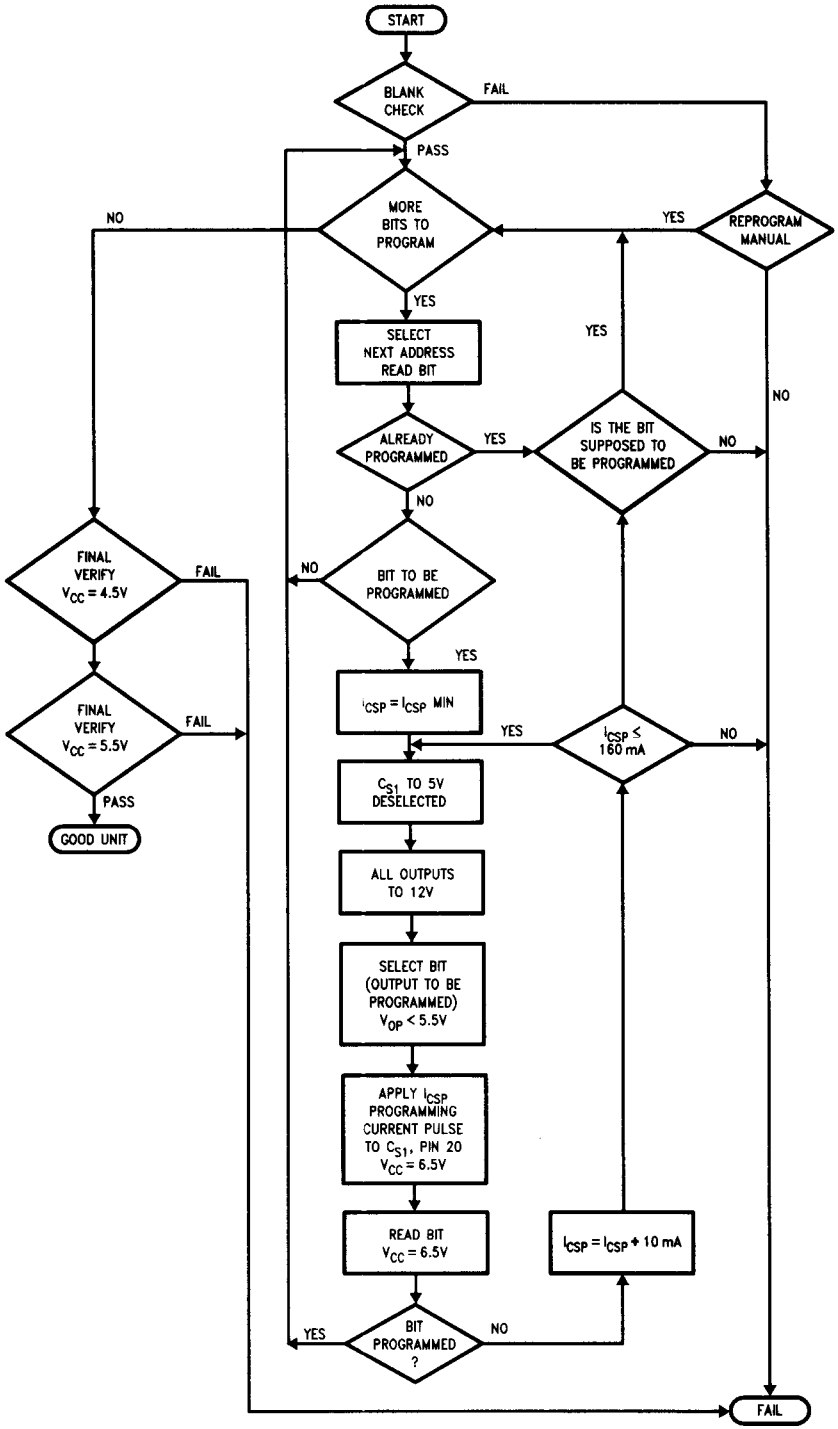
The 93Z665 and 93Z667 are manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure below. One may use any of the commercially available programmers which have been approved by National Semiconductor.

I. Blank Check—Initial Read.
   - A. Chip Select is Enabled
   - B. V_{CC} is Raised to 5.5V
   - C. TTL Levels are Applied to All Address Lines
   - D. Verify All Outputs are TTL High on All Addresses
   - E. Repeat C and D until All Addresses have been Checked

II. Programming Mode
   - A. TTL Levels are Applied to All Address Lines
   - B. V_{CC} is Raised to 6.5V
   - C. Chip Select is Deselected
   - D. All Outputs are Raised to 12V
   - E. Selected Output is Lowered Below 5.5V
   - F. Programming Current Pulse Train is Applied to the Chip Select Pin
   - G. Consecutive Current Pulses are 7 μs–9 μs Wide and Increase at 10 mA per Pulse
   - H. A Read is Performed before and after Each Pulse (V_{CC} = 6.5V)
   - I. The Programming Current is Stepped Up until the Cell Programs

III. Final Verify (2 Pass)
   - A. V_{CC} is Lowered to 4.5V
   - B. Chip Select is Enabled
   - C. TTL Levels are Applied to All Address Lines
   - D. Verify Pattern on All Outputs, All Addresses
   - E. Repeat C and D for All Addresses
   - F. V_{CC} Increases to 5.5V
   - G. Repeat B, C, D and E

Programming Flow Chart



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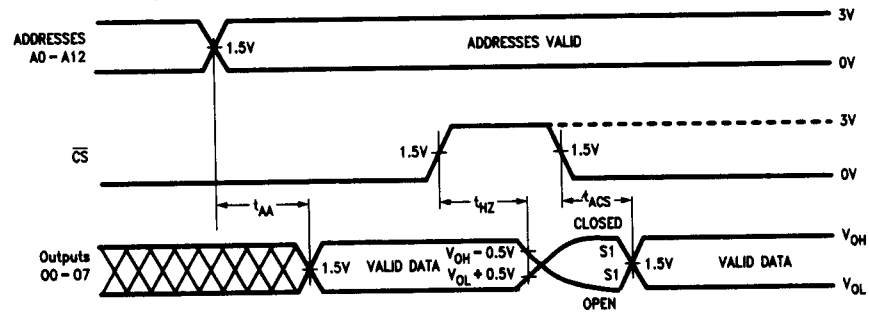
Timing Diagrams

READ MODE TIMING

Propagation Delay from Address Valid to Output and $\overline{CS}$ Valid to Output



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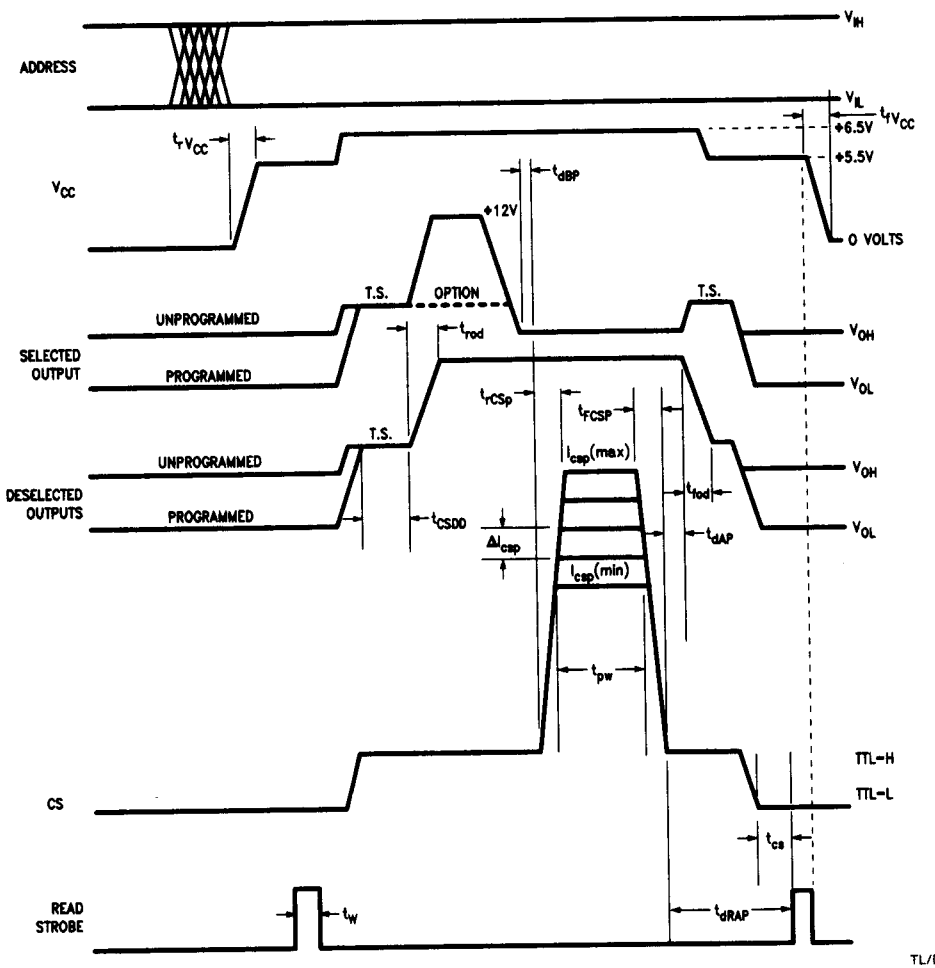
PROGRAMMING TIMING DIAGRAM



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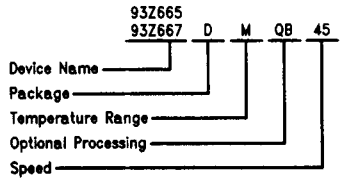
Note:

Typical Output Characteristics using a 1 kΩ Pull-Up Resistor to 5V. 12V, TTL-H, and TTL-L Force Voltages.
T.S. is TRI-STATE.

Ordering Information



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Packages

D = Side-Braze DIP

L = Leadless Chip Carrier

F = Flatpak

Temperature Ranges

Com. = 0°C to +75°C

Mil. = −55°C to +125°C

Speed

Com		Mil.	
=	35 ns	=	45 ns
=	40 ns	=	50 ns
=	45 ns	=	55 ns

Optional Processing

QB = Mil STD 883
Method 5004 & 5005
Level B