

# SN74LS373, SN74LS374



ON Semiconductor

<http://onsemi.com>

## Octal Transparent Latch with 3-State Outputs; Octal D-Type Flip-Flop with 3-State Output

The SN74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH the bus output is in the high impedance state.

The SN74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all ON Semiconductor TTL families.

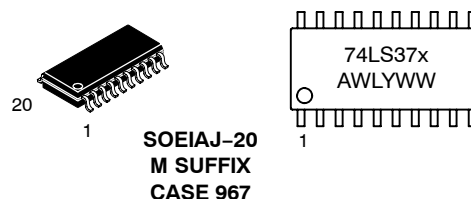
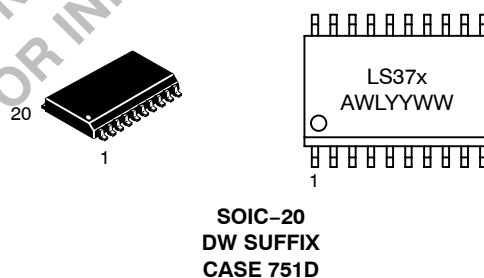
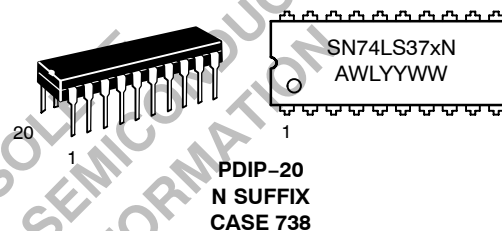
- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current - High			-2.6	mA
$I_{OL}$	Output Current - Low			24	mA

LOW  
POWER  
SCHOTTKY

### MARKING DIAGRAMS



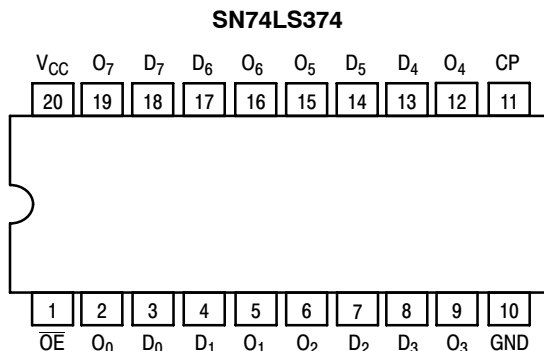
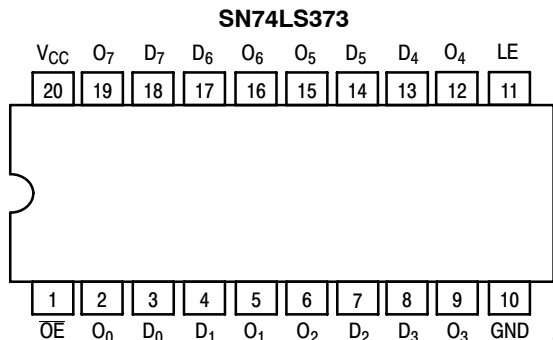
x = 3 or 4  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# SN74LS373, SN74LS374

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

D<sub>0</sub> - D<sub>7</sub> Data Inputs  
 LE Latch Enable (Active HIGH) Input  
 CP Clock (Active HIGH Going Edge) Input  
 $\overline{O}E$  Output Enable (Active LOW) Input  
 O<sub>0</sub> - O<sub>7</sub> Outputs

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOADING (Note a)

	HIGH	LOW
D <sub>0</sub> - D <sub>7</sub>	0.5 U.L.	0.25 U.L.
LE	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
$\overline{O}E$	0.5 U.L.	0.25 U.L.
O <sub>0</sub> - O <sub>7</sub>	65 U.L.	15 U.L.

### TRUTH TABLE

#### LS373

D <sub>n</sub>	LE	$\overline{O}E$	O <sub>n</sub>
H	H	L	H
L	H	L	L
X	L	L	Q <sub>0</sub>
X	X	H	Z*

#### LS374

D <sub>n</sub>	LE	$\overline{O}E$	O <sub>n</sub>
H		L	H
L		L	L
X	X	H	Z*

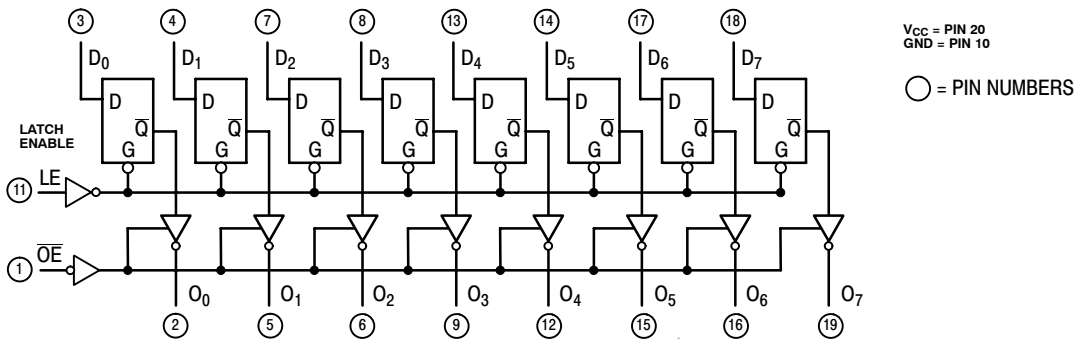
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

\* Note: Contents of flip-flops unaffected by the state of the Output Enable input ( $\overline{O}E$ ).

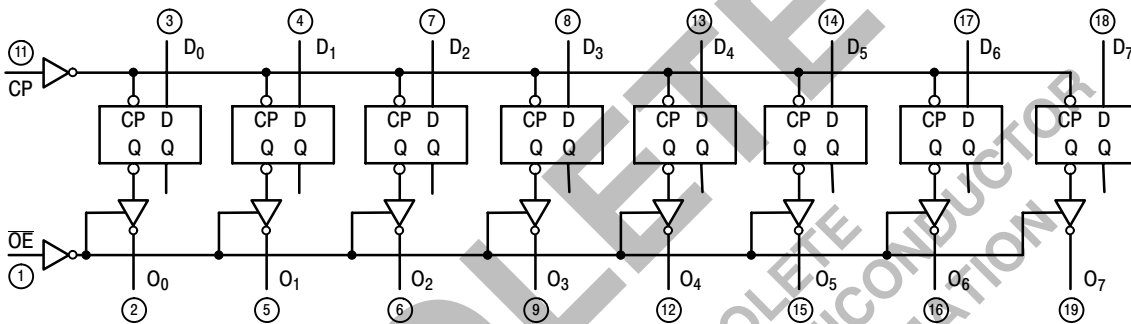
# SN74LS373, SN74LS374

## LOGIC DIAGRAMS

### SN74LS373



### SN74LS374



## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4	3.1		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>OZH</sub>	Output Off Current HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V
I <sub>OZL</sub>	Output Off Current LOW			-20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-30		-130	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			40	mA	V <sub>CC</sub> = MAX

1. Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS373, SN74LS374

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS373			LS374				
		Min	Typ	Max	Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency				35	50		MHz	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Data to Output		12 12	18 18				ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time		15 25	28 36		20 21	28 28	ns	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time		12 15	20 25		12 15	20 25	ns	C <sub>L</sub> = 5.0 pF

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits				Unit
		LS373		LS374		
		Min	Max	Min	Max	
t <sub>w</sub>	Clock Pulse Width	15		15		ns
t <sub>s</sub>	Setup Time	5.0		20		ns
t <sub>h</sub>	Hold Time	20		0		ns

## DEFINITION OF TERMS

**SETUP TIME (t<sub>s</sub>)** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

**HOLD TIME (t<sub>h</sub>)** — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

## SN74LS373

### AC WAVEFORMS

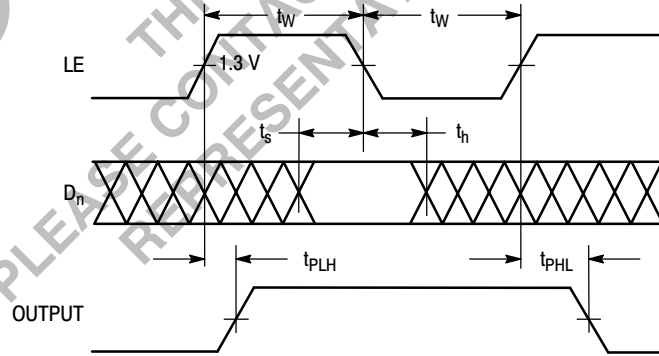


Figure 1.

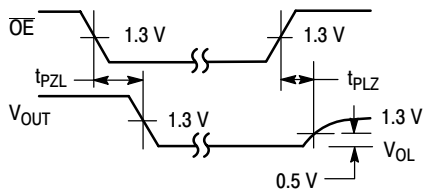


Figure 2.

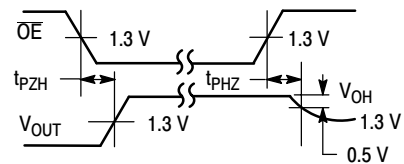
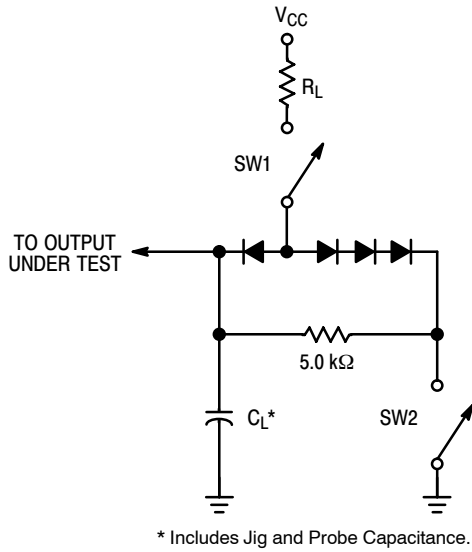


Figure 3.

# SN74LS373, SN74LS374

## SN74LS373

### AC LOAD CIRCUIT



### SWITCH POSITIONS

SYMBOL	SW1	SW2
$t_{pZH}$	Open	Closed
$t_{pZL}$	Closed	Open
$t_{pLZ}$	Closed	Closed
$t_{pHZ}$	Closed	Closed

Figure 4.

## SN74LS374

### AC WAVEFORMS

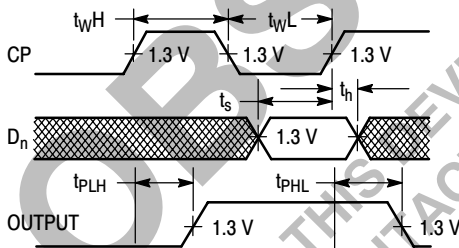


Figure 5.

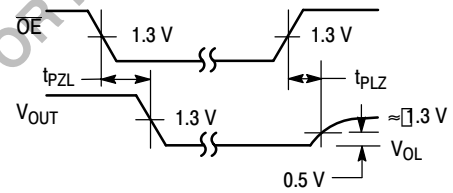


Figure 6.

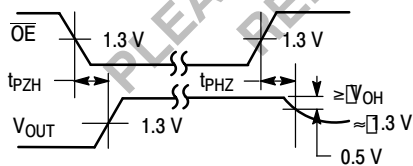
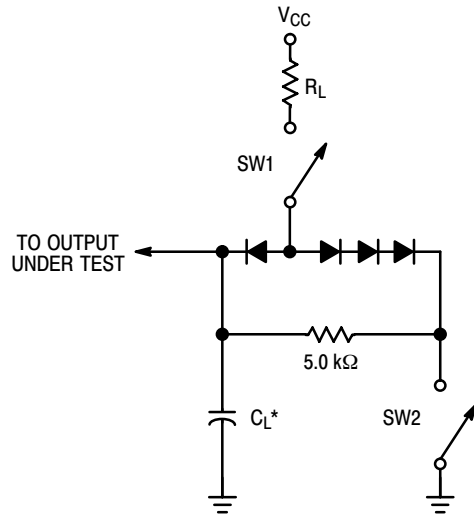


Figure 7.

# SN74LS373, SN74LS374

## SN74LS374

### AC LOAD CIRCUIT



\* Includes Jig and Probe Capacitance.

### SWITCH POSITIONS

SYMBOL	SW1	SW2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PLZ}$	Closed	Closed
$t_{PHZ}$	Closed	Closed

Figure 8.

### DEVICE ORDERING INFORMATION

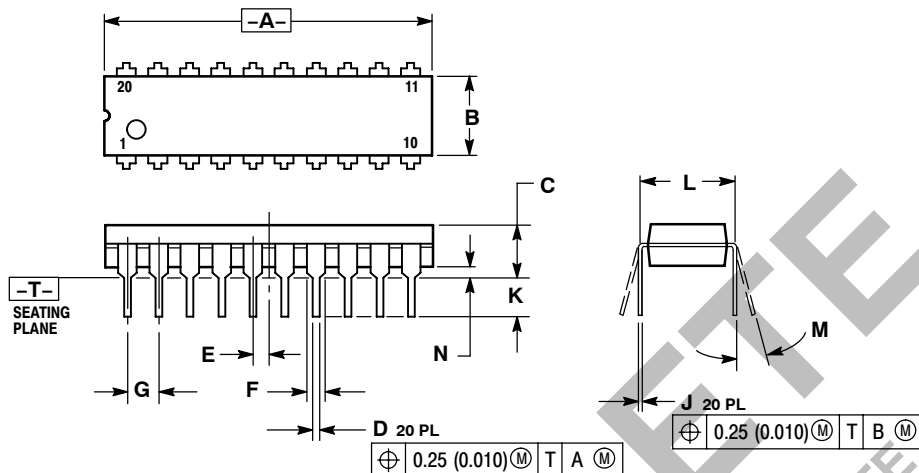
Device Order Number	Package Type	Tape and Reel Size
SN74LS373N	PDIP-20	1440 Units/Box
SN74LS373DW	SOIC-WIDE	38 Units/Rail
SN74LS373DWR2	SOIC-WIDE	2500/Tape and Reel
SN74LS373M	SOEIAJ-20	See Note 2
SN74LS373MEL	SOEIAJ-20	See Note 2
SN74LS374N	PDIP-20	1440 Units/Box
SN74LS374DW	SOIC-WIDE	38 Units/Rail
SN74LS374DWR2	SOIC-WIDE	2500/Tape and Reel
SN74LS374M	SOEIAJ-20	See Note 2
SN74LS374MEL	SOEIAJ-20	See Note 2

2. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

# SN74LS373, SN74LS374

## PACKAGE DIMENSIONS

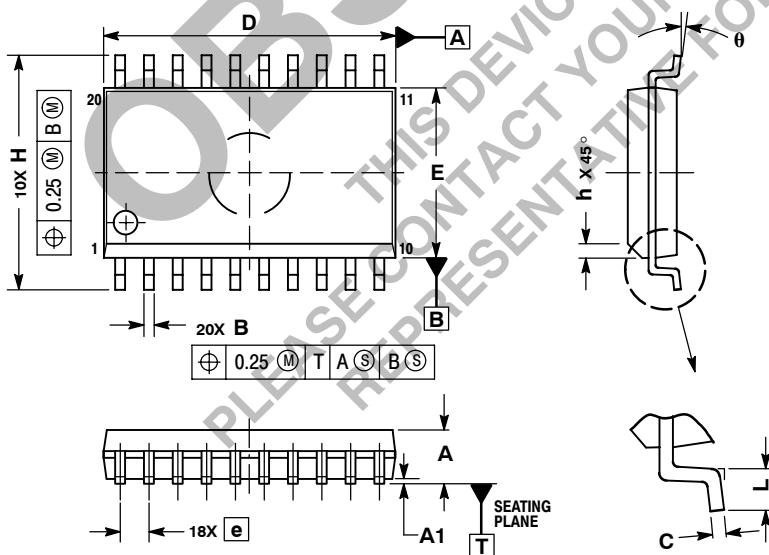
### N SUFFIX PLASTIC PACKAGE CASE 738-03 ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### D SUFFIX PLASTIC SOIC PACKAGE CASE 751D-05 ISSUE F



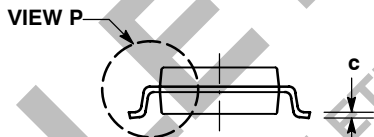
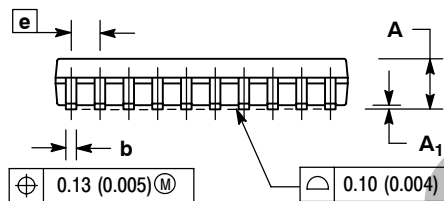
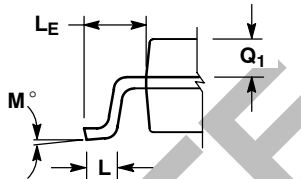
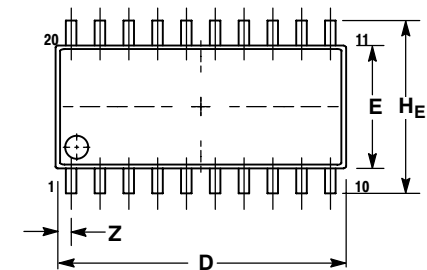
- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
theta	0°	7°

# SN74LS373, SN74LS374

## PACKAGE DIMENSIONS

**M SUFFIX**  
**SOEIAJ PACKAGE**  
**CASE 967-01**  
**ISSUE O**



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

**ON Semiconductor** and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT:**  
 Literature Distribution Center for ON Semiconductor  
 P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
 Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
 Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative