FAIRCHILD

December 2014

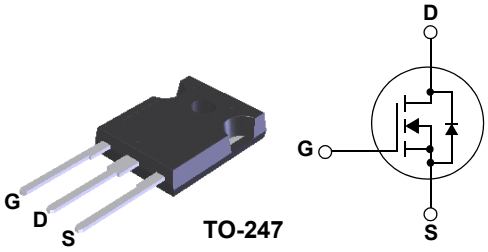
FCH077N65F_F085

N-Channel SuperFET II FRFET MOSFET

650 V, 54 A, 77 mΩ

Features

- Typical $R_{DS(on)}$ = 68 mΩ at V_{GS} = 10 V, I_D = 27 A
- Typical $Q_{g(tot)}$ = 126 nC at V_{GS} = 10V, I_D = 27 A
- UIS Capability
- Qualified to AEC Q101
- RoHS Compliant



Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently SuperFETII is very well suited for the Soft switching and Hard Switching topologies like High Voltage Full Bridge and Half Bridge DC-DC, Interleaved Boost PFC, Boost PFC for HEV-EV automotive.
SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.

For current package drawing, please refer to the Fairchild web-site at https://www.fairchildsemi.com/package-drawings/TO/TO247A03.pdf

Application

- Automotive On Board Charger
- Automotive DC/DC converter for HEV

Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	650	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current - Continuous (V_{GS}=10) (Note 1)	54	A
	Pulsed Drain Current	See Fig 4	A
E_{AS}	Single Pulse Avalanche Rating (Note 2)	1128	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
P_D	Power Dissipation	481	W
	Derate Above 25°C	3.85	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to + 150	°C
$R_{\theta JC}$	Maximum Thermal Resistance Junction to Case	0.26	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient (Note 4)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH077N65F	FCH077N65F_F085	TO-247	-	-	30

Notes:
1: Current is limited by bondwire configuration.
2: Starting T_J = 25°C, L = 18.65mH, I_{AS} = 11A, V_{DD} = 100V during inductor charging and V_{DD} = 0V during time in avalanche.
3: I_{SD} ≤ 27A, di/dt ≤ 200 A/us, V_{DD} ≤ 380V, starting T_J = 25°C.
4: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	650	-	-	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=650V, V_{GS} = 0V, T_J = 25°C	-	-	10	μA
		V_{DS}=650V, V_{GS} = 0V, T_J = 150°C(Note 5)	-	-	1	mA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	3.0	-	5.0	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = 27A, V_{GS} = 10V, T_J = 25°C	-	68	77	mΩ
		I_D = 27A, V_{GS} = 10V, T_J = 150°C(Note 5)	-	154	184	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	5385	7162	pF
C_{oss}	Output Capacitance		-	5629	7486	pF
C_{rss}	Reverse Transfer Capacitance		-	194	-	pF
$C_{oss(eff)}$	Effective Output Capacitance	V_{DS} = 0V to 520V, V_{GS} = 0V	-	693	-	pF
R_g	Gate Resistance	f = 1MHz	-	0.5	-	Ω
$Q_{g(ToT)}$	Total Gate Charge	V_{DD} = 380V, I_D = 27A, V_{GS} = 10V	-	126	164	nC
$Q_{g(th)}$	Threshold Gate Charge		-	9	12	nC
Q_{gs}	Gate to Source Gate Charge		-	28	-	nC
Q_{gd}	Gate to Drain “Miller“ Charge		-	53	-	nC

Switching Characteristics

t_{on}	Turn-On Time	V_{DD} = 380V, I_D = 27A, V_{GS} = 10V, R_G = 4.7Ω	-	64	148	ns
$t_{d(on)}$	Turn-On Delay Time		-	37	-	ns
t_r	Rise Time		-	27	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	105	-	ns
t_f	Fall Time		-	5.3	-	ns
t_{off}	Turn-Off Time		-	108.3	237	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	I_{SD} = 27A, V_{GS} = 0V	-	-	1.2	V
T_{rr}	Reverse Recovery Time	I_F = 27A, dI_{SD}/dt = 100A/μs, V_{DD} = 520V	-	190	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.5	-	μC

Notes:

5: The maximum value is specified by design at T_J = 150°C. Product is not tested to this condition in production.

Typical Characteristics

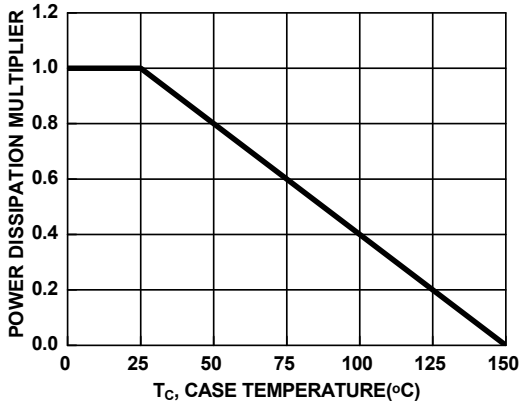


Figure 1. Normalized Power Dissipation vs. Case Temperature

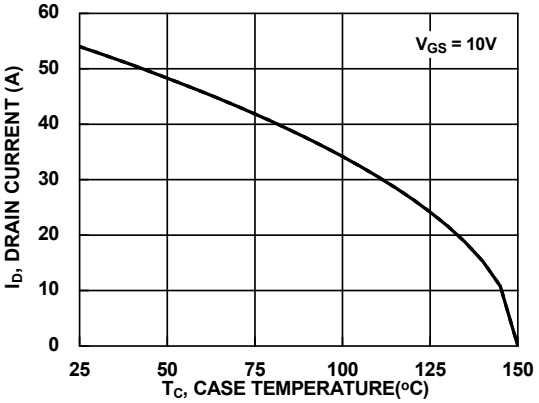


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

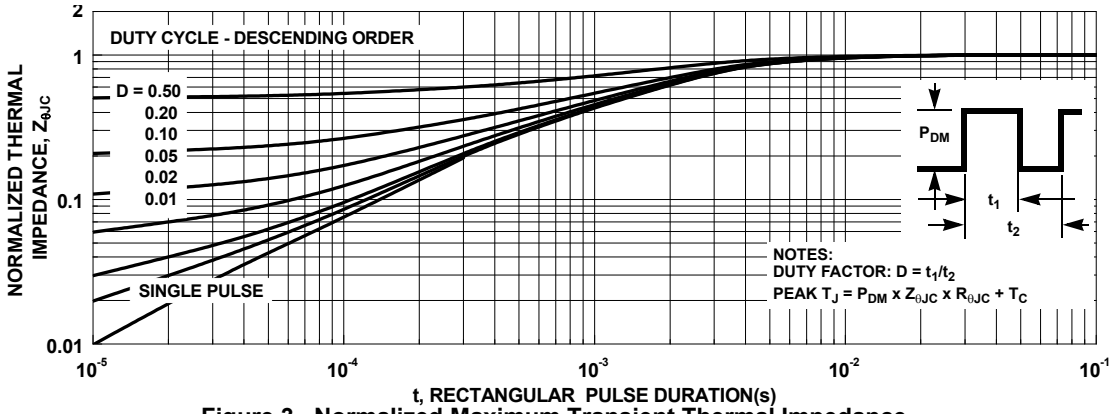


Figure 3. Normalized Maximum Transient Thermal Impedance

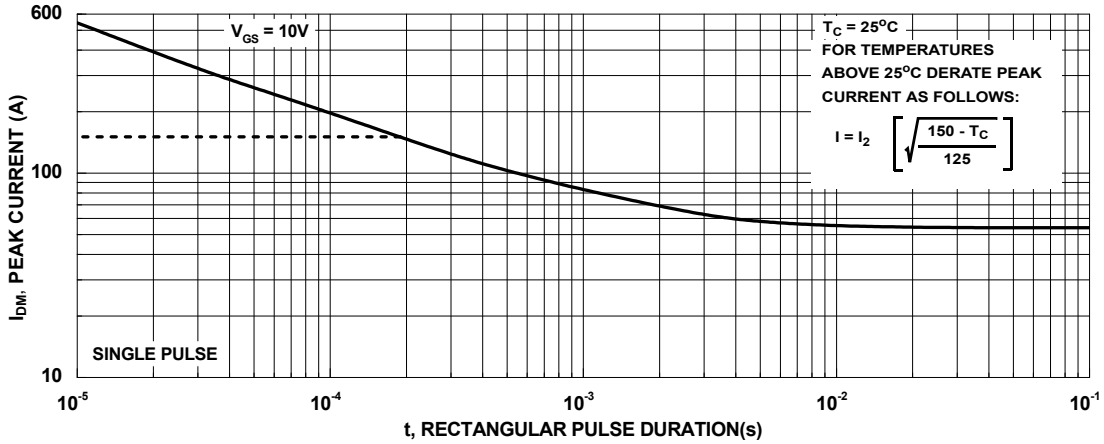


Figure 4. Peak Current Capability

Typical Characteristics

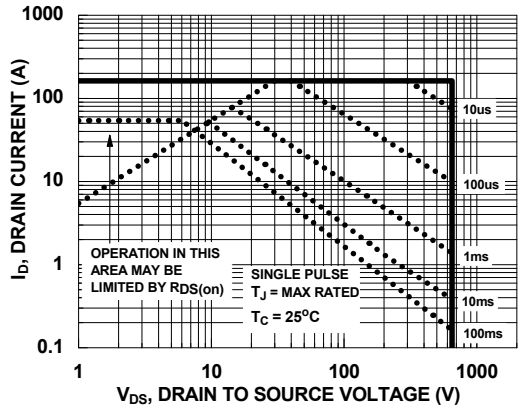


Figure 5. Forward Bias Safe Operating Area

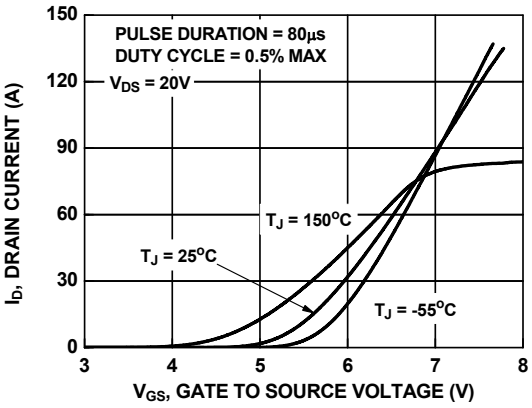


Figure 6. Transfer Characteristics

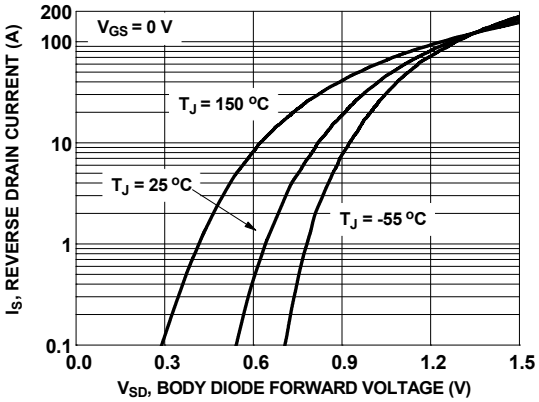


Figure 7. Forward Diode Characteristics

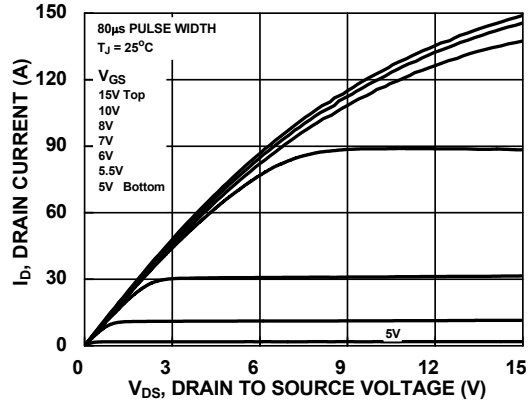


Figure 8. Saturation Characteristics

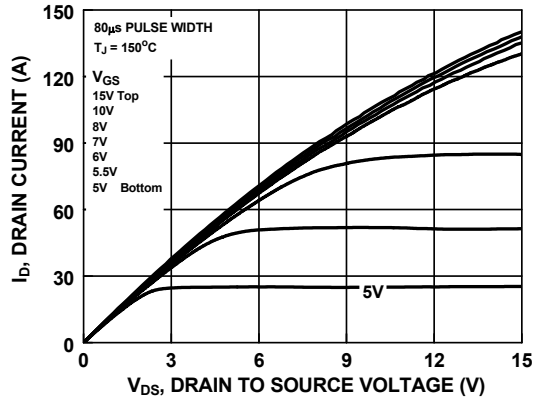


Figure 9. Saturation Characteristics

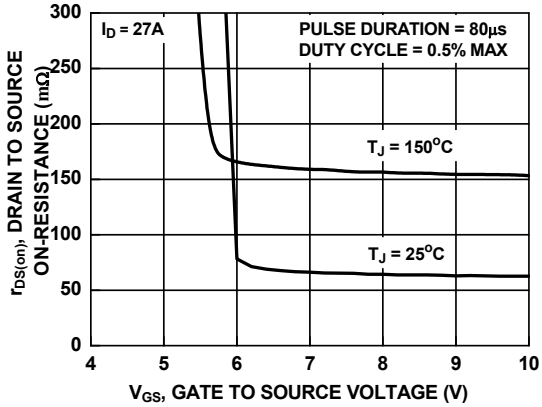


Figure 10. R_{DSON} vs. Gate Voltage

Typical Characteristics

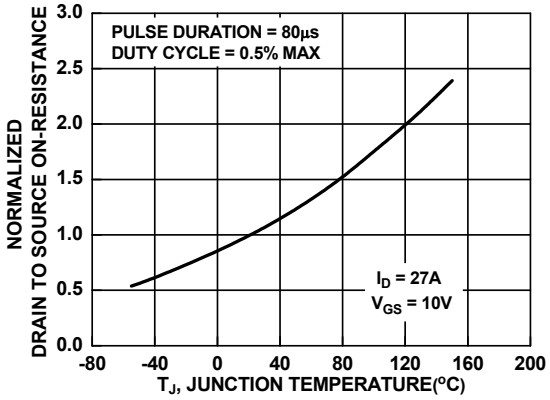


Figure 11. Normalized R_{DSON} vs. Junction Temperature

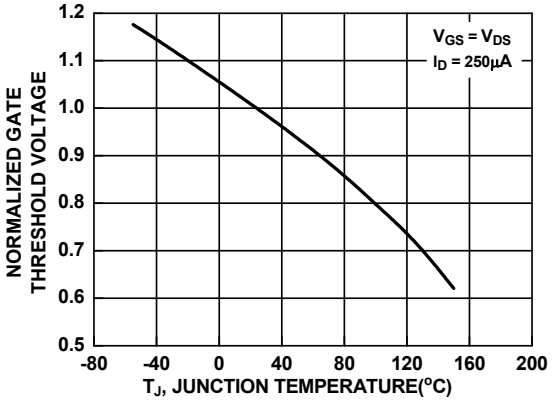


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

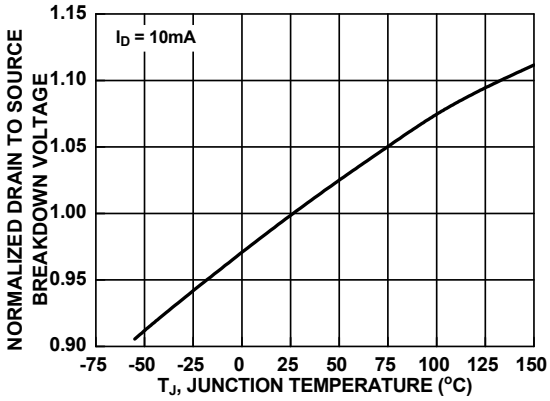


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

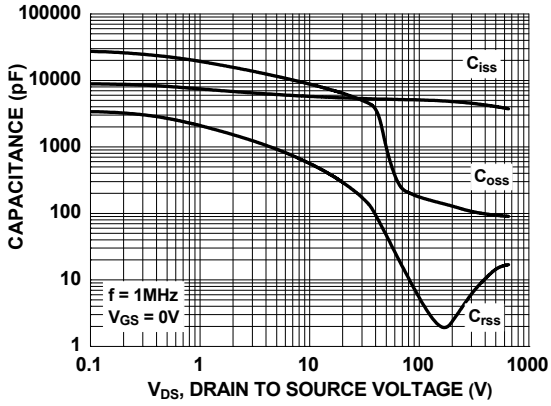


Figure 14. Capacitance vs. Drain to Source Voltage

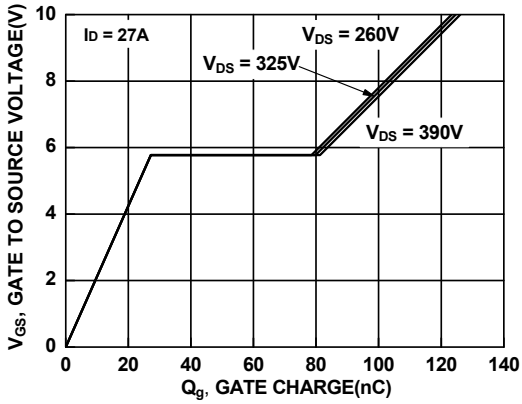


Figure 15. Gate Charge vs. Gate to Source Voltage

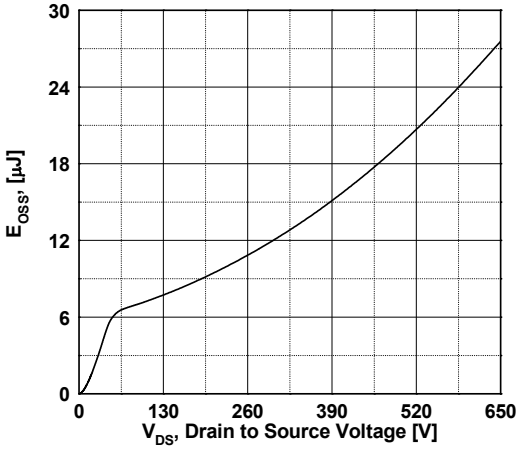


Figure 16. Eoss vs. Drain to Source Voltage

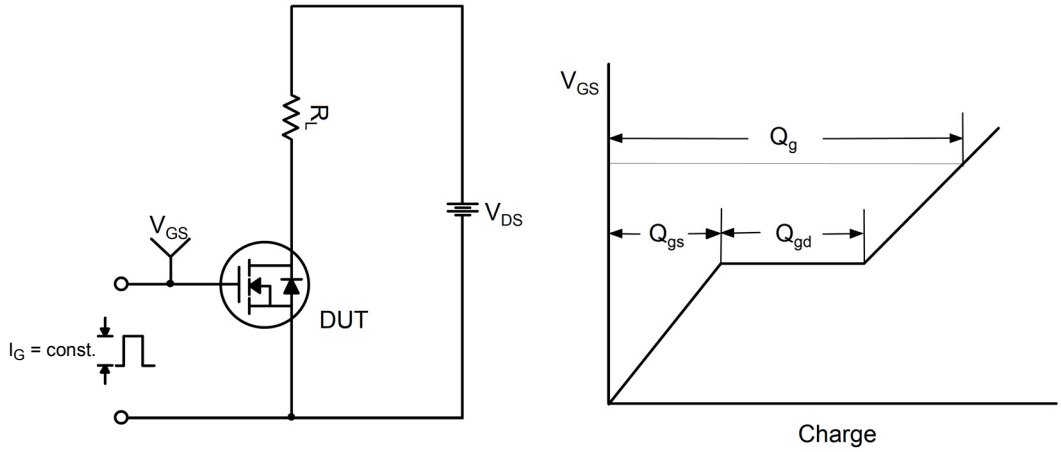


Figure 17. Gate Charge Test Circuit & Waveform

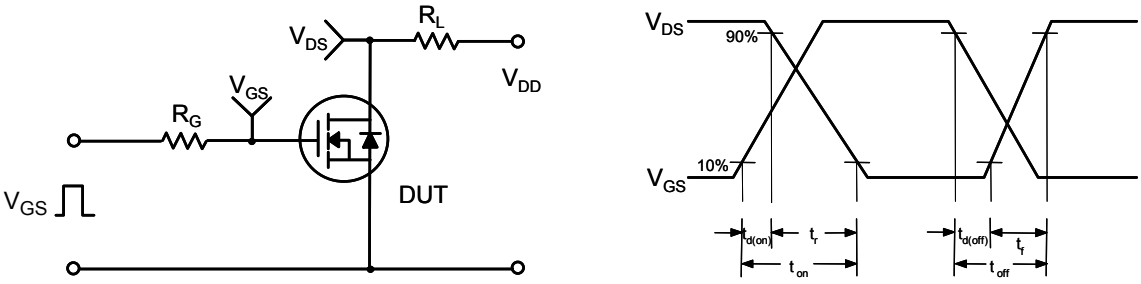


Figure 18. Resistive Switching Test Circuit & Waveforms

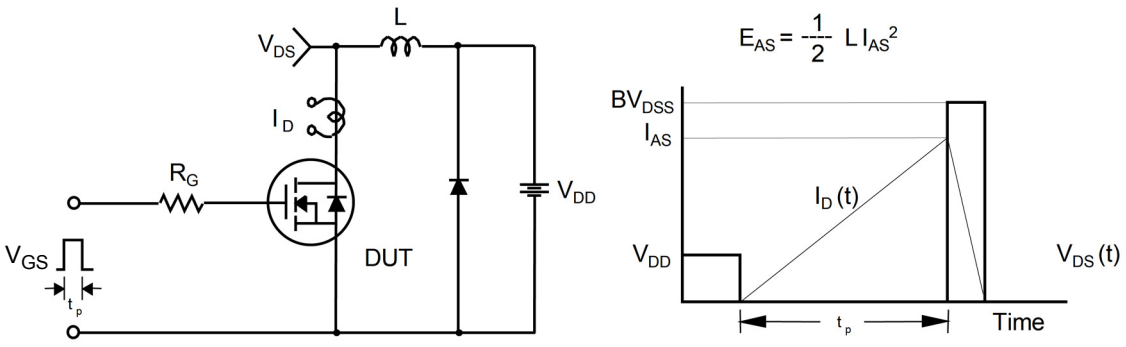


Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms

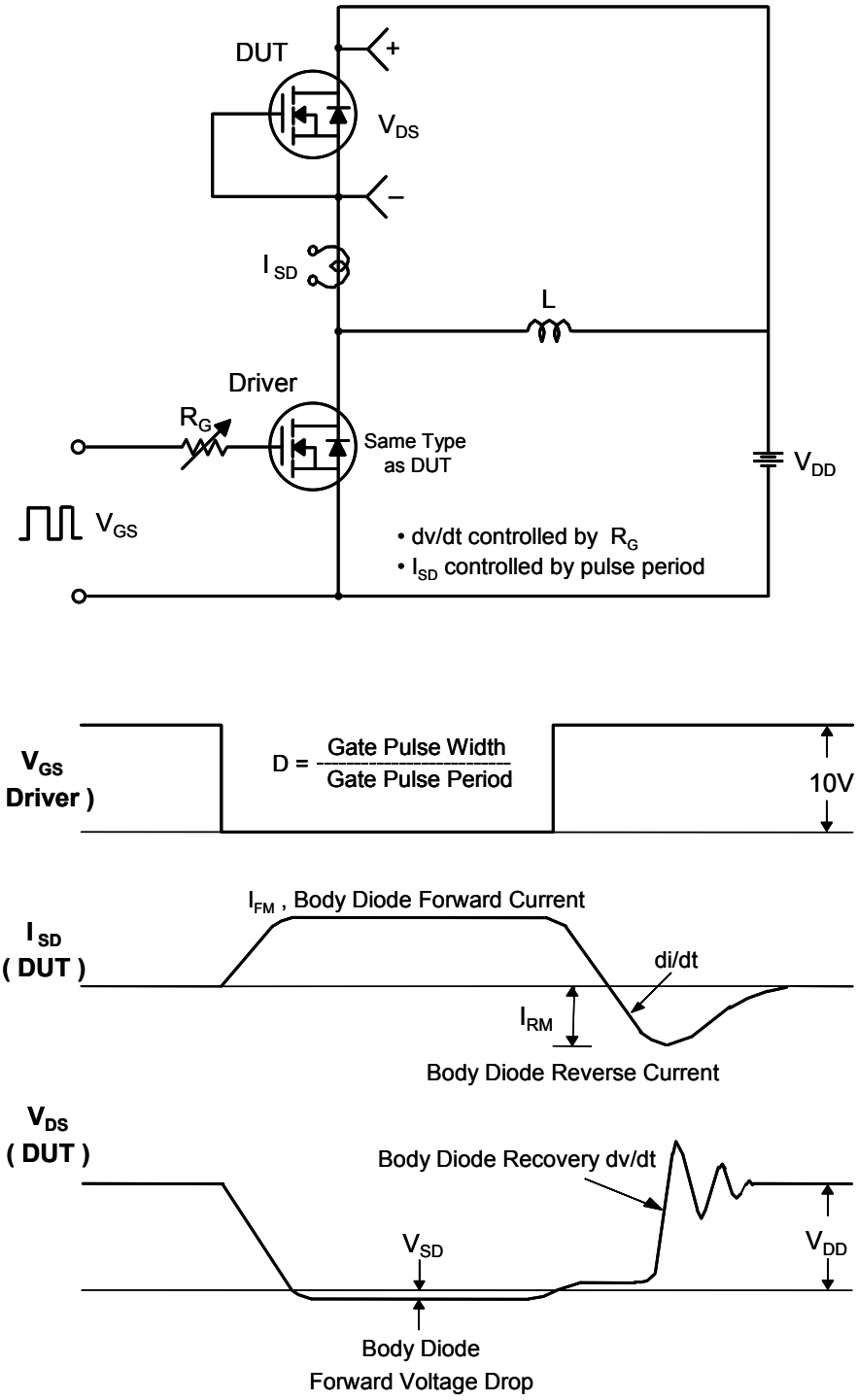
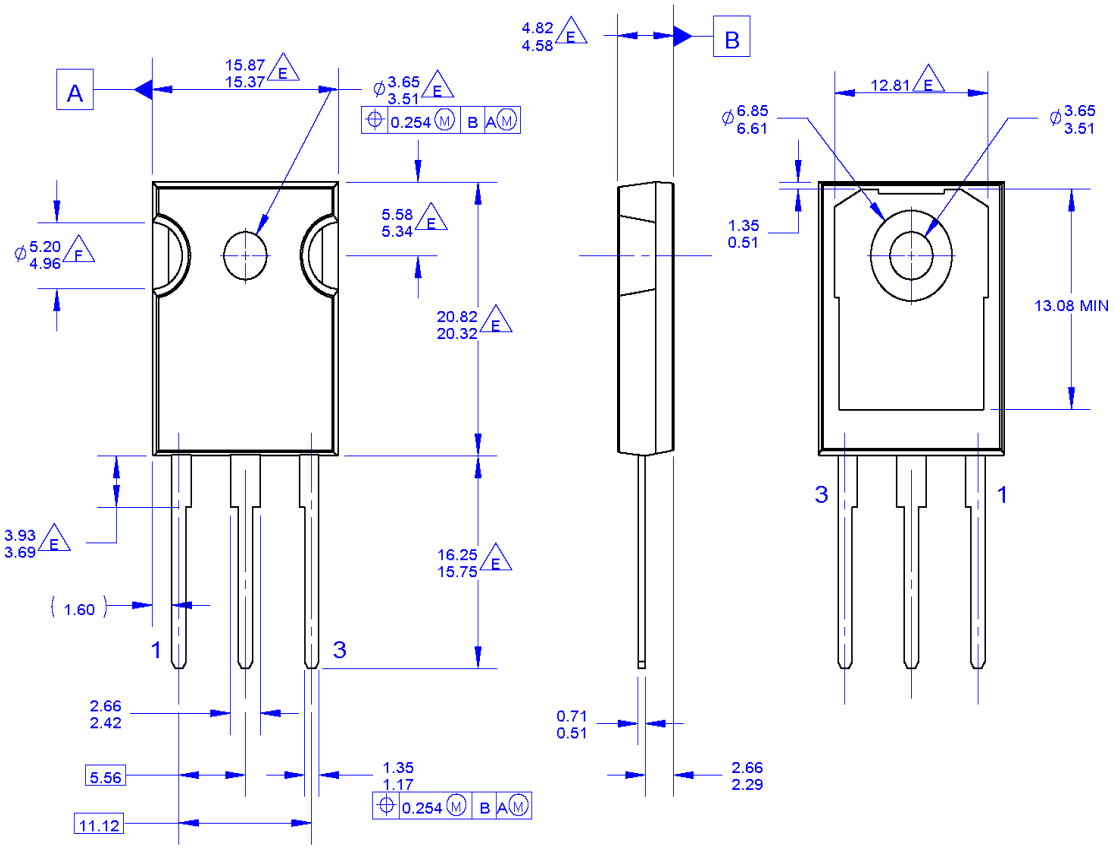


Figure 20. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



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C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DRAWING CONFORMS TO ASME Y14.5 - 1994

E DOES NOT COMPLY JEDEC STANDARD VALUE

F NOTCH MAY BE SQUARE
G. DRAWING FILENAME: MKT-TO247A03_REV03

Figure 21. TO-247, Molded, 3-Lead, Jedec Variation AB

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TinyCalc™
TinyLogic®
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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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