8-Bit Dynamic-RAM Drivers with Three-State Outputs

SN54/74S700/-1 SN54/74S730/-1 SN54/74S731/-1 SN54/74S734/-1

FOR MORE DETAIL SEE SECTION 8

Features/Benefits:

- Provides MOS voltage levels for 16 K and 64 K D-RAMs
- Undershoot of low-going output is less than -0.5 V
- Large capacitive drive capability
- Symmetric rise and fall times due to balanced output impedance
- Glitch-free outputs at power-up and power-down
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- 'S730/734 are exact replacement for the Am2965/66
- 'S700/730/731/734 are pin-compatible with 'S210/240/241/244, and can replace them in many applications
- 'S700-1/730-1/731-1/734-1 have a larger resistor in the output stage for better undershoot protection
- Commercial devices are specified at $V_{CC} \pm 10\%$.

Description:

The 'S700, 'S730, 'S731, and 'S734 are buffers that can drive multiple address and control lines of MOS dynamic RAMs. The 'S700 and 'S730 are inverting drivers and the 'S731 and 'S734 are non-inverting drivers. The 'S700/731 are pin-compatible with the 'S210/241 and have complementary enables. The 'S730 is pin-compatible with the 'S240 and an exact replacement for the Am2965. The 'S734 is pin-compatible with the 'S244 and an exact replacement for the Am2966.

These devices have been designed with an additional internal resistor in the lower output driver transistor circuit, unlike regular 8-bit buffers. This resistor serves two purposes: it causes a slower fall time for a high-to-low transition, and it limits the undershoot without the use of an external series resistor.

The 'S700, 'S730, 'S731, and 'S734 have been designed to drive the highly-capacitive input lines of dynamic RAMs. The drivers provide a guaranteed V_{OH} of V_{CC} - 1.15 volts, limit undershoot to 0.5V, and exhibit a rise time symmetrical to their fall time by having balanced outputs. These features enhance dynamic RAM performance.

For a better-controlled undershoot for lightly capacitive-loaded circuits the 'S700-1, 'S730-1, 'S731-1 and 'S734-1 provide a larger resistor in the lower output stage. Also an improved undershoot volatge of -0.3 V is provided in the 'S700-1 series.

A typical fully-loaded-board dynamic-RAM array consists of 4 banks of dynamic-RAM memory. Each bank has its own $\overline{RAS}$ and $\overline{CAS}$, but has identical address lines. The $\overline{RAS}$ and $\overline{CAS}$ inputs to the array can come from one driver, reducing the skew between the $\overline{RAS}$ and $\overline{CAS}$ signals. Also, only one driver is needed to drive eight address lines of a dynamic RAM. The propagation delays are specified for 50pf and 500pf load capacitances, and the commercial-range specifications are extended to $V_{CC} \pm 10\%$.

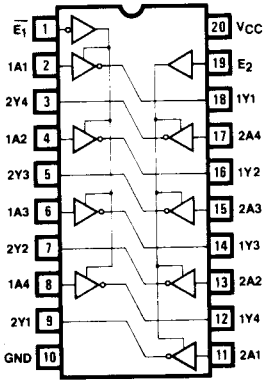
All of the octal devices are packaged in the popular 20-pin SKINNYDIP™.

Ordering Information

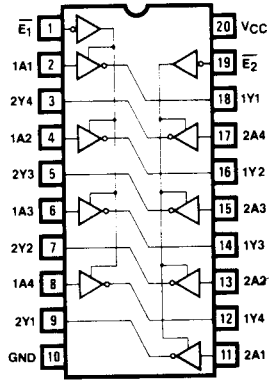
PART NUMBER	PKG	TEMP	ENABLE	POLARITY	POWER
SN54S700/-1	J,W,L	Mil	High-Low	Invert	S
SN74S700/-1	N,J	Com			
SN54S730/-1	J,W,L	Mil	Low		
SN74S730/-1	N,J	Com			
SN54S731/-1	J,W,L	Mil	High-Low	Non-Invert	
SN74S731/-1	N,J	Com			
SN54S734/-1	J,W,L	Mil	Low		
SN74S734/-1	N,J	Com			

Logic Symbols

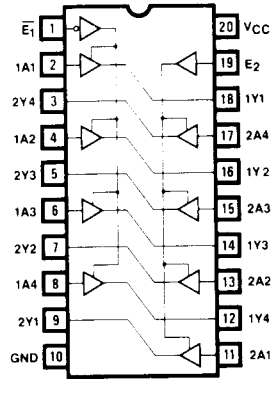
'S700/-1



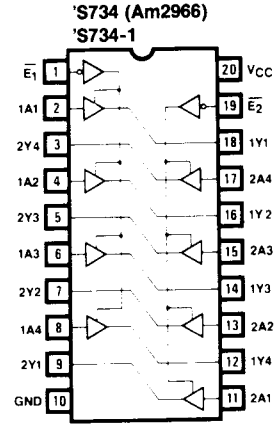
'S730 (Am2965)
'S730-1



'S731/-1



'S734 (Am2966)
'S734-1



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