Five/Ten Output Clock Programmable Buffer

Check for Samples: CDCE18005

FEATURES

- **Universal Input Buffers That Accept LVPECL, LVDS, or LVCMOS Level Signaling**
- **Fully Configurable Outputs Including Frequency, Output Format, and Output Skew**
- **Output Multiplexer That Serves as a Clock Switch Between the Three Reference Inputs and the Outputs**
- **Clock Generation Via AT-Cut Crystal**
- **Integrated EEPROM Determines Device Configuration at Power-up**
- **Low Additive Jitter Performance**
- **Universal Output Blocks Support up to 5 Differential, 10 Single-ended, or Combinations of Differential or Single-ended:**
  - **Low Additive Jitter**
  - **Output Frequency up to 1.5 GHz**
  - **LVPECL, LVDS, LVCMOS, and Special High Output Swing Modes**
  - **Independent Output Dividers Support Divide Ratios from 1–80**
  - **Independent limited Coarse Skew Control on all Outputs**
- **Flexible Inputs:**
  - **Two Universal Differential Inputs Accept Frequencies up to 1500 MHz (LVPECL), 800 MHz (LVDS), or 250 MHz (LVCMOS).**
  - **One Auxiliary Input Accepts Crystal. Auxiliary Input Accepts Crystals in the Range of 2 MHz–42 MHz**
  - **Clock Generator Mode Using Crystal Input.**
- **Typical Power Consumption 1W at 3.3V (see Table 28)**
- **Offered in QFN-48 Package**
- **ESD Protection Exceeds 2kV HBM**
- **Industrial Temperature Range –40°C to 85°C**

APPLICATIONS

- **Data Converter and Data Aggregation Clocking**
- **Wireless Infrastructure**
- **Switches and Routers**
- **Medical Electronics**
- **Military and Aerospace**
- **Industrial**
- **Clock Fan-out**

DESCRIPTION

The CDCE18005 is a high performance clock distributor featuring a high degree of configurability via a SPI interface, and programmable start up modes determined by on-chip EEPROM. Specifically tailored for buffering clocks for data converters and high-speed digital signals, the CDCE18005 achieves low additive jitter in the 50 fs RMS (1) range. The clock distribution block includes five individually programmable outputs that can be configured to provide different combinations of output formats (LVPECL, LVDS, LVCMOS). Each output can also be programmed to a unique output frequency (up to 1.5 GHz (2)) and skew relationship via a programmable delay block. If all outputs are configured in single-ended mode (e.g. LVCMOS), the CDCE18005 supports up to ten outputs. Each output can select one of three clock input sources. The input block includes two universal differential inputs which support frequencies up to 1500 MHz and an auxiliary input that can be configured to connect to a crystal via an on chip oscillator block.

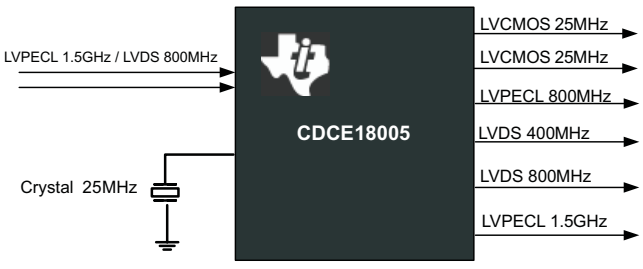


Figure 1. CDCE18005 Application Example

(1) 12 kHz to 20 MHz integration bandwidth.
(2) Maximum output frequency depends on the output format selected

DEVICE INFORMATION

PACKAGE

The CDCE18005 is packaged in a 48-Pin Plastic Quad Flatpack Package with enhanced bottom thermal pad for heat dissipation. The Texas Instruments Package Designator is: **RGZ (S-PQFP-N48)**

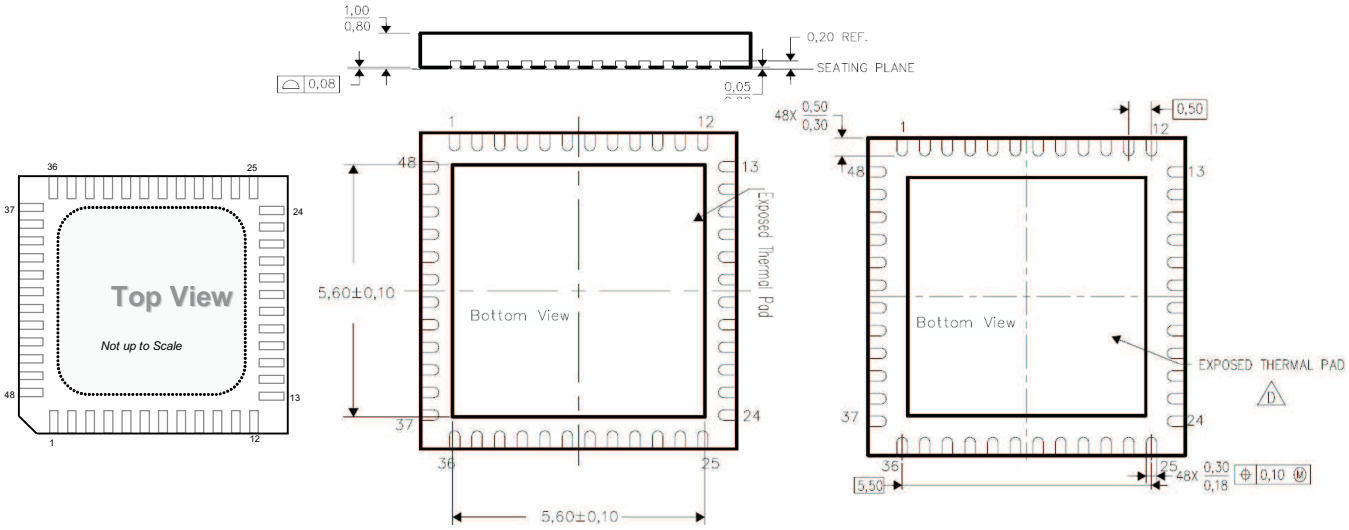
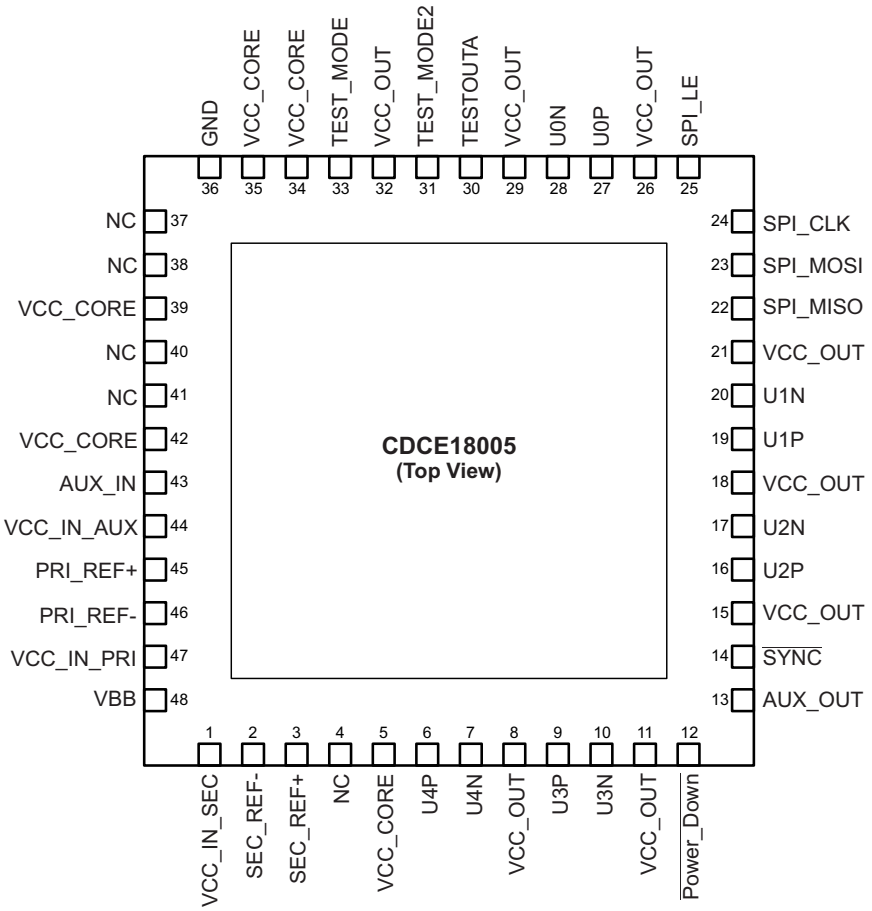


Figure 2. 48-Pin QFN Package Outline



PIN FUNCTIONS(1)

PIN		TYPE	DESCRIPTION
NAME	QFN		
VCC_OUT	8, 11, 15, 18, 21, 26, 29, 32	Power	3.3V Supply for the Output Buffers
VCC_CORE	5, 39, 42, 34, 35	Power	3.3V Core Voltage Circuitry
VCC_IN_PRI	47	A. Power	3.3V References Input Buffer and Circuitry Supply Voltage.
VCC_IN_SEC	1	A. Power	3.3V References Input Buffer and Circuitry Supply Voltage.
VCC_IN_AUX	44	A. Power	3.3V Crystal Oscillator Input Circuitry.
GND	36	Ground	Ground (All internal Ground Pins are connected to the PAD)
GND	PAD	Ground	Ground is on Thermal PAD. See Layout recommendation
SPI_MISO	22	O	3-state LVCMOS Output that is enabled when SPI_LE is asserted low. It is the serial Data Output to the SPI bus interface
SPI_LE	25	I	LVCMOS input, control Latch Enable for Serial Programmable Interface (SPI), with Hysteresis in SPI Mode. The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level "1". The SPI_LE status also impacts whether the device loads the EEPROM into the device registers at power up. SPI_LE has to be logic "0" before the Power_Down# toggles low-to-high in order for the EEPROM to load properly.
SPI_CLK	24	I	LVCMOS input, serial Control Clock Input for the SPI bus interface, with Hysteresis. The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level "1".
SPI_MOSI	23	I	LVCMOS input, Master Out Slave In as a serial Control Data Input to **CDCE18005** for the SPI bus interface. The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level "1".
TEST_MODE	33	I	Pull High or leave unconnected
TEST_MODE2	31	I	Pull High or leave unconnected
$\overline{\text{Power\_Down}}$	12	I	Active Low. Power down mode can be activated via this pin. See Table 14 for more details. The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level "1". SPI_LE has to be HIGH in order for the rising edge of $\overline{\text{Power\_Down}}$ signal to load the EEPROM.
$\overline{\text{SYNC}}$	14	I	Active Low. Sync mode can be activated via this pin. See Table 14 for more details. The input has an internal 150-kΩ, pull-up resistor if left unconnected it will default to logic level “1”.
AUX_IN	43	I	Auxiliary Input is a single ended input including an on-board oscillator circuit so that a crystal may be connected.
AUX_OUT	13	O	Auxiliary Output LVCMOS level that can be programmed via SPI interface to be driven by Output 2 or Output 3.
PRI_REF+	45	I	Universal Input Buffer (LVPECL, LVDS, LVCMOS) positive input for the Primary Reference Clock,
PRI_REF–	46	I	Universal Input Buffer (LVPECL, LVDS) negative input for the Primary Reference Clock. In case of LVCMOS signaling Ground this pin through 1kΩ resistor.
SEC_REF+	3	I	Universal Input Buffer (LVPECL, LVDS, LVCMOS) positive input for the Secondary Reference Clock,
SEC_REF–	2	I	Universal Input Buffer (LVPECL, LVDS,) negative input for the Secondary Reference Clock. In case of LVCMOS signaling Ground this pin through 1kΩ resistor.
TESTOUTA	30	Analog	Analog Test Point for Use for TI Internal Testing. Pull Down to GND Via a 1kΩ Resistor.
NC	4, 37, 38, 40, 41		This Pin is not used
VBB	48	Analog	Capacitor for the internal termination viltage. Connect to a 1µF Capacitor.
U0P:U0N U1P:U1N: U2P:U2N U3P:U3N U4P:U4N	27, 28 19, 20 16,17 9, 10 6, 7	O	The Main outputs of **CDCE18005** are user definable and can be any combination of up to 5 LVPECL outputs, 5 LVDS outputs or up to 10 LVCMOS outputs. The outputs are selectable via SPI interface. The power-up setting is EEPROM configurable.

(1) The internal memory (EEPROM and RAM) are sourced from various power pins. All VCC connections must be powered for proper functionality of the device.

FUNCTIONAL DESCRIPTION

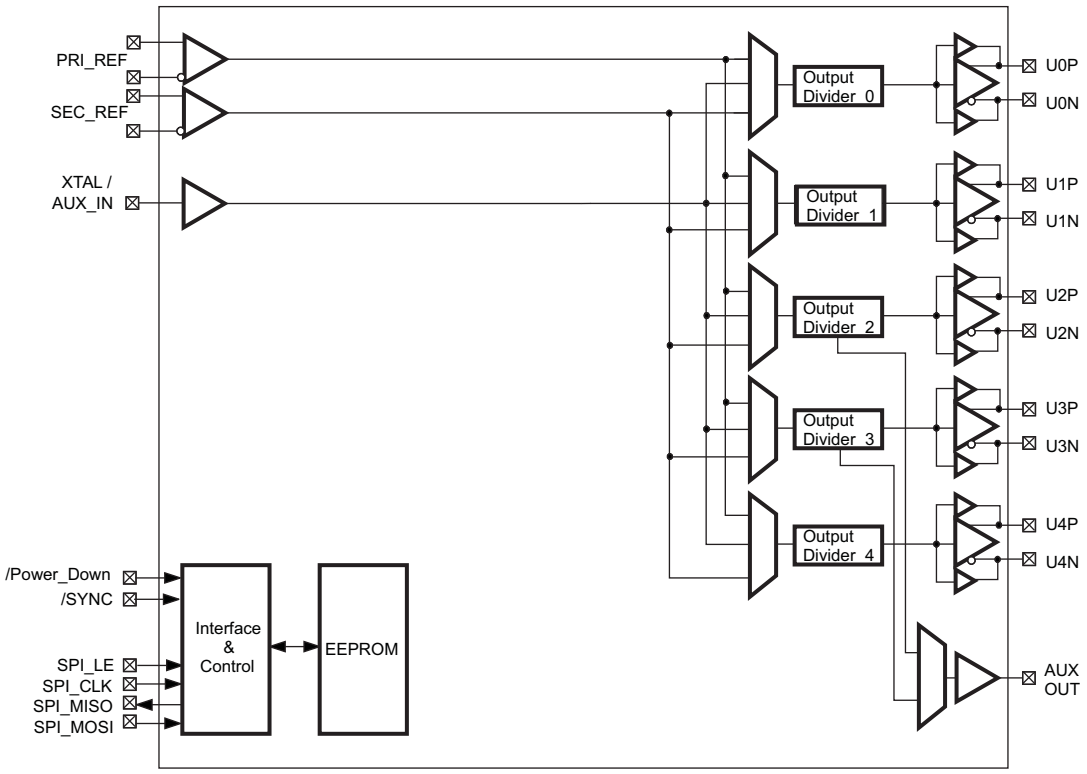


Figure 3. CDCE18005 Block Diagram

The CDCE18005 comprises three primary blocks: the interface and control block, the input block and the output block. In order to determine which settings are appropriate for any specific combination of input/output frequencies, a basic understanding of these blocks is required. The interface and control block determines the state of the CDCE18005 at power-up based on the contents of the on-chip EEPROM. In addition to the EEPROM, the SPI port is available to configure the CDCE18005 by writing directly to the device registers after power-up. The input block buffers three clock signals, converts them to differential signals, and drives them onto an internal clock distribution bus. The output block provides five separate clock channels that are fully programmable and configurable to select and condition one of four internal clock sources

NOTE

This Section of the data sheet provides a high-level description of the features of the CDCE18005 for purpose of understanding its capabilities. For a complete description of device registers and I/O, please refer to the Device Configuration Section.

Interface and Control Block

The CDCE18005 is a highly flexible and configurable architecture and as such contains a number of registers so that the user may specify device operation. The contents of nine 28-bit wide registers implemented in static RAM determine device configuration at all times. The CDCE18005 implements the SPI Interface Mode. SPI Interface Mode is used to access the device RAM and EEPROM either during normal operation (if the host system provides a native SPI interface) or during device configuration (i.e. device programming). During power up the EEPROM content gets copied into the registers after the detection of a valid device power-up. The EEPROM can be locked enabling the designer to implement a fault tolerant design.

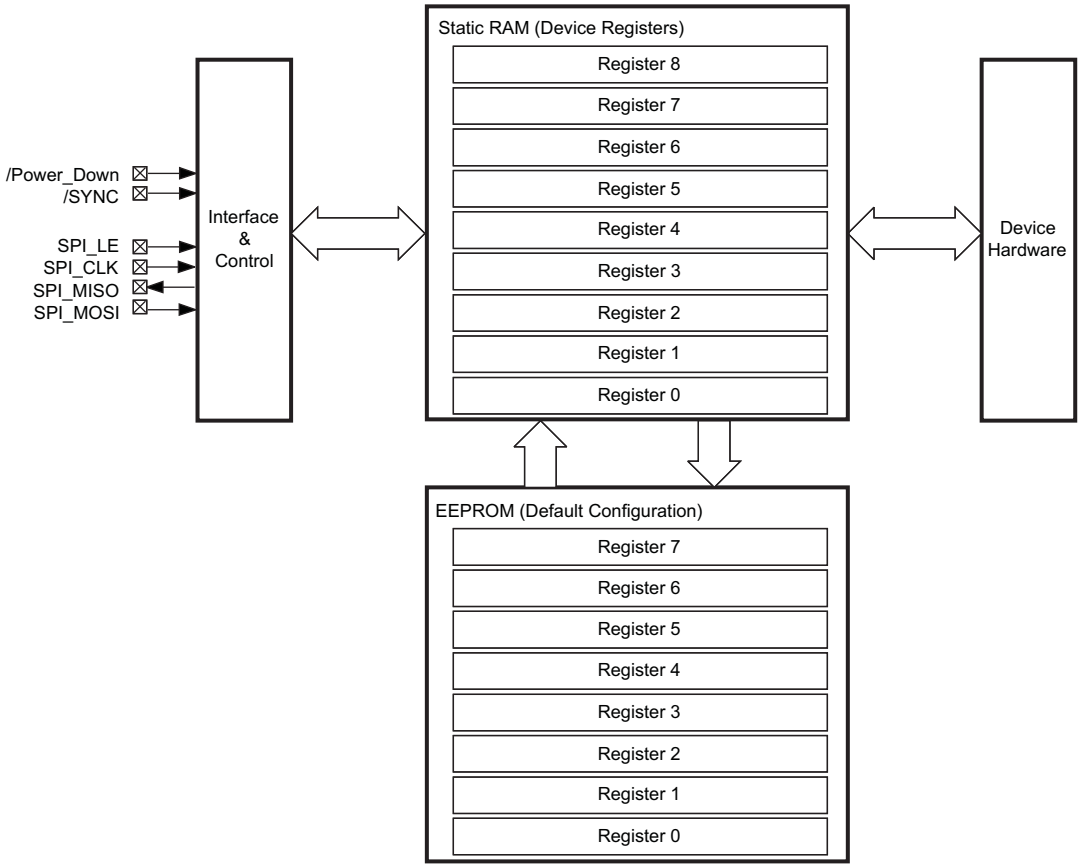


Figure 4. CDCE18005 Interface and Control Block

Input Block

The Input Block includes a pair of Universal Input Buffers and an Auxiliary Input. The Input Block buffers the incoming signals and facilitates signal routing to the Internal Clock Distribution bus. The Internal Clock Distribution Bus connects to all output blocks discussed in the next section. Therefore, a clock signal present on the Internal Clock Distribution bus can appear on any or all of the device outputs.

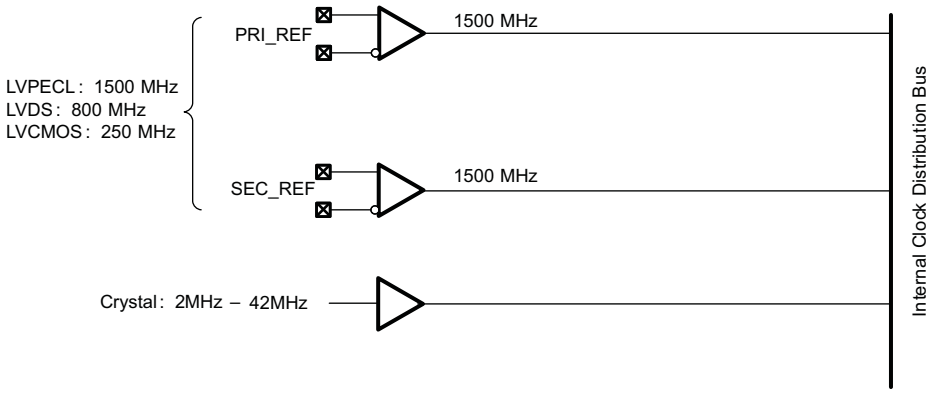


Figure 5. CDCE18005 Input Block

Output Block

Each of the five identical output blocks incorporates an output multiplexer, a clock divider module, and a universal output array as shown.

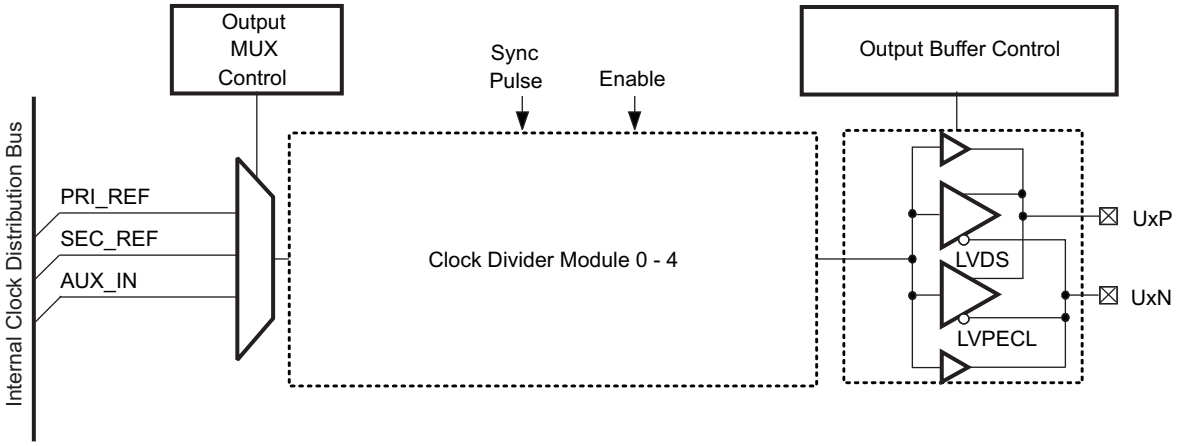


Figure 6. CDCE18005 Output Block (1 of 5)

Clock Divider Module 0–4

The following shows a simplified version of a Clock Divider Module (CDM). If an individual clock output channel is not used, then the user should disable the CDM and Output Buffer for the unused channel to save device power. Each channel includes two 7-bit registers to control the divide ratio used and the clock phase for each output.

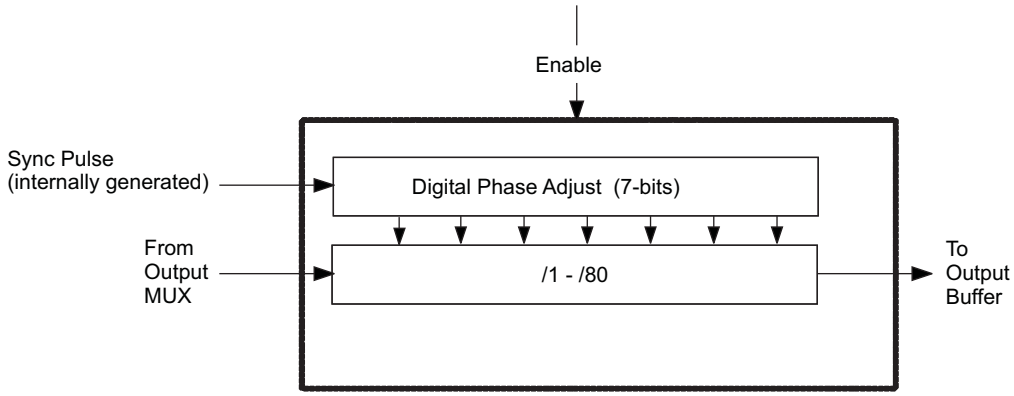


Figure 7. CDCE18005 Output Divider Module (1 of 5)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_{CC}	Supply voltage range(2)	-0.5 to 4.6	V
V_I	Input voltage range(3)	–0.5 to VCC + 0.5	V
V_O	Output voltage range(3)	–0.5 to VCC + 0.5	V
	Input Current (V_I < 0, V_I > V_{CC})	±20	mA
	Output current for LVPECL/LVCMOS Outputs (0 < V_O < V_{CC})	±50	mA
T_J	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated *under recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All supply voltages have to be supplied simultaneously.
(3) The input and output negative voltage ratings may be exceeded if the input and output clamp–current ratings are observed.

THERMAL CHARACTERISTICS

Package Thermal Resistance for QFN (RGZ) Package (1) (2)

AIRFLOW (LFM)		θ_{JP} (°C/W)(3)	θ_{JA} (°C/W)
0	JEDEC Compliant Board (6X6 VIAs on PAD)	2	28.9
100	JEDEC Compliant Board (6X6 VIAs on PAD)	2	20.4
0	Recommended Layout (7X7 VIAs on PAD)	2	27.3
100	Recommended Layout (7X7 VIAs on PAD)	2	20.3

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(2) Connected to GND with 36 thermal vias (0,3 mm diameter).
(3) θ_{JP} (Junction – Pad) is used for the QFN Package, because the main heat flow is from the Junction to the GND-Pad of the QFN.

ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS

recommended operating conditions for the **CDCE18005** device for under the specified Industrial temperature range of –40°C to 85°C

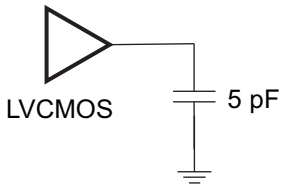
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{CC_IN} , V_{Core}	Analog supply voltage		3	3.3	3.6	
P_{LVPECL}	REF at 491.52 MHz, Outputs are LVPECL	Output 1 = 491.52 MHz (LVCMOS = 245 MHz) Output 2 = 245.76 MHz Output 3 = 122.88 MHz Output 4 = 61.44 MHz Output 5 = 30.72 MHz		1.6		W
P_{LVDS}	REF at 491.52 MHz, Outputs are LVDS			1.3		W
P_{LVCMOS}	REF at 491.52 MHz, Outputs are LVCMOS			1.5		W
P_{OFF}	REF at 491.52 MHz	Dividers are disabled. Outputs are disabled.		0.45		W
P_{PD}		Device is powered down		20		mW
DIFFERENTIAL INPUT MODE (PRI_REF, SEC_REF)						
V_{IN}	Differential input amplitude ($V_{IN} – V_{\overline{IN}}$)		0.1		1.3	V
V_{IC}	Common-mode input voltage		1.0		V_{CC}–0.3	V
I_{IH}	Differential input current high (no internal termination)	$V_I = V_{CC}$, V_{CC} = 3.6 V			20	µA
I_{IL}	Differential input current low (no internal termination)	V_I = 0 V, V_{CC} = 3.6 V	–20		20	µA
	Input Capacitance on PRI_REF, SEC_REF			3		pF
CRYSTAL INPUT SPECIFICATIONS						
	On-chip load capacitance			8	10	pF
	Equivalent series resistance (ESR)				50	Ω
LVCMOS INPUT MODE (SPI_CLK, SPI_MOSI, SPI_LE, $\overline{\text{Power\_Down}}$, $\overline{\text{SYNC}}$, PRI_REF, SEC_REF)						
	Low-level input voltage LVCMOS,		0		0.3 V_{CC}	V
	High-level input voltage LVCMOS		0.7 V_{CC}		V_{CC}	V
V_{IK}	LVCMOS input clamp voltage	V_{CC} = 3 V, I_I = –18 mA			–1.2	V
I_{IH}	LVCMOS input current	$V_I = V_{CC}$, V_{CC} = 3.6 V				µA
I_{IL}	LVCMOS input (Except PRI_REF and SEC_REF)	V_I = 0 V, V_{CC} = 3.6 V	–10		–40	µA
I_{IL}	LVCMOS input (PRI_REF and SEC_REF)	V_I = 0 V, V_{CC} = 3.6 V	–10		10	µA
C_I	Input capacitance (LVCMOS signals)	V_I = 0 V or V_{CC}		3		pF

ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS (Continued)

recommended operating conditions for the **CDCE18005** device for under the specified Industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
SPI OUTPUT (MISO)							
I_{OH}	High-level output current	V_{CC} = 3.3 V,	V_O = 1.65 V		–30		mA
I_{OL}	Low-level output current	V_{CC} = 3.3 V,	V_O = 1.65 V		33		mA
V_{OH}	High-level output voltage for LVCMOS outputs	V_{CC} = 3 V,	I_{OH} = −100 µA	V_{CC}–0.5			V
V_{OL}	Low-level output voltage for LVCMOS outputs	V_{CC} = 3 V,	I_{OL} = 100 µA			0.3	V
C_O	Output capacitance on MISO	VCC = 3.3 V; VO = 0 V or VCC			3		pF
I_{OZH}	3-state output current	V_O = V_{CC} , V_O = 0 V			5		µA
I_{OZL}					–5		
VBB							
VBB	Termination voltage for reference inputs.	I_{BB} = –0.2 mA, Depending on the setting.		0.9		1.9	V
INPUT BUFFERS INTERNAL TERMINATION RESISTORS (PRI_REF and SEC_REF)							
	Termination resistance	Single ended			50		Ω
LVCMOS OUTPUT / AUXILIARY OUTPUT							
f_{clk}	Output frequency, see Figure Below	Load = 5 pF to GND				250	MHz
V_{OH}	High-level output voltage for LVCMOS outputs	V_{CC} = min to max	I_{OH} = –100 µA	V_{CC} –0.5			
V_{OL}	Low-level output voltage for LVCMOS outputs	V_{CC} = min to max	I_{OL} =100 µA			0.3	V
I_{OH}	High-level output current	V_{CC} = 3.3 V	V_O = 1.65 V		–30		mA
I_{OL}	Low-level output current	V_{CC} = 3.3 V	V_O = 1.65 V		33		mA
$t_{pd(LH)}$/ $t_{pd(HL)}$	Propagation delay from PRI_REF or SEC_REF to Outputs (LVCMOS to LVCMOS)	V_{CC}/2 to V_{CC}/2			4		ns
$t_{sk(o)}$	Skew, output to output For Y0 to Y4	All Outputs set at 200 MHz, Reference = 200 MHz			75		ps
C_O	Output capacitance on Y0 to Y4	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}			5		pF
I_{OZH}	3-State LVCMOS output current	V_O = V_{CC}			5		µA
I_{OZL}		V_O = 0 V			–5		µA
I_{OPDH}	Power Down output current	V_O = V_{CC}				25	µA
I_{OPDL}		V_O = 0 V				5	µA
	Duty cycle LVCMOS	50% / 50% input duty cycle		45%		55%	
$t_{slew-rate}$	Output rise/fall slew rate			3.6	5.2		V/ns

(1) All typical values are at V_{CC} = 3.3 V, temperature = 25°C



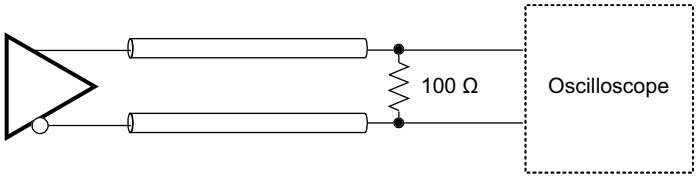
ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS (Continued)

recommended operating conditions for the **CDCE18005** device for under the specified Industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
LVDS OUTPUT						
f_{clk}	Output frequency	Configuration Load (100 Ω)			800	MHz
$\|V_{OD}\|$	Differential output voltage	R_L = 100 Ω	270		550	mV
ΔV_{OD}	LVDS VOD magnitude change				50	mV
V_{OS}	Offset Voltage	–40°C to 85°C		1.24		V
ΔV_{OS}	VOS magnitude change			40		mV
	Short circuit Vout+ to ground	VOUT = 0			27	mA
	Short circuit Vout– to ground	VOUT = 0			27	mA
$t_{pd(LH)}/t_{pd(HL)}$	Propagation delay from PRI_REF or SEC_REF to outputs (LVDS to LVDS)	Crosspoint to Crosspoint		3.1		ns
$t_{sk(o)}$ (2)	Skew, output to output For Y0 to Y4	All Outputs set at 200 MHz Reference = 200 MHz		25		ps
C_O	Output capacitance on Y0 to Y4	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}		5		pF
I_{OPDH}	Power down output current	$V_O = V_{CC}$			25	µA
I_{OPDL}	Power down output current	V_O = 0 V			5	µA
	Duty cycle	50% / 50% input duty cycle	45%		55%	
t_r / t_f	Rise and fall time	20% to 80% of $V_{OUT(PP)}$	110	160	190	ps
LVCMOS-TO-LVDS						
t_{skP_c}	Output skew between LVCMOS and LVDS outputs(3)	Crosspoint to VCC/2	0.9	1.4	1.9	ns

(1) All typical values are at V_{CC} = 3.3 V, temperature = 25°C
(2) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
(3) The phase of LVCMOS is lagging in reference to the phase of LVDS.

LVDS DC Termination Test



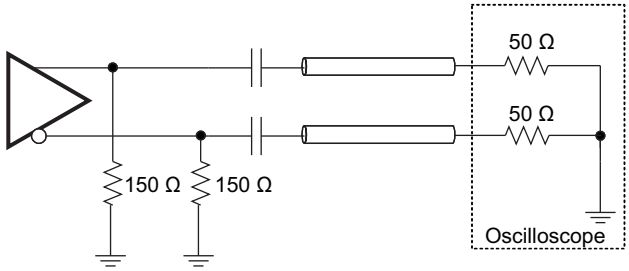
ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS (Continued)

recommended operating conditions for the **CDCE18005** device for under the specified Industrial temperature range of –40°C to 85°C

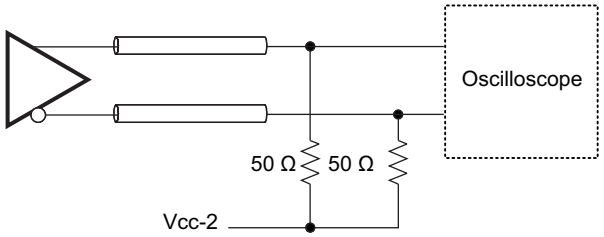
PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
LVPECL OUTPUT						
f_{clk}	Output frequency	Configuration load (Figures below)			1500	MHz
V_{OH}	LVPECL high-level output voltage load		V_{CC} –1.06		V_{CC} –0.88	V
V_{OL}	LVPECL low-level output voltage load		V_{CC} –2.02		V_{CC} –1.58	V
$\|V_{OD}\|$	Differential output voltage		610		970	mV
$t_{pd(LH)}$/ $t_{pd(HL)}$	Propagation delay from PRI_REF or SEC_REF to outputs (LVPECL to LVPECL)	Crosspoint to Crosspoint		3.4		ns
$t_{sk(o)}$	Skew, output to output For Y0 to Y4	All Outputs set at 200 MHz Reference = 200MHz		25		ps
C_O	Output capacitance on Y0 to Y4	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}		5		pF
I_{OPDH}	Power Down output current	V_O = V_{CC}			25	µA
I_{OPDL}		V_O = 0 V			5	µA
	Duty Cycle	50% / 50% input duty cycle	45%		55%	
t_r / t_f	Rise and fall time	20% to 80% of Voutpp	55	75	135	ps
LVDS-TO-LVPECL						
t_{skP_C}	Output skew between LVDS and LVPECL outputs	Crosspoint to Crosspoint	0.9	1.1	1.3	ns
LVCMOS-TO-LVPECL						
t_{skP_C}	Output skew between LVCMOS and LVPECL outputs	V_{CC}/2 to crosspoint	–150	260	700	ps
LVPECL HI-SWING OUTPUT						
V_{OH}	LVPECL high-level output voltage load		V_{CC} –1.11		V_{CC} –0.87	V
V_{OL}	LVPECL low-level output voltage load		V_{CC} –2.06		V_{CC} –1.73	V
$\|V_{OD}\|$	Differential output voltage		760		1160	mV
t_r / t_f	Rise and fall time	20% to 80% of Voutpp	55	75	135	ps

(1) All typical values are at V_{CC} = 3.3 V, temperature = 25°C

LVPECL AC Termination Test



LVPECL DC Termination Test



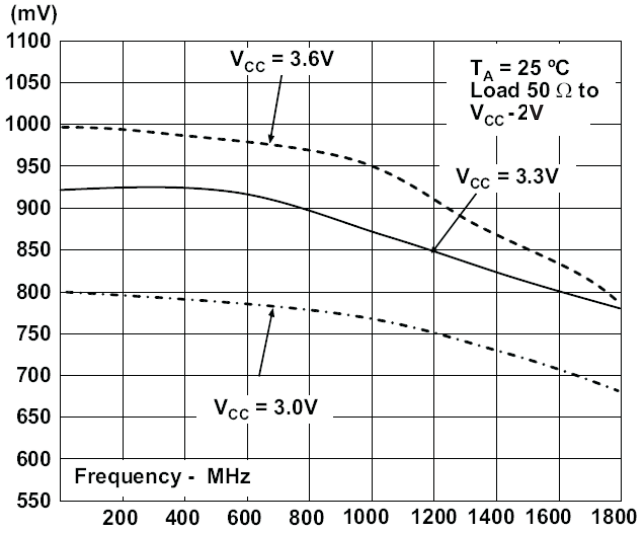


Figure 8. LVPECL Output Swing vs Frequency

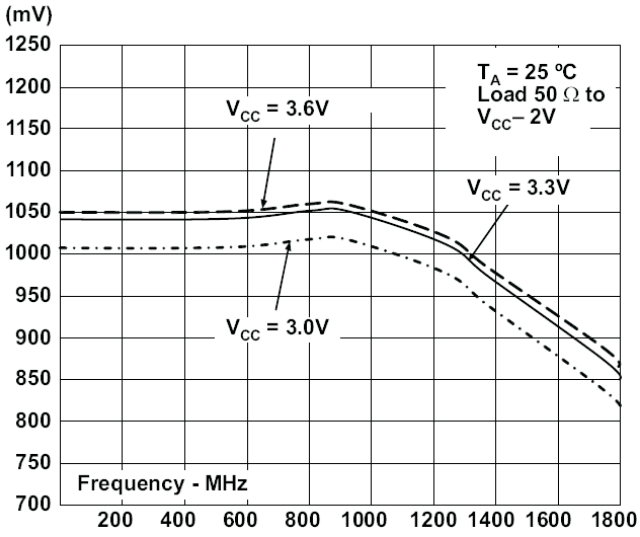


Figure 9. HI Swing LVPECL Output Swing vs Frequency

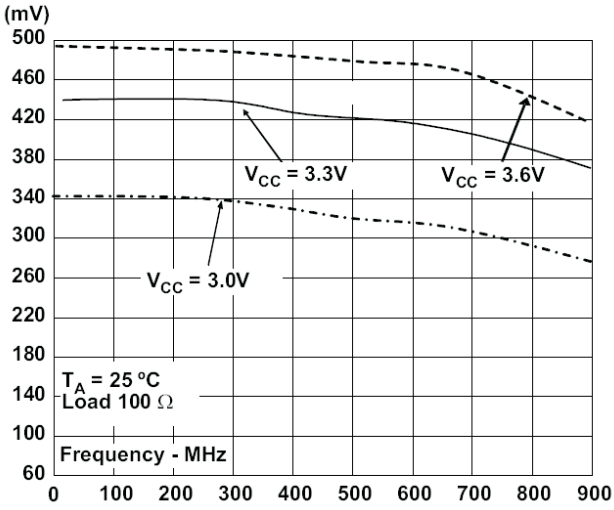


Figure 10. LVDS Output Swing vs Frequency

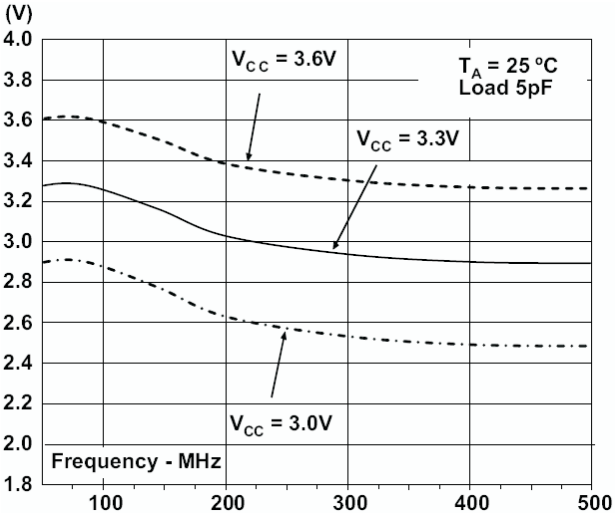


Figure 11. LVCMOS Output Swing vs Frequency

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load and operating free air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
PRI_REF/SEC_REF INPUT REQUIREMENTS					
f_{max}	For Single ended Inputs (LVCMOS) on PRI_REF and SEC_REF			250	MHz
	For Differential Inputs on PRI_REF and SEC_REF			1500	MHz
AUX_IN Input REQUIREMENTS					
f_{REF}	AT-Cut Crystal Input	2		42	MHz
	Drive level	100			µW
	Maximum Shunt Capacitance			7	pF
$\overline{\text{Power\_Down}}$, $\overline{\text{SYNC}}$ REQUIREMENTS					
t_r/ t_f	Rise and fall time of the $\overline{\text{Power\_Down}}$, $\overline{\text{SYNC}}$, signal from 20% to 80% of V_{CC}			4	ns

PHASE NOISE ANALYSIS

Table 1. Output Phase Noise for a 491.52 MHz External Reference

Phase Noise Specifications under following configuration: REF = 491.52 MHz Diff, LVPECL					
Phase Noise	**Reference 491.52 MHz**	**LVPECL 491.52 MHz**	**LVDS 245.52 MHz**	**LVCMOS 122.88 MHz**	**Unit**
10 Hz	-86	-84	-90	-96	dBc/Hz
100 Hz	-100	-100	-105	-111	dBc/Hz
1 kHz	-108	-109	-115	-121	dBc/Hz
10 kHz	-130	-130	-136	-140	dBc/Hz
100 kHz	-135	-135	-140	-145	dBc/Hz
1 MHz	-138	-142	-143	-148	dBc/Hz
10 MHz	-150	-148	-150	-153	dBc/Hz
20 MHz	-150	-148	-150	-152	dBc/Hz
Jitter RMS 10k–20MHz	84	93	150	206	fs

Table 2. Output Phase Noise for a 25 MHz Crystal Reference

Phase Noise Specifications under following configuration: REF = 25 MHz, SE:LVCMOS				
PHASE NOISE	**LVPECL 25 MHz**	**LVDS 25 MHz**	**LVCMOS 25 MHz**	**UNIT**
10 Hz	-83	-82	-82	dBc/Hz
100 Hz	-115	-116	-115	dBc/Hz
1 kHz	-142	-142	-141	dBc/Hz
10 kHz	-152	-149	-151	dBc/Hz
100 kHz	-155	-151	-155	dBc/Hz
1 MHz	-157	-151	-158	dBc/Hz
5 MHz	-157	-151	-158	dBc/Hz
Jitter RMS 10k–5MHz	275	345	249	fs

DEVICE CONFIGURATION

The Functional Description Section described three different functional blocks contained within the CDCE18005. Figure 12 depicts these blocks along with a high-level functional block diagram of the circuit elements comprising each block. The balance of this section focuses on a detailed discussion of each functional block from the perspective of how to configure them.

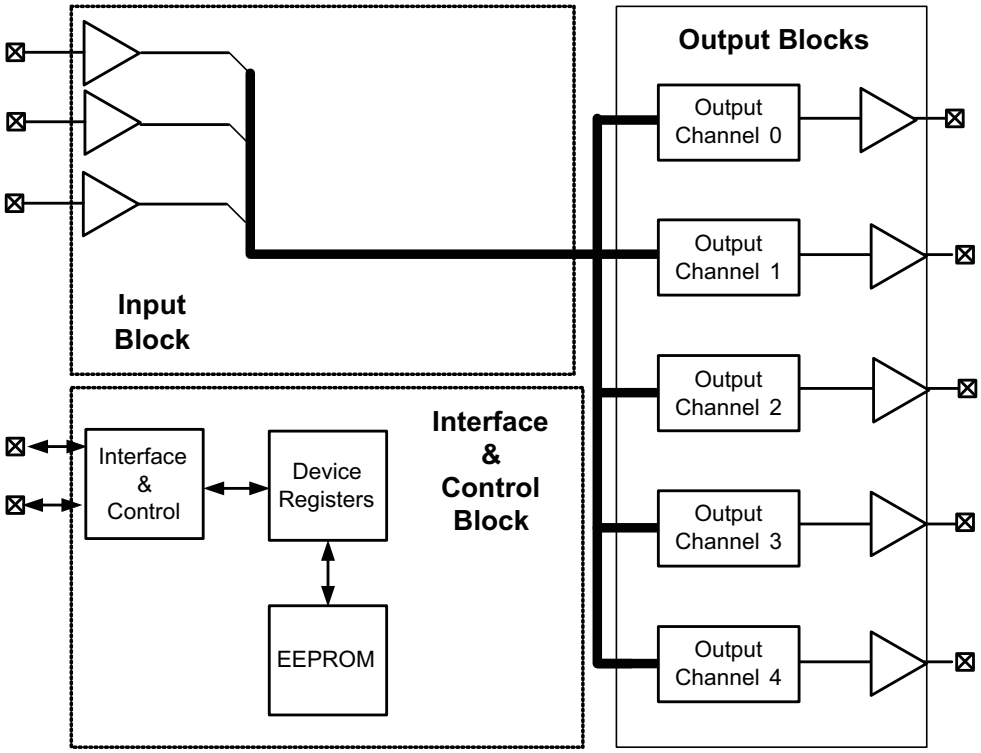


Figure 12. CDCE18005 Circuit Blocks

Throughout this section, references to Device Register memory locations follow the following convention:

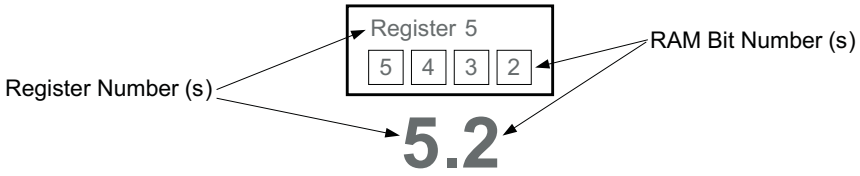


Figure 13. Device Register Reference Convention

INTERFACE AND CONTROL BLOCK

The Interface and Control Block includes a SPI interface, two control pins, a non-volatile memory array in which the device stores default configuration data, and an array of device registers implemented in Static RAM. This RAM, also called the device registers, configures all hardware within the CDCE18005.

SPI (Serial Peripheral Interface)

The serial interface of CDCE18005 is a simple bidirectional SPI interface for writing and reading to and from the device registers. It implements a low speed serial communications link in a master/slave topology in which the CDCE18005 is a slave. The SPI consists of four signals:

- **SPI_CLK:** Serial Clock (Output from Master) – the CDCE18005 clocks data in and out on the rising edge of SPI_CLK. Data transitions therefore occur on the falling edge of the clock.
- **SPI_MOSI:** Master Output Slave Input (Output from Master).
- **SPI_MISO:** Master Input Slave Output (Output from Slave).
- **SPI_LE:** Latch Enable (Output from Master). The falling edge of SPI_LE initiates a transfer. If SPI_LE is high, no data transfer can take place.

SPI Interface Master

The Interface master can be designed using a FPGA or a micro controller. The CDCE18005 acts as a slave to the SPI master and only supports nonconsecutive read and write command. The SPI clock should start and stop with respect to the SPI_LE signal as shown in Figure 14 SPI_MOSI, SPI_CLK and SPI_LE are generated by the SPI Master. SPI_MISO is generated by the SPI slave the CDCE18005.

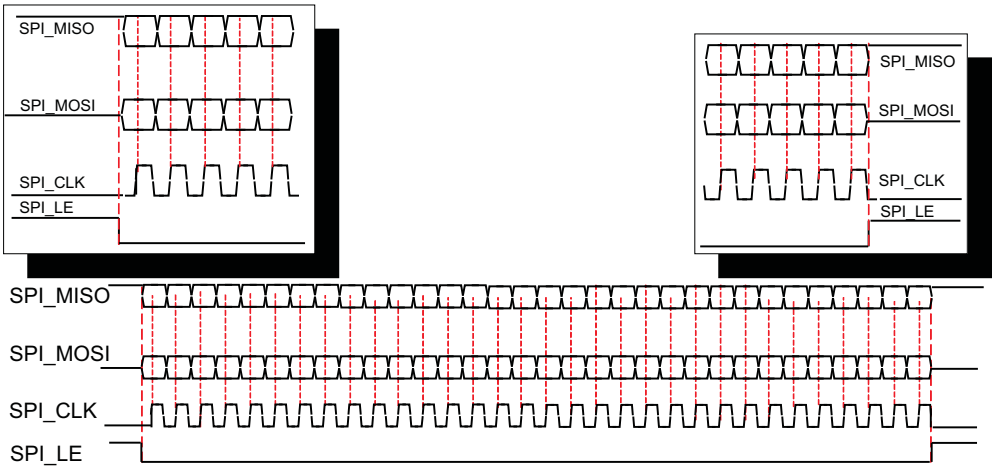


Figure 14. CDCE18005 SPI Read/Write Command

SPI Consecutive Read/Write Cycles to the CDCE18005

Figure 15 Illustrates how two consecutive SPI cycles are performed between a SPI Master and the CDCE18005 SPI Slave.

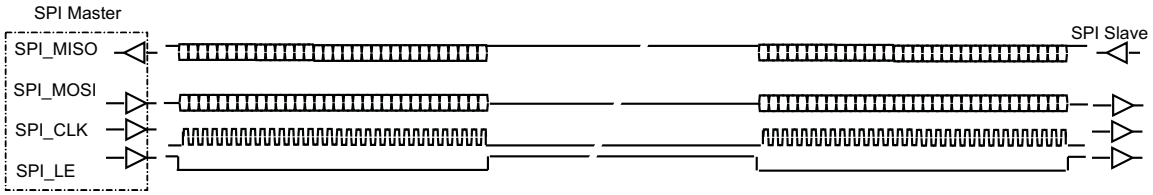


Figure 15. Consecutive Read/Write Cycles

Writing to the CDCE18005

Figure 16 illustrates a Write to RAM operation. Notice that the latching of the first data bit in the data stream (Bit 0) occurs on the first rising edge of SPI_CLK after SPI_LE transitions from a high to a low. For the CDCE18005, data transitions occur on the falling edge of SPI_CLK. A rising edge on SPI_LE signals to the CDCE18005 that the transmission of the last bit in the stream (Bit 31) has occurred.

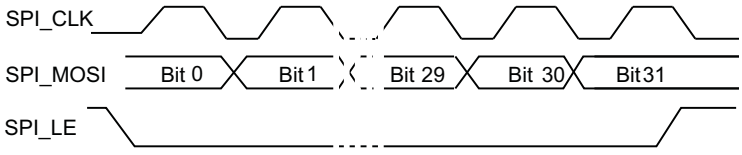


Figure 16. CDCE18005 SPI Write Operation

Reading from the CDCE18005

Figure 17 shows how the CDCE18005 executes a Read Command. The SPI master first issues a Read Command to initiate a data transfer from the CDCE18005 back to the host (see Table 5)This command specifies the address of the register of interest. By transitioning SPI_LE from a low to a high, the CDCE18005 resolves the address specified in the appropriate bits of the data field. The host drives SPI_LE low and the CDCE18005 presents the data present in the register specified in the Read Command on SPI_MISO.

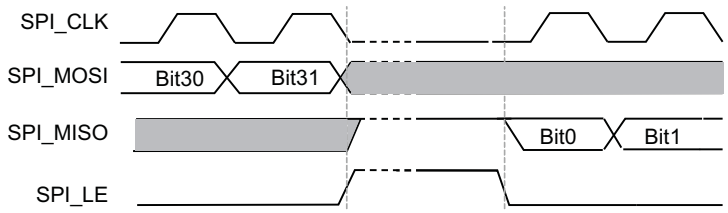


Figure 17. CDCE18005 SPI Read Operation

Writing to EEPROM

After the CDCE18005 detects a power-up and completes a reset cycle, the device copies the contents of the on-chip EEPROM into the Device Registers. (SPI_LE signal has to be HIGH in order for the EEPROM to load correctly during the rising edge of Power_Down signal).

The host issues one of two special commands shown in Table 6 to copy the contents of Device Registers 0 through 7 (a total of 224 bits) into EERPOM. They include:

- Copy RAM to EEPROM – Unlock, Execution of this command can happen many times.
- Copy RAM to EEPROM – Lock: Execution of this command can happen only once; after which the EEPROM is **permanently locked**.

After either command is initiated, power must remain stable and the host must not access the CDCE18005 for at least 50 ms to allow the EEPROM to complete the write cycle and to avoid the possibility of EEPROM corruption.

SPI CONTROL INTERFACE TIMING

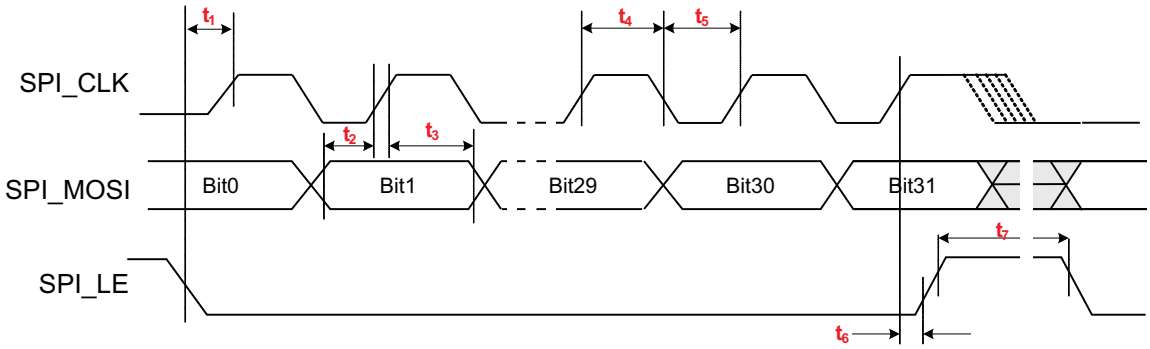


Figure 18. Timing Diagram for SPI Write Command

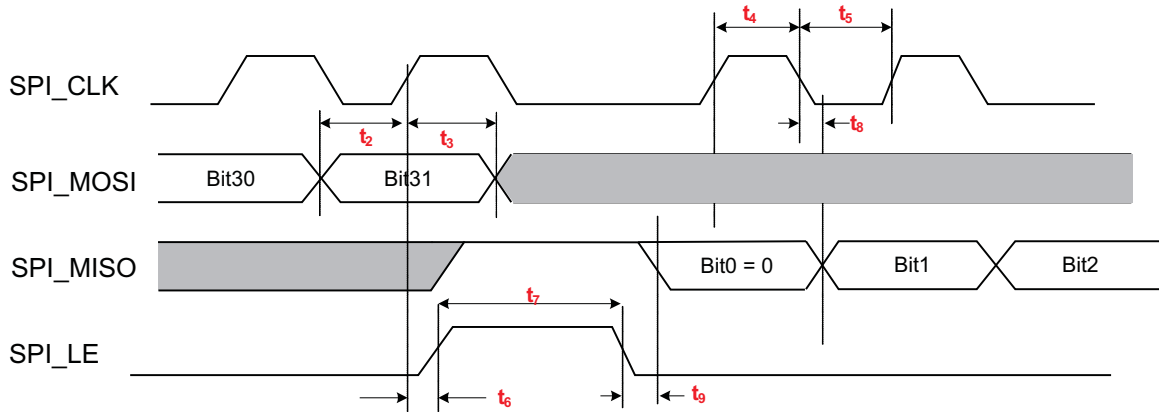


Figure 19. Timing Diagram for SPI Read Command

Table 3. SPI Bus Timing Characteristics

SPI BUS TIMINGS					
PARAMETER		**MIN**	**TYP**	**MAX**	**UNIT**
f_{Clock}	Clock Frequency for the SPI_CLK			20	MHz
t_1	SPI_LE to SPI_CLK setup time	10			ns
t_2	SPI_MOSI to SPI_CLK setup time	10			ns
t_3	SPI_MOSI to SPI_CLK hold time	10			ns
t_4	SPI_CLK high duration	25			ns
t_5	SPI_CLK low duration	25			ns
t_6	SPI_CLK to SPI_LE Hold time	10			ns
t_7	SPI_LE Pulse Width	20			ns
t_8	SPI_CLK to MISO data valid			10	ns
t_9	SPI_LE to SPI_MISO Data Valid			10	ns

CDCE18005 SPI Command Structure

The CDCE18005 supports four commands issued by the Master via the SPI:

- Write to RAM
- Read Command
- Copy RAM to EEPROM – unlock
- Copy RAM to EEPROM – lock

Table 4 provides a summary of the CDCE18005 SPI command structure. The host (master) constructs a Write to RAM command by specifying the appropriate register address in the address field and appends this value to the beginning of the data field. Therefore, a valid command stream must include 32 bits, transmitted LSB first. The host must issue a Read Command to initiate a data transfer from the CDCE18005 back to the host. This command specifies the address of the register of interest in the data field.

Table 4. CDCE18005 SPI Command Structure

			Data Field (28 Bits)																												Addr Field (4 Bits)			
Register	**Operation**	**NVM**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**3**	**2**	**1**	**0**
0	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0
1	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1
2	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	0
3	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	1
4	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	0
5	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	1
6	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1	0
7	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1	1
8	Status/Control	No	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	0
Instruction	Read Command	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	A	A	A	A	1	1	1	0
Instruction	RAMM EEPROM	Unlock(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Instruction	RAMM EEPROM	Lock	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1

(1) **CAUTION:** After execution of this command, the EEPROM is permanently locked. After locking the EEPROM, device configuration can only be changed via Write to RAM after power-up; however, the EEPROM can no longer be changed

The CDCE18005 on-board EEPROM has been factory preset to the default settings listed in the table below.

REGISTER	DEFAULT SETTING
REG0000	8140000
REG0001	8140000
REG0002	8140000
REG0003	8140000
REG0004	8140000
REG0005	0000096
REG0006	0000000
REG0007	9400000

The default configuration programmed in the device is set to: PRI_REF (set to LVPECL) feeding all outputs. Output dividers are set to DIVIDE by 1. All outputs are set to LVPECL.

Device Registers: Register 0 Address 0x00

Table 5. CDCE18005 Register 0 Bit Definitions

<table>
<tr><th>RAM BIT</th><th>BIT NAME</th><th>RELATED BLOCK</th><th>DESCRIPTION/FUNCTION</th><th></th></tr>
<tr><td>0</td><td>RESERVED</td><td rowspan="4"></td><td rowspan="4">Always Set to "0" for Proper Operation</td><td>EEPROM</td></tr>
<tr><td>1</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>2</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>3</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>4</td><td>OUTMUX0SELX</td><td>Output 0</td><td rowspan="2">OUTPUT MUX “0” Select. Selects the Signal driving Output Divider ”0”
(X,Y) = 00: PRI_REF, 01: SEC_REF, 10: AUX_IN, 11: Reserved</td><td>EEPROM</td></tr>
<tr><td>5</td><td>OUTMUX0SELY</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>6</td><td>PH0ADJC0</td><td>Output 0</td><td rowspan="7">Coarse phase adjust select for output divider “0”</td><td>EEPROM</td></tr>
<tr><td>7</td><td>PH0ADJC1</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>8</td><td>PH0ADJC2</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>9</td><td>PH0ADJC3</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>10</td><td>PH0ADJC4</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>11</td><td>PH0ADJC5</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>12</td><td>PH0ADJC6</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>13</td><td>OUT0DIVRSEL0</td><td>Output 0</td><td rowspan="7">OUTPUT DIVIDER “0” Ratio Select</td><td>EEPROM</td></tr>
<tr><td>14</td><td>OUT0DIVRSEL1</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>15</td><td>OUT0DIVRSEL2</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>16</td><td>OUT0DIVRSEL3</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>17</td><td>OUT0DIVRSEL4</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>18</td><td>OUT0DIVRSEL5</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>19</td><td>OUT0DIVRSEL6</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>20</td><td>OUT0DIVSEL</td><td>Output 0</td><td>When set to “0”, the divider is disabled
When set to “1”, the divider is enabled</td><td>EEPROM</td></tr>
<tr><td>21</td><td>HiSWINGLVPECL0</td><td>Output 0</td><td>High Swing LVPECL When set to “1” and Normal Swing when set to “0”
– If LVCMOS or LVDS is selected the Output swing will stay at the same level.(1)
– If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to “1” and Normal LVPECL if it is set to “0”.</td><td>EEPROM</td></tr>
<tr><td>22</td><td>CMOSMODE0PX</td><td>Output 0</td><td rowspan="2">LVCMOS mode select for OUTPUT “0” Positive Pin.
(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State</td><td>EEPROM</td></tr>
<tr><td>23</td><td>CMOSMODE0PY</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>24</td><td>CMOSMODE0NX</td><td>Output 0</td><td rowspan="2">LVCMOS mode select for OUTPUT “0” Negative Pin.
(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State</td><td>EEPROM</td></tr>
<tr><td>25</td><td>CMOSMODE0NY</td><td>Output 0</td><td>EEPROM</td></tr>
<tr><td>26</td><td>OUTBUFSEL0X</td><td>Output 0</td><td rowspan="2"><table>
<tr><th>OUTPUT TYPE</th><th colspan="6">RAM BITS</th></tr>
<tr><th></th><th>22</th><th>23</th><th>24</th><th>25</th><th>26</th><th>27</th></tr>
<tr><td>LVPECL</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>LVDS</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>LVCMOS</td><td colspan="4">See Settings Above*</td><td>0</td><td>0</td></tr>
<tr><td>Output Disabled</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table>
* Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs</td><td>EEPROM</td></tr>
<tr><td>27</td><td>OUTBUFSEL0Y</td><td>Output 0</td><td>EEPROM</td></tr>
</table>

(1) Set Register R0.21 to '0' for LVDS and LVCMOS outputs

Device Registers: Register 1 Address 0x01

Table 6. CDCE18005 Register 1 Bit Definitions

<table>
<tr><th>RAM BIT</th><th>BIT NAME</th><th>RELATED BLOCK</th><th>DESCRIPTION/FUNCTION</th><th></th></tr>
<tr><td>0</td><td>RESERVED</td><td rowspan="4"></td><td rowspan="4">Always St "0" for Proper Operation</td><td>EEPROM</td></tr>
<tr><td>1</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>2</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>3</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>4</td><td>OUTMUX1SELX</td><td>Output 1</td><td rowspan="2">OUTPUT MUX “1” Select. Selects the Signal driving Output Divider ”1”
(X,Y) = 00: PRI_REF, 01:SEC_REF, 10:AUX_IN, 11:Reserved</td><td>EEPROM</td></tr>
<tr><td>5</td><td>OUTMUX1SELY</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>6</td><td>PH1ADJC0</td><td>Output 1</td><td rowspan="7">Coarse phase adjust select for output divider “1”</td><td>EEPROM</td></tr>
<tr><td>7</td><td>PH1ADJC1</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>8</td><td>PH1ADJC2</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>9</td><td>PH1ADJC3</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>10</td><td>PH1ADJC4</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>11</td><td>PH1ADJC5</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>12</td><td>PH1ADJC6</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>13</td><td>OUT1DIVRSEL0</td><td>Output 1</td><td rowspan="7">OUTPUT DIVIDER “1” Ratio Select</td><td>EEPROM</td></tr>
<tr><td>14</td><td>OUT1DIVRSEL1</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>15</td><td>OUT1DIVRSEL2</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>16</td><td>OUT1DIVRSEL3</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>17</td><td>OUT1DIVRSEL4</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>18</td><td>OUT1DIVRSEL5</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>19</td><td>OUT1DIVRSEL6</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>20</td><td>OUT1DIVSEL</td><td>Output 1</td><td>When set to “0”, the divider is disabled
When set to “1”, the divider is enabled</td><td>EEPROM</td></tr>
<tr><td>21</td><td>HiSWINGLVPECL1</td><td>Output 1</td><td>High Swing LVPECL When set to “1” and Normal Swing when set to “0”
– If LVCMOS or LVDS is selected the Output swing will stay at the same level.(1)
– If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to “1” and Normal LVPECL if it is set to “0”.</td><td>EEPROM</td></tr>
<tr><td>22</td><td>CMOSMODE1PX</td><td>Output 1</td><td rowspan="2">LVCMOS mode select for OUTPUT “1” Positive Pin.
(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State</td><td>EEPROM</td></tr>
<tr><td>23</td><td>CMOSMODE1PY</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>24</td><td>CMOSMODE1NX</td><td>Output 1</td><td rowspan="2">LVCMOS mode select for OUTPUT “1” Negative Pin.
(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State</td><td>EEPROM</td></tr>
<tr><td>25</td><td>CMOSMODE1NY</td><td>Output 1</td><td>EEPROM</td></tr>
<tr><td>26</td><td>OUTBUFSEL1X</td><td>Output 1</td><td rowspan="2"><table>
<tr><th>OUTPUT TYPE</th><th colspan="6">RAM BITS</th></tr>
<tr><th></th><th>22</th><th>23</th><th>24</th><th>25</th><th>26</th><th>27</th></tr>
<tr><td>LVPECL</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>LVDS</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>LVCMOS</td><td colspan="3">See Settings Above*</td><td></td><td>0</td><td>0</td></tr>
<tr><td>Output Disabled</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table>
* Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs</td><td>EEPROM</td></tr>
<tr><td>27</td><td>OUTBUFSEL1Y</td><td>Output 1</td><td>EEPROM</td></tr>
</table>

(1) Set Register R1.21 to '0' for LVDS and LVCMOS outputs

Device Registers: Register 2 Address 0x02

Table 7. CDCE18005 Register 2 Bit Definitions

<table>
<tr><th>RAM BIT</th><th>BIT NAME</th><th>RELATED BLOCK</th><th>DESCRIPTION/FUNCTION</th><th></th></tr>
<tr><td>0</td><td>RESERVED</td><td rowspan="4"></td><td rowspan="4">Always Set to "0" for Proper Operation</td><td>EEPROM</td></tr>
<tr><td>1</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>2</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>3</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>4</td><td>OUTMUX2SELX</td><td>Output 2</td><td rowspan="2">OUTPUT MUX “2” Select. Selects the Signal driving Output Divider ”2”
(X,Y) = 00: PRI_REF, 01:SEC_REF, 10:AUX_IN, 11:Reserved</td><td>EEPROM</td></tr>
<tr><td>5</td><td>OUTMUX2SELY</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>6</td><td>PH2ADJC0</td><td>Output 2</td><td rowspan="7">Coarse phase adjust select for output divider “2”</td><td>EEPROM</td></tr>
<tr><td>7</td><td>PH2ADJC1</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>8</td><td>PH2ADJC2</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>9</td><td>PH2ADJC3</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>10</td><td>PH2ADJC4</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>11</td><td>PH2ADJC5</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>12</td><td>PH2ADJC6</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>13</td><td>OUT2DIVRSEL0</td><td>Output 2</td><td rowspan="7">OUTPUT DIVIDER “2” Ratio Select</td><td>EEPROM</td></tr>
<tr><td>14</td><td>OUT2DIVRSEL1</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>15</td><td>OUT2DIVRSEL2</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>16</td><td>OUT2DIVRSEL3</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>17</td><td>OUT2DIVRSEL4</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>18</td><td>OUT2DIVRSEL5</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>19</td><td>OUT2DIVRSEL6</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>20</td><td>OUT2DIVSEL</td><td>Output 2</td><td>When set to “0”, the divider is disabled
When set to “1”, the divider is enabled</td><td>EEPROM</td></tr>
<tr><td>21</td><td>HiSWINGLVPEC2</td><td>Output 2</td><td>High Swing LVPECL When set to “1” and Normal Swing when set to “0”
– If LVCMOS or LVDS is selected the Output swing will stay at the same level.(1)
– If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to “1” and Normal LVPECL if it is set to “0”.</td><td>EEPROM</td></tr>
<tr><td>22</td><td>CMOSMODE2PX</td><td>Output 2</td><td rowspan="2">LVCMOS mode select for OUTPUT “2” Positive Pin.
(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State</td><td>EEPROM</td></tr>
<tr><td>23</td><td>CMOSMODE2PY</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>24</td><td>CMOSMODE2NX</td><td>Output 2</td><td rowspan="2">LVCMOS mode select for OUTPUT “2” Negative Pin.
(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State</td><td>EEPROM</td></tr>
<tr><td>25</td><td>CMOSMODE2NY</td><td>Output 2</td><td>EEPROM</td></tr>
<tr><td>26</td><td>OUTBUFSEL2X</td><td>Output 2</td><td rowspan="2"><table>
<tr><th>OUTPUT TYPE</th><th colspan="6">RAM BITS</th></tr>
<tr><th></th><th>22</th><th>23</th><th>24</th><th>25</th><th>26</th><th>27</th></tr>
<tr><td>LVPECL</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>LVDS</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>LVCMOS</td><td colspan="4">See Settings Above*</td><td>0</td><td>0</td></tr>
<tr><td>Output Disabled</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table>
* Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs</td><td>EEPROM</td></tr>
<tr><td>27</td><td>OUTBUFSEL2Y</td><td>Output 2</td><td>EEPROM</td></tr>
</table>

(1) Set Register R2.21 to '0' for LVDS and LVCMOS outputs

Device Registers: Register 3 Address 0x03

Table 8. CDCE18005 Register 3 Bit Definitions

<table>
<tr><th>RAM BIT</th><th>BIT NAME</th><th>RELATED BLOCK</th><th>DESCRIPTION/FUNCTION</th><th></th></tr>
<tr><td>0</td><td>RESERVED</td><td rowspan="4"></td><td rowspan="4">Always Set to "0" for Proper Operation</td><td>EEPROM</td></tr>
<tr><td>1</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>2</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>3</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>4</td><td>OUTMUX3SELX</td><td>Output 3</td><td rowspan="2">OUTPUT MUX “3” Select. Selects the Signal driving Output Divider ”3”
(X,Y) = 00: PRI_REF, 01:SEC_REF, 10:AUX_IN, 11:Reserved</td><td>EEPROM</td></tr>
<tr><td>5</td><td>OUTMUX3SELY</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>6</td><td>PH3ADJC0</td><td>Output 3</td><td rowspan="7">Coarse phase adjust select for output divider “3”</td><td>EEPROM</td></tr>
<tr><td>7</td><td>PH3ADJC1</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>8</td><td>PH3ADJC2</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>9</td><td>PH3ADJC3</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>10</td><td>PH3ADJC4</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>11</td><td>PH3ADJC5</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>12</td><td>PH3ADJC6</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>13</td><td>OUT3DIVRSEL0</td><td>Output 3</td><td rowspan="7">OUTPUT DIVIDER “3” Ratio Select</td><td>EEPROM</td></tr>
<tr><td>14</td><td>OUT3DIVRSEL1</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>15</td><td>OUT3DIVRSEL2</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>16</td><td>OUT3DIVRSEL3</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>17</td><td>OUT3DIVRSEL4</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>18</td><td>OUT3DIVRSEL5</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>19</td><td>OUT3DIVRSEL6</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>20</td><td>OUT3DIVSEL</td><td>Output 3</td><td>When set to “0”, the divider is disabled
When set to “1”, the divider is enabled</td><td>EEPROM</td></tr>
<tr><td>21</td><td>HiSWINGLVPEC3</td><td>Output 3</td><td>High Swing LVPECL When set to “1” and Normal Swing when set to “0”
– If LVCMOS or LVDS is selected the Output swing will stay at the same level.(1)
– If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to “1” and Normal LVPECL if it is set to “0”.</td><td>EEPROM</td></tr>
<tr><td>22</td><td>CMOSMODE3PX</td><td>Output 3</td><td rowspan="2">LVCMOS mode select for OUTPUT “3” Positive Pin.
(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State</td><td>EEPROM</td></tr>
<tr><td>23</td><td>CMOSMODE3PY</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>24</td><td>CMOSMODE3NX</td><td>Output 3</td><td rowspan="2">LVCMOS mode select for OUTPUT “3” Negative Pin.
(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State</td><td>EEPROM</td></tr>
<tr><td>25</td><td>CMOSMODE3NY</td><td>Output 3</td><td>EEPROM</td></tr>
<tr><td>26</td><td>OUTBUFSEL3X</td><td>Output 3</td><td rowspan="2">
<table>
<tr><th rowspan="2">OUTPUT TYPE</th><th colspan="6">RAM BITS</th></tr>
<tr><th>22</th><th>23</th><th>24</th><th>25</th><th>26</th><th>27</th></tr>
<tr><td>LVPECL</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>LVDS</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>LVCMOS</td><td colspan="4">See Settings Above*</td><td>0</td><td>0</td></tr>
<tr><td>Output Disabled</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table>
* Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs
</td><td>EEPROM</td></tr>
<tr><td>27</td><td>OUTBUFSEL3Y</td><td>Output 3</td><td>EEPROM</td></tr>
</table>

(1) Set Register R3.21 to '0' for LVDS and LVCMOS outputs

Device Registers: Register 4 Address 0x04

Table 9. CDCE18005 Register 4 Bit Definitions

<table>
<tr><th>RAM BIT</th><th>BIT NAME</th><th>RELATED BLOCK</th><th>DESCRIPTION/FUNCTION</th><th></th></tr>
<tr><td>0</td><td>RESERVED</td><td rowspan="4"></td><td rowspan="4">Must be set to "0" for proper operation</td><td>EEPROM</td></tr>
<tr><td>1</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>2</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>3</td><td>RESERVED</td><td>EEPROM</td></tr>
<tr><td>4</td><td>OUTMUX4SELX</td><td>Output 4</td><td rowspan="2">OUTPUT MUX “4” Select. Selects the Signal driving Output Divider ”4”
(X,Y) = 00: PRI_REF, 01:SEC_REF, 10:SMART_AUX_IN, 11:Reserved</td><td>EEPROM</td></tr>
<tr><td>5</td><td>OUTMUX4SELY</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>6</td><td>PH4ADJC0</td><td>Output 4</td><td rowspan="7">Coarse phase adjust select for output divider “4”</td><td>EEPROM</td></tr>
<tr><td>7</td><td>PH4ADJC1</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>8</td><td>PH4ADJC2</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>9</td><td>PH4ADJC3</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>10</td><td>PH4ADJC4</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>11</td><td>PH4ADJC5</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>12</td><td>PH4ADJC6</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>13</td><td>OUT4DIVRSEL0</td><td>Output 4</td><td rowspan="7">OUTPUT DIVIDER “4” Ratio Select</td><td>EEPROM</td></tr>
<tr><td>14</td><td>OUT4DIVRSEL1</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>15</td><td>OUT4DIVRSEL2</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>16</td><td>OUT4DIVRSEL3</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>17</td><td>OUT4DIVRSEL4</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>18</td><td>OUT4DIVRSEL5</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>19</td><td>OUT4DIVRSEL6</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>20</td><td>OUT4DIVSEL</td><td>Output 4</td><td>When set to “0”, the divider is disabled
When set to “1”, the divider is enabled</td><td>EEPROM</td></tr>
<tr><td>21</td><td>HiSWINGLVPEC4</td><td>Output 4</td><td>High Swing LVPECL When set to “1” and Normal Swing when set to “0”(1)
– If LVCMOS or LVDS is selected the Output swing will stay at the same level.
– If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to “1” and Normal LVPECL if it is set to “0”.</td><td>EEPROM</td></tr>
<tr><td>22</td><td>CMOSMODE4PX</td><td>Output 4</td><td rowspan="2">LVCMOS mode select for OUTPUT “4” Positive Pin.
(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State</td><td>EEPROM</td></tr>
<tr><td>23</td><td>CMOSMODE4PY</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>24</td><td>CMOSMODE4NX</td><td>Output 4</td><td rowspan="2">LVCMOS mode select for OUTPUT “3” Negative Pin.
(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State</td><td>EEPROM</td></tr>
<tr><td>25</td><td>CMOSMODE4NY</td><td>Output 4</td><td>EEPROM</td></tr>
<tr><td>26</td><td>OUTBUFSEL4X</td><td>Output 4</td><td rowspan="2">
<table>
<tr><th>OUTPUT TYPE</th><th colspan="6">RAM BITS</th></tr>
<tr><th></th><th>22</th><th>23</th><th>24</th><th>25</th><th>26</th><th>27</th></tr>
<tr><td>LVPECL</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>LVDS</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>LVCMOS</td><td colspan="4">See Settings Above*</td><td>0</td><td>0</td></tr>
<tr><td>Output Disabled</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table>
* Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs
</td><td>EEPROM</td></tr>
<tr><td>27</td><td>OUTBUFSEL4Y</td><td>Output 4</td><td>EEPROM</td></tr>
</table>

(1) Set Register R4.21 to '0' for LVDS and LVCMOS outputs

Device Registers: Register 5 Address 0x05

Table 10. CDCE18005 Register 5 Bit Definitions

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	
0	INBUFSELX	INBUFSELX	Input Buffer Select (LVPECL,LVDS or LVCMOS) XY(01) LVPECL, (11) LVDS, (00) LVCMOS- Input is Positive Pin	EEPROM
1	INBUFSELY	INBUFSELY		EEPROM
2	SYNCSEL1	Output Divider Synchronization	SYNCSEL(1,2)= 10 :Output divider sync to Primary input SYNCSEL(1,2)= 01 :Output divider sync to Secondary input SYNCSEL(1,2)= 00 :Output divider sync to Auxiliary input	EEPROM
3	SYNCSEL2			EEPROM
4	RESERVED		Always Set to **"1"** for Proper Operation	EEPROM
5	RESERVED		Always Set to **"0"** for Proper Operation	EEPROM
6	ACDCSEL	Input Buffers	If Set to “1” DC Termination, If set to “0” AC Termination	EEPROM
7	HYSTEN	Input Buffers	If Set to “1” Input Buffers Hysteresis Enabled. It is not recommended that Hysteresis be disabled.	EEPROM
8	PRI_TERMSEL	Input Buffers	If Set to “0” Primary Input Buffer Internal Termination Enabled If set to “1” Primary Internal Termination circuitry Disabled	EEPROM
9	PRIINVBB	Input Buffers	If Set to “1” Primary Input Negative Pin Biased with Internal VBB Voltage.	EEPROM
10	SECINVBB	Input Buffers	If Set to “1” Secondary Input Negative Pin Biased with Internal VBB Voltage	EEPROM
11	FAILSAFE	Input Buffers	If Set to “1” Fail Safe is Enabled for all Input Buffers configured as LVDS, DC Coupling only.	EEPROM
12	RESERVED	- - - -	Must be set to "0" for proper operation	EEPROM
13	RESERVED			EEPROM
14	RESERVED			EEPROM
15	RESERVED			EEPROM
16	RESERVED			EEPROM
17	RESERVED			EEPROM
18	RESERVED			EEPROM
19	RESERVED			EEPROM
20	RESERVED			EEPROM
21	RESERVED			EEPROM
22	RESERVED			EEPROM
23	RESERVED			EEPROM
24	RESERVED			EEPROM
25	RESERVED			EEPROM
26	RESERVED			EEPROM
27	RESERVED			EEPROM

Device Registers: Register 6 Address 0x06

Table 11. CDCE18005 Register 6 Bit Definitions

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	
0	RESERVED			EEPROM
1	RESERVED			EEPROM
2	RESERVED			EEPROM
3	RESERVED			EEPROM
4	RESERVED			EEPROM
5	RESERVED		Must be set to "0"	EEPROM
6	RESERVED			EEPROM
7	RESERVED			EEPROM
8	RESERVED			EEPROM
9	RESERVED			EEPROM
10	RESERVED			EEPROM
11	RESERVED			EEPROM
12	SEC_TERMSEL	Input Buffers	If Set to “0” Secondary Input Buffer Internal Termination Enabled If set to “1” Secondary Internal Termination circuitry Disabled	EEPROM
13	RESERVED			EEPROM
14	RESERVED			EEPROM
15	RESERVED			EEPROM
16	RESERVED			EEPROM
17	RESERVED			EEPROM
18	RESERVED		Must be set to "0"	EEPROM
19	RESERVED			EEPROM
20	RESERVED			EEPROM
21	RESERVED			EEPROM
22	RESERVED			EEPROM
23	RESERVED			EEPROM
24	AUXOUTEN	Output AUX	Enable Auxiliary Output when set to “1”	EEPROM
25	AUXFEEDSEL	Output AUX	Select the Output that will driving the AUX Output; Low for Selecting Output Divider “2” and High for Selecting Output Divider “3”	EEPROM
26	RESERVED		Must be set to "0"	EEPROM
27	RESERVED		Must be set to "0"	EEPROM

Device Registers: Register 7 Address 0x07

Table 12. CDCE18005 Register 7 Bit Definitions

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	
0	RESERVED			EEPROM
1	RESERVED			EEPROM
2	RESERVED			EEPROM
3	RESERVED			EEPROM
4	RESERVED			EEPROM
5	RESERVED			EEPROM
6	RESERVED			EEPROM
7	RESERVED			EEPROM
8	RESERVED			EEPROM
9	RESERVED			EEPROM
10	RESERVED			EEPROM
11	RESERVED		Always Set to "0" for Proper Operation	EEPROM
12	RESERVED			EEPROM
13	RESERVED			EEPROM
14	RESERVED			EEPROM
15	RESERVED			EEPROM
16	RESERVED			EEPROM
17	RESERVED			EEPROM
18	RESERVED			EEPROM
19	RESERVED			EEPROM
20	RESERVED			EEPROM
21	RESERVED			EEPROM
22	TESTMUX1	Diagnostics	Set to “1”	EEPROM
23	RESERVED		Always Set to "0" for Proper Operation	EEPROM
24	TEXTMUX2	Diagnostics	Set to “1”	EEPROM
25	RESERVED		Always Set to "0" for Proper Operation	EEPROM
26	EPUNLOCK	Status	If it reads "0" the EEPROM is unlocked. If it reads "1" the EEPROM is Locked	RAM
27	EPSTATUS	Status	Read only; always reads "1"	RAM

Device Registers: Register 8 Address 0x08

Table 13. CDCE18005 Register 8 Bit Definitions(1)

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	
0	RESERVED			RAM
1	RESERVED			RAM
2	RESERVED			RAM
3	RESERVED		*TI Test Registers. For TI Use Only*	RAM
4	RESERVED			RAM
5	RESERVED			RAM
6	RESERVED			RAM
7	$\overline{\text{SLEEP}}$	Status	Set Device Sleep mode On when set to “0”, Normal Mode when set to “1”	RAM
8	$\overline{\text{SYNC}}$	Status	If set to “0” this bit forces “$\overline{\text{SYNC}}$; Set to “1” to exit the Synchronization State.	RAM
9	RESERVED		Must be set to "0"	RAM
10	VERSION0		Silicon Revision	RAM
11	VERSION1		Silicon Revision	RAM
12	VERSION2		Silicon Revision	RAM
13	RESERVED			RAM
14	RESERVED			RAM
15	RESERVED			RAM
16	RESERVED			RAM
17	RESERVED			RAM
18	RESERVED			RAM
19	RESERVED			RAM
20	RESERVED		*TI Test Registers. For TI Use Only*	RAM
21	RESERVED			RAM
22	RESERVED			RAM
23	RESERVED			RAM
24	RESERVED			RAM
25	RESERVED			RAM
26	RESERVED			RAM
27	RESERVED			RAM

(1) All reserved Bits can be set to "0" when writing to Register 8

Device Control

Figure 20 provides a conceptual explanation of the CDCE18005 Device operation. Table 14 defines how the device behaves in each of the operational states.

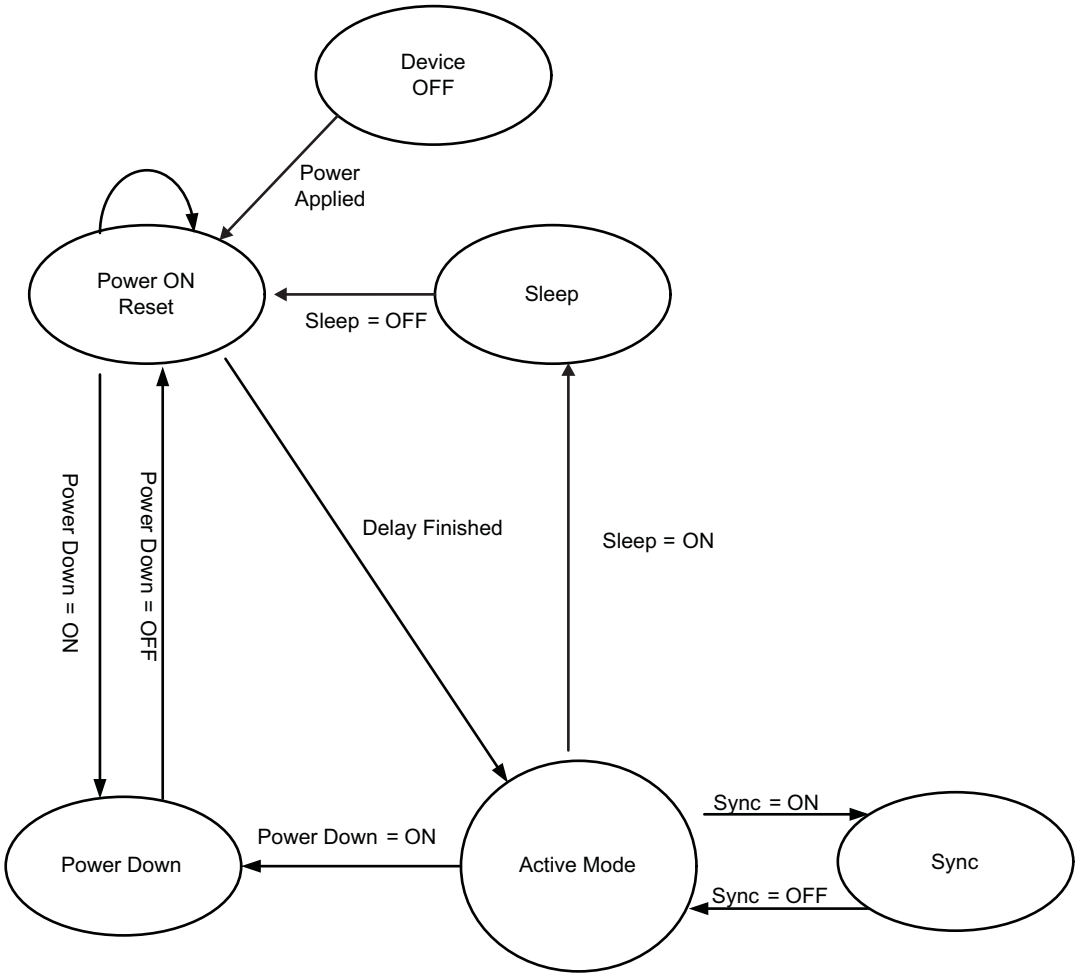


Figure 20. CDCE18005 Device State Control Diagram

Table 14. CDCE18005 Device State Definitions

State	Device Behavior	Entered Via	Exited Via	Status		
				SPI Port	Output Divider	Output Buffer
Power-On Reset	After device power supply reaches approximately 2.35V, the contents of EEPROM are copied into the Device Registers within 100 ns, thereby initializing the device hardware.	Power applied to the device or upon exit from Power Down State via the Power_Down pin set HIGH.	Power On Reset and EEPROM loading delays are finished OR the Power_Down pin is set LOW.	OFF	Disabled	OFF
Active Mode	Normal Operation	Sync = OFF (from Sync State).	Sync, Power Down, Sleep, or Manual Recalibration activated.	ON	Disabled or Enabled	HI-Z or Enabled
Power Down	Used to shut down all hardware and Resets the device after exiting the Power Down State. Therefore, the EEPROM contents will eventually be copied into RAM after the Power Down State is exited.	$\overline{\text{Power\_Down}}$ pin is pulled LOW.	$\overline{\text{Power\_Down}}$ pin is pulled HIGH.	ON	Disabled	HI-Z
Sleep	Identical to the Power Down State except the EEPROM contents are not copied into RAM.	$\overline{\text{SLEEP}}$ bit in device register 8 bit 7 is set LOW.	$\overline{\text{SLEEP}}$ bit in device register 8 bit 7 is set HIGH.	ON	Disabled	HI-Z

Table 14. CDCE18005 Device State Definitions (continued)

State	Device Behavior	Entered Via	Exited Via	Status		
				SPI Port	Output Divider	Output Buffer
Sync	Sync synchronizes all output dividers so that they begin counting at the same time. Note: this operation is performed automatically each time a divider register is accessed.	$\overline{\text{SYNC}}$ Bit in device register 8 bit 8 is set LOW or $\overline{\text{SYNC}}$ pin is pulled LOW	$\overline{\text{SYNC}}$ Bit in device register 8 bit 8 is set HIGH or $\overline{\text{SYNC}}$ pin is pulled HIGH	ON	Disabled	HI-Z

External Control Pins

$\overline{\text{Power\_Down}}$

The Power_Down pin places the CDCE18005 into the power down state. Additionally, the CDCE18005 loads the contents of the EEPROM into RAM after the Power_Down pin is de-asserted; therefore, it is used to initialize the device after power is applied. SPI_LE signal has to be HIGH in order for EEPROM to load correctly during the rising edge of Power_Down.

$\overline{\text{SYNC}}$

The $\overline{\text{SYNC}}$ pin (Active LOW) has a complementary register location located in Device Register 8 bit 8. When $\overline{\text{SYNC}}$ enabled, Sync synchronizes all output dividers so that they begin counting simultaneously. Further, $\overline{\text{SYNC}}$ disables all outputs when in the active State.

INPUT BLOCK

The Input Block includes two Universal Input Buffers, an Auxiliary Input. The Input Block drives three different clock signals onto the Internal Clock Distribution Bus.

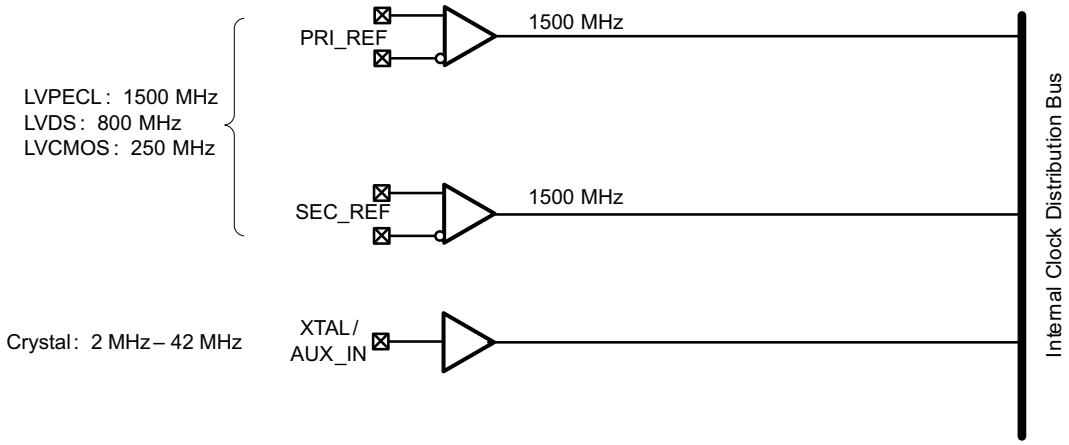
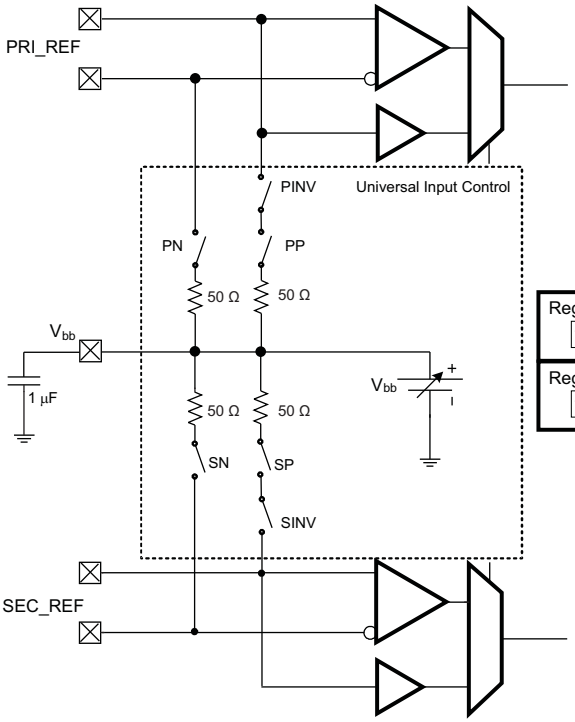


Figure 21. CDCE18005 Input Block With References to Registers

Universal Input Buffers (UIB)

Figure 22 shows the key elements of a universal input buffer. A UIB supports multiple formats along with different termination and coupling schemes. The CDCE18005 implements the UIB by including on board switched termination, a programmable bias voltage generator, and an output multiplexer. The CDCE18005 provides a high degree of configurability on the UIB to facilitate most existing clock input formats.



Settings			Nominal Vbb
5.1 INBUFSELY	5.0 INBUFSELX	5.6 ACDCSEL	
1	0	0	1.9V
1	0	1	1.2V
1	1	0	1.2V
1	1	1	1.2V

Register 6

12

Register 5

10	9	8	7	6	1	0

Settings				SWITCH Status		
5.0 INBUFSELX	5.1 INBUFSELY	5.8, 6.12 TERMSEL	5.9,5.10 INVBB	P	N	INV
0	0	X	X	OFF	OFF	OFF
X	X	1	X	OFF	OFF	OFF
X	1	0	0	ON	ON	ON
X	1	0	1	ON	ON	OFF

Figure 22. CDCE18005 Universal Input Buffer

Table 15 lists several settings for many possible clock input scenarios. Note that the two universal input buffers share the Vbb generator. Therefore, if both inputs use internal termination, they must use the same configuration mode (LVDS, LVPECL, or LVCMOS). If the application requires different modes (e.g. LVDS and LVPECL) then one of the two inputs must implement external termination.

Table 15. CDCE18005 Universal Input Buffer Configuration Matrix

PRI_REF CONFIGURATION MATRIX											
	SETTINGS						CONFIGURATION				
Register.Bit →	5.7	5.1	5.0	5.8	5.9	5.6					
Bit Name →	HYSTEN	INBUFSELY	INBUFSELX	PRI_TERMSEL	PRIINVBB	ACDCSEL	Hysteresis	Mode	Coupling	Termination	Vbb
	1	0	0	X	X	X	ENABLED	LVCMOS	DC	N/A	—
	1	1	0	0	0	0	ENABLED	LVPECL	AC	Internal	1.9V
	1	1	0	0	0	1	ENABLED	LVPECL	DC	Internal	1.2V
	1	1	0	1	X	X	ENABLED	LVPECL	—	External	—
	1	1	1	0	0	0	ENABLED	LVDS	AC	Internal	1.2V
	1	1	1	0	0	1	ENABLED	LVDS	DC	Internal	1.2V
	1	1	1	1	X	X	ENABLED	LVDS	—	External	—
	0	X	X	X	X	X	OFF	—	—	—	—
	1	X	X	X	X	X	ENABLED	—	—	—	—

Table 15. CDCE18005 Universal Input Buffer Configuration Matrix (continued)

PRI_REF CONFIGURATION MATRIX											
	SETTINGS						CONFIGURATION				
Register.Bit →	5.7	5.1	5.0	5.8	5.9	5.6					
Bit Name →	HYSTEN	INBUFSELY	INBUFSELX	PRI_TERMSEL	PRIINVBB	ACDCSEL	Hysteresis	Mode	Coupling	Termination	Vbb
SEC_REF CONFIGURATION MATRIX											
	SETTINGS						CONFIGURATION				
Register.Bit →	5.7	5.1	5.0	6.12	5.10	5.6					
Bit Name →	HYSTEN	INBUFSELY	INBUFSELX	SEC_TERMSEL	SECINVBB	ACDCSEL	Hysteresis	Mode	Coupling	Termination	Vbb
	1	0	0	X	X	X	ENABLED	LVCMOS	DC	N/A	—
	1	1	0	0	0	0	ENABLED	LVPECL	AC	Internal	1.9V
	1	1	0	0	0	1	ENABLED	LVPECL	DC	Internal	1.2V
	1	1	0	1	X	X	ENABLED	LVPECL	—	External	—
	1	1	1	0	0	0	ENABLED	LVDS	AC	Internal	1.2V
	1	1	1	0	0	1	ENABLED	LVDS	DC	Internal	1.2V
	1	1	1	1	X	X	ENABLED	LVDS	—	External	—
	0	X	X	X	X	X	OFF	—	—	—	—
	1	X	X	X	X	X	ENABLED	—	—	—	—

LVDS Fail Safe Mode

Differential data line receivers can switch on noise in the absence of an input signal. This occurs when the clock driver is turned off or the interconnect is damaged or missing. Traditionally the solution to this problem involves incorporating an external resistor network on the receiver input. This network applies a steady-state bias voltage to the input pins. The additional cost of the external components notwithstanding, the use of such a network lowers input signal magnitude and thus reduces the differential noise margin. The CDCE18005 provides internal failsafe circuitry on all LVDS inputs if enabled as shown in Table 16 for DC termination only.

Table 16. LVDS Failsafe Settings

Bit Name → Register.Bit →	FAILSAFE 5.11	LVDS Failsafe
	0	Disabled for all inputs
	1	Enabled for all inputs

OUTPUT BLOCK

The output block includes five identical output channels. Each output channel comprises an output multiplexer, a clock divider module, and a universal output buffer as shown in Figure 23.

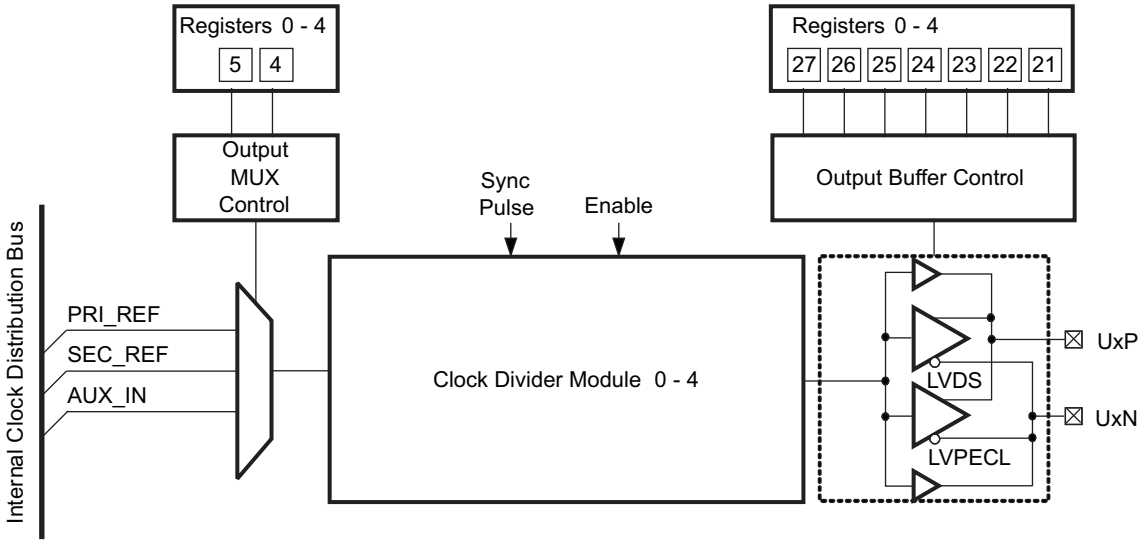


Figure 23. CDCE18005 Output Channel

Output Multiplexer Control

The output multiplexer selects which of the four clock sources available on the Internal Clock Distribution Bus will be presented to the Clock Divider Module. For a description of these clock sources, see Figure 21.

Table 17. CDCE18005 Output Multiplexer Control Settings

OUTPUT MULTIPLEXER CONTROL		
Register n (n = 0,1,2,3,4)		
OUTMUXnSELX n.4	OUTMUXnSELY n.5	CLOCK SOURCE SELECTED
0	0	PRI_REF
0	1	SEC_REF
1	0	AUX_IN
1	1	Reserved

Output Buffer Control

Each of the five output channels includes a programmable output buffer; supporting LVPECL, LVDS, and LVCMOS modes. Table 18 lists the settings required to configure the CDCE18005 for each output type. Registers 0 through 4 correspond to Output Channels 0 through 4 respectively.

Table 18. CDCE18005 Output Buffer Control Settings

OUTPUT BUFFER CONTROL						OUTPUT TYPE
Register n (n = 0,1,2,3,4)						
CMOSMODEnPX	CMOSMODEnPY	CMOSMODEnNX	CMOSMODEnNY	OUTBUFSELnX	OUTBUFSELnY	
n.22	n.23	n.24	n.25	n.26	n.27	
0	0	0	0	0	1	LVPECL
0	1	0	1	1	1	LVDS
See LVCMOS Output Buffer Configuration Settings				0	0	LVCMOS
0	1	0	1	1	0	HI-Z

Output Buffer Control – LVCMOS Configurations

A LVCMOS output configuration requires additional configuration data. In the single ended configuration, each Output Channel provides a pair of outputs. The CDCE18005 supports four modes of operation for single ended outputs as listed in Table 19.

Table 19. LVCMOS Output Buffer Configuration Settings

OUTPUT BUFFER CONTROL – LVCMOS CONFIGURATION						Output Type	Pin	Output Mode
Register n (n = 0,1,2,3,4)								
CMOSMODEnPX	CMOSMODEnPY	CMOSMODEnNX	CMOSMODEnNY	OUTBUFSELnX	OUTBUFSELnY			
n.22	n.23	n.24	n.25	n.26	n.27			
X	X	0	0	0	0	LVCMOS	Negative	Active – Non-inverted
X	X	0	1	0	0	LVCMOS	Negative	Hi-Z
X	X	1	0	0	0	LVCMOS	Negative	Active – Non-inverted
X	X	1	1	0	0	LVCMOS	Negative	Low
0	0	X	X	0	0	LVCMOS	Positive	Active – Non-inverted
0	1	X	X	0	0	LVCMOS	Positive	Hi-Z
1	0	X	X	0	0	LVCMOS	Positive	Active – Non-inverted
1	1	X	X	0	0	LVCMOS	Positive	Low

Output Dividers

Figure 24 shows that each output channel provides a 7-bit divider and digital phase adjust block. Table 20 lists the divide ratios supported by the output divider for each output channel. The output divider's maximum input frequency is limited to 1.175GHz. If the divider is bypassed (divide ratio = 1) then the maximum frequency of the output channel is 1.5GHz.

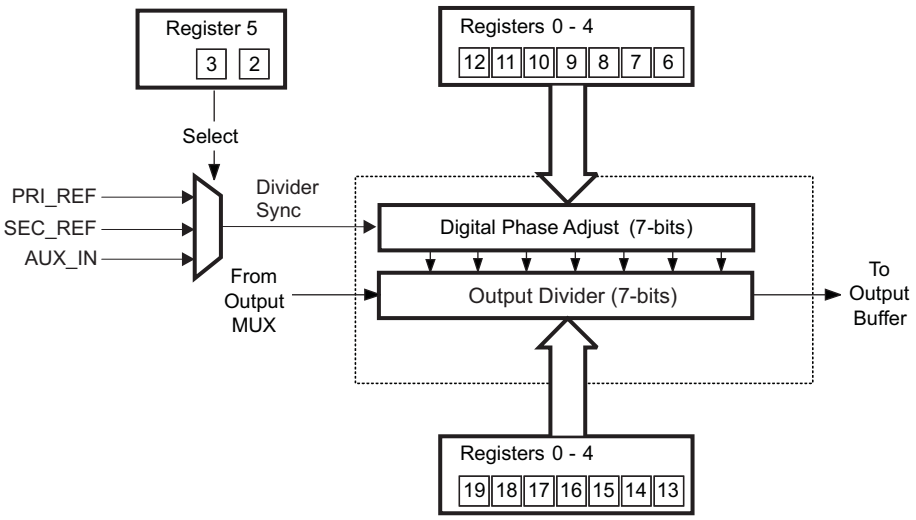


Figure 24. CDCE18005 Output Divider and Phase Adjust

Table 20. CDCE18005 Output Divider Settings

OUTPUT DIVIDER n SETTINGS Register n (n = 0,1,2,3,4)										Output Divide Ratio	
Multiplexer		Integer Divider			Prescaler			Prescaler Setting	Integer Divider Setting	Output Channels 0–4	Auxiliary Output
OUTnDIVSEL6	OUTnDIVSEL5	OUTnDIVSEL4	OUTnDIVSEL3	OUTnDIVSEL2	OUTnDIVSEL1	OutnDIVSEL0	OUTnDIVSEL				
n.19	n.18	n.17	n.16	n.15	n.14	n.13	n.20				
X	X	X	X	X	X	X	0			OFF	OFF
0	1	0	0	0	0	0	1	–	–	1	OFF
1	0	0	0	0	0	0	1	2	–	2**	4
1	0	0	0	0	0	1	1	3	–	3**	6
1	0	0	0	0	1	0	1	4	–	4	8
1	0	0	0	0	1	1	1	5	–	5	10
0	0	0	0	0	0	1	1	3	2	6	6
0	0	0	0	0	1	0	1	4	2	8	8
0	0	0	0	0	1	1	1	5	2	10	10
0	0	0	0	1	0	1	1	3	4	12	12
0	0	0	0	1	1	0	1	4	4	16	16
0	0	0	0	1	1	1	1	5	4	20	20
0	0	0	1	0	0	1	1	3	6	18	18
0	0	0	1	0	1	0	1	4	6	24	24
0	0	0	1	0	1	1	1	5	6	30	30
0	0	0	1	1	1	0	1	4	8	32	32
0	0	0	1	1	1	1	1	5	8	40	40
0	0	1	0	0	1	1	1	5	10	50	50
0	0	1	0	1	0	1	1	3	12	36	36
0	0	1	0	1	1	0	1	4	12	48	48
0	0	1	0	1	1	1	1	5	12	60	60
0	0	1	1	0	0	0	1	2	14	28	28
0	0	1	1	0	0	1	1	3	14	42	42
0	0	1	1	0	1	0	1	4	14	56	56
0	0	1	1	0	1	1	1	5	14	70	70
0	0	1	1	1	1	0	1	4	16	64	64
0	0	1	1	1	1	1	1	5	16	80	80

**Output channel 2 or 3 determine the auxiliary output divide ratio. For example, if the auxiliary output is programmed to drive via output 2 and output 2 divider is programmed to divide by 3, then the divide ratio for the auxiliary output will be 6.

Digital Phase Adjust

Figure 25 provides an overview of the Digital Phase Adjust feature. The output divider includes a coarse phase adjust that shifts the divided clock signal that drives the output buffer. Essentially, the Digital Phase Adjust timer delays when the output divider starts dividing; thereby shifting the phase of the output clock. The phase adjust resolution is a function of the divide function. Coarse phase adjust parameters include:

- Number of Phase Delay Steps – the number of phase delay steps available is equal to the divide ratio selected. For example, if a Divide by 4 is selected, then the Digital Phase Adjust can be programmed to select when the output divider changes state based upon selecting one of the four counts on the input. Figure 25 shows an example of divide by 16 in which there are 16 rising edges of Clock IN at which the output divider changes state (this particular example shows the fourth edge shifting the output by one fourth of the period of the output).
- Phase Delay Step Size – the step size is determined by the number of phase delay steps according to the following equations:

$$\text{Stepsize(deg)} = \frac{360 \text{ degrees}}{\text{OutputDivideRatio}} \quad (1)$$

$$\text{Stepsize(sec)} = \frac{\frac{1}{f_{\text{ClockIN}}}}{\text{OutputDivideRatio}} \quad (2)$$

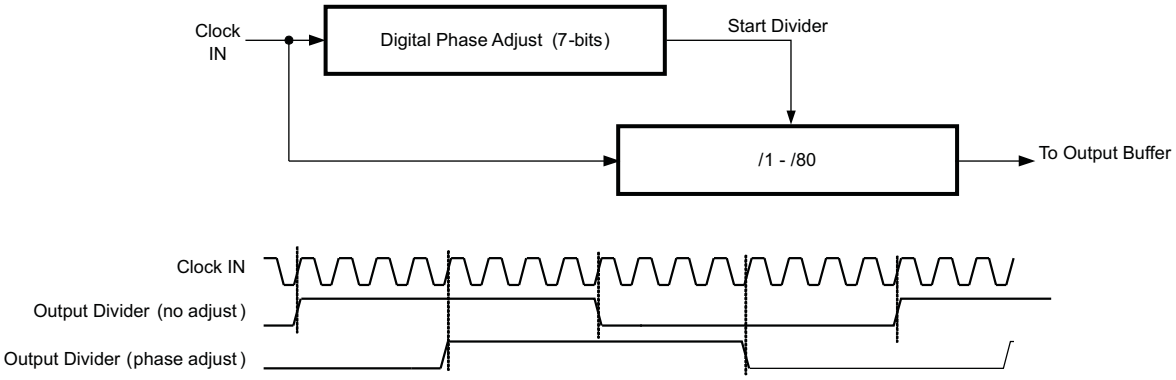


Figure 25. CDCE18005 Phase Adjust

Phase Adjust example

Given:

Output Frequency: 30.72 MHz
Input Frequency: 491.52 MHz
Output Divider Setting: 16

$$\text{Stepsize(deg)} = \frac{360}{16} = 22.5^{\circ}/\text{Step} \quad (3)$$

The tables that follow provide a list of valid register settings for the digital phase adjust blocks.

Table 21. CDCE18005 Output Coarse Phase Adjust Settings (1)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/2)
3	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/3)
	0	0	0	0	0	1	0	2(2π/3)
4	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/4)
	0	0	0	0	0	1	0	2(2π/4)
	0	0	0	0	0	1	1	3(2π/4)
5	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/5)
	0	0	0	0	0	1	0	2(2π/5)
	0	0	0	0	0	1	1	3(2π/5)
	0	0	0	0	1	0	0	4(2π/5)
6	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/6)
	0	0	0	0	0	1	0	2(2π/6)
	1	0	0	0	0	0	0	3(2π/6)
	1	0	0	0	0	0	1	4(2π/6)
	1	0	0	0	0	1	0	5(2π/6)
8	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/8)
	0	0	0	0	0	1	0	2(2π/8)
	0	0	0	0	0	1	1	3(2π/8)
	1	0	0	0	0	0	0	4(2π/8)
	1	0	0	0	0	0	1	5(2π/8)
	1	0	0	0	0	1	0	6(2π/8)
	1	0	0	0	0	1	1	7(2π/8)
10	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/10)
	0	0	0	0	0	1	0	2(2π/10)
	0	0	0	0	0	1	1	3(2π/10)
	0	0	0	0	1	0	0	4(2π/10)
	1	0	0	0	0	0	0	5(2π/10)
	1	0	0	0	0	0	1	6(2π/10)
	1	0	0	0	0	1	0	7(2π/10)
	1	0	0	0	0	1	1	8(2π/10)
	1	0	0	0	1	0	0	9(2π/10)
12	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/12)
	0	0	0	0	0	1	0	2(2π/12)
	0	0	0	1	0	0	0	3(2π/12)
	0	0	0	1	0	0	1	4(2π/12)
	0	0	0	1	0	1	0	5(2π/12)
	0	0	1	0	0	0	0	6(2π/12)
	0	0	1	0	0	0	1	7(2π/12)
	0	0	1	0	0	1	0	8(2π/12)
	0	0	1	1	0	0	0	9(2π/12)
	0	0	1	1	0	0	1	10(2π/12)
	0	0	1	1	0	1	0	11(2π/12)
16	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/16)
	0	0	0	0	0	1	0	2(2π/16)
	0	0	0	0	0	1	1	3(2π/16)
	0	0	0	1	0	0	0	4(2π/16)
	0	0	0	1	0	0	1	5(2π/16)
	0	0	0	1	0	1	0	6(2π/16)
	0	0	0	1	0	1	1	7(2π/16)
	0	0	1	0	0	0	0	8(2π/16)
	0	0	1	0	0	0	1	9(2π/16)
	0	0	1	0	0	1	0	10(2π/16)
	0	0	1	0	0	1	1	11(2π/16)
	0	0	1	1	0	0	0	12(2π/16)
	0	0	1	1	0	0	1	13(2π/16)
	0	0	1	1	0	1	0	14(2π/16)
	0	0	1	1	0	1	1	15(2π/16)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
18	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/18)
	0	0	0	0	0	1	0	2(2π/18)
	0	0	0	1	0	0	0	3(2π/18)
	0	0	0	1	0	0	1	4(2π/18)
	0	0	0	1	0	1	0	5(2π/18)
	0	0	1	0	0	0	0	6(2π/18)
	0	0	1	0	0	0	1	7(2π/18)
	0	0	1	0	0	1	0	8(2π/18)
	0	0	1	1	0	0	0	9(2π/18)
	0	0	1	1	0	0	1	10(2π/18)
	0	0	1	1	0	1	0	11(2π/18)
	0	1	0	0	0	0	0	12(2π/18)
	0	1	0	0	0	0	1	13(2π/18)
	0	1	0	0	0	1	0	14(2π/18)
	0	1	0	1	0	0	0	15(2π/18)
	0	1	0	1	0	0	1	16(2π/18)
	0	1	0	1	0	1	0	17(2π/18)
20	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/20)
	0	0	0	0	0	1	0	2(2π/20)
	0	0	0	0	0	1	1	3(2π/20)
	0	0	0	0	1	0	0	4(2π/20)
	0	0	0	1	0	0	0	5(2π/20)
	0	0	0	1	0	0	1	6(2π/20)
	0	0	0	1	0	1	0	7(2π/20)
	0	0	0	1	0	1	1	8(2π/20)
	0	0	0	1	1	0	0	9(2π/20)
	0	0	1	0	0	0	0	10(2π/20)
	0	0	1	0	0	0	1	11(2π/20)
	0	0	1	0	0	1	0	12(2π/20)
	0	0	1	0	0	1	1	13(2π/20)
	0	0	1	0	1	0	0	14(2π/20)
	0	0	1	1	0	0	0	15(2π/20)
	0	0	1	1	0	0	1	16(2π/20)
	0	0	1	1	0	1	0	17(2π/20)
	0	0	1	1	0	1	1	18(2π/20)
	0	0	1	1	1	0	0	19(2π/20)
24	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/24)
	0	0	0	0	0	1	0	2(2π/24)
	0	0	0	0	0	1	1	3(2π/24)
	0	0	0	1	0	0	0	4(2π/24)
	0	0	0	1	0	0	1	5(2π/24)
	0	0	0	1	0	1	0	6(2π/24)
	0	0	0	1	0	1	1	7(2π/24)
	0	0	1	0	0	0	0	8(2π/24)
	0	0	1	0	0	0	1	9(2π/24)
	0	0	1	0	0	1	0	10(2π/24)
	0	0	1	0	0	1	1	11(2π/24)
	0	0	1	1	0	0	0	12(2π/24)
	0	0	1	1	0	0	1	13(2π/24)
	0	0	1	1	0	1	0	14(2π/24)
	0	0	1	1	0	1	1	15(2π/24)
	0	1	0	0	0	0	0	16(2π/24)
	0	1	0	0	0	0	1	17(2π/24)
	0	1	0	0	0	1	0	18(2π/24)
	0	1	0	0	0	1	1	19(2π/24)
	0	1	0	1	0	0	0	20(2π/24)
	0	1	0	1	0	0	1	21(2π/24)
	0	1	0	1	0	1	0	22(2π/24)
	0	1	0	1	0	1	1	23(2π/24)

Table 22. CDCE18005 Output Coarse Phase Adjust Settings (2)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
28	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/28)
	0	0	0	1	0	0	0	2(2π/28)
	0	0	0	1	0	0	1	3(2π/28)
	0	0	1	0	0	0	0	4(2π/28)
	0	0	1	0	0	0	1	5(2π/28)
	0	0	1	1	0	0	0	6(2π/28)
	0	0	1	1	0	0	1	7(2π/28)
	0	1	0	0	0	0	0	8(2π/28)
	0	1	0	0	0	0	1	9(2π/28)
	0	1	0	1	0	0	0	10(2π/28)
	0	1	0	1	0	0	1	11(2π/28)
	0	1	1	0	0	0	0	12(2π/28)
	0	1	1	0	0	0	1	13(2π/28)
	1	0	0	0	0	0	0	14(2π/28)
	1	0	0	0	0	0	1	15(2π/28)
	1	0	0	1	0	0	0	16(2π/28)
	1	0	0	1	0	0	1	17(2π/28)
	1	0	1	0	0	0	0	18(2π/28)
	1	0	1	0	0	0	1	19(2π/28)
	1	0	1	1	0	0	0	20(2π/28)
	1	0	1	1	0	0	1	21(2π/28)
	1	1	0	0	0	0	0	22(2π/28)
	1	1	0	0	0	0	1	23(2π/28)
	1	1	0	1	0	0	0	24(2π/28)
	1	1	0	1	0	0	1	25(2π/28)
	1	1	1	0	0	0	0	26(2π/28)
	1	1	1	0	0	0	1	27(2π/28)
30	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/30)
	0	0	0	0	0	1	0	2(2π/30)
	0	0	0	0	0	1	1	3(2π/30)
	0	0	0	0	1	0	0	4(2π/30)
	0	0	0	1	0	0	0	5(2π/30)
	0	0	0	1	0	0	1	6(2π/30)
	0	0	0	1	0	1	0	7(2π/30)
	0	0	0	1	0	1	1	8(2π/30)
	0	0	0	1	1	0	0	9(2π/30)
	0	0	1	0	0	0	0	10(2π/30)
	0	0	1	0	0	0	1	11(2π/30)
	0	0	1	0	0	1	0	12(2π/30)
	0	0	1	0	0	1	1	13(2π/30)
	0	0	1	0	1	0	0	14(2π/30)
	0	0	1	1	0	0	0	15(2π/30)
	0	0	1	1	0	0	1	16(2π/30)
	0	0	1	1	0	1	0	17(2π/30)
	0	0	1	1	0	1	1	18(2π/30)
	0	0	1	1	1	0	0	19(2π/30)
	0	1	0	0	0	0	0	20(2π/30)
	0	1	0	0	0	0	1	21(2π/30)
	0	1	0	0	0	1	0	22(2π/30)
	0	1	0	0	0	1	1	23(2π/30)
	0	1	0	0	1	0	0	24(2π/30)
	0	1	0	1	0	0	0	25(2π/30)
	0	1	0	1	0	0	1	26(2π/30)
	0	1	0	1	0	1	0	27(2π/30)
	0	1	0	1	0	1	1	28(2π/30)
	0	1	0	1	1	0	0	29(2π/30)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
32	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/32)
	0	0	0	0	0	1	0	2(2π/32)
	0	0	0	0	0	1	1	3(2π/32)
	0	0	0	1	0	0	0	4(2π/32)
	0	0	0	1	0	0	1	5(2π/32)
	0	0	0	1	0	1	0	6(2π/32)
	0	0	0	1	0	1	1	7(2π/32)
	0	0	1	0	0	0	0	8(2π/32)
	0	0	1	0	0	0	1	9(2π/32)
	0	0	1	0	0	1	0	10(2π/32)
	0	0	1	0	0	1	1	11(2π/32)
	0	0	1	1	0	0	0	12(2π/32)
	0	0	1	1	0	0	1	13(2π/32)
	0	0	1	1	0	1	0	14(2π/32)
	0	0	1	1	0	1	1	15(2π/32)
	0	1	0	0	0	0	0	16(2π/32)
	0	1	0	0	0	0	1	17(2π/32)
	0	1	0	0	0	1	0	18(2π/32)
	0	1	0	0	0	1	1	19(2π/32)
	0	1	0	1	0	0	0	20(2π/32)
	0	1	0	1	0	0	1	21(2π/32)
	0	1	0	1	0	1	0	22(2π/32)
	0	1	0	1	0	1	1	23(2π/32)
	0	1	1	0	0	0	0	24(2π/32)
	0	1	1	0	0	0	1	25(2π/32)
	0	1	1	0	0	1	0	26(2π/32)
	0	1	1	0	0	1	1	27(2π/32)
	0	1	1	1	0	0	0	28(2π/32)
	0	1	1	1	0	0	1	29(2π/32)
	0	1	1	1	0	1	0	30(2π/32)
	0	1	1	1	0	1	1	31(2π/32)
36	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/36)
	0	0	0	0	0	1	0	2(2π/36)
	0	0	0	1	0	0	0	3(2π/36)
	0	0	0	1	0	0	1	4(2π/36)
	0	0	0	1	0	1	0	5(2π/36)
	0	0	1	0	0	0	0	6(2π/36)
	0	0	1	0	0	0	1	7(2π/36)
	0	0	1	0	0	1	0	8(2π/36)
	0	0	1	1	0	0	0	9(2π/36)
	0	0	1	1	0	0	1	10(2π/36)
	0	0	1	1	0	1	0	11(2π/36)
	0	1	0	0	0	0	0	12(2π/36)
	0	1	0	0	0	0	1	13(2π/36)
	0	1	0	0	0	1	0	14(2π/36)
	0	1	0	1	0	0	0	15(2π/36)
	0	1	0	1	0	0	1	16(2π/36)
	0	1	0	1	0	1	0	17(2π/36)
	1	0	0	0	0	0	0	18(2π/36)
	1	0	0	0	0	0	1	19(2π/36)
	1	0	0	0	0	1	0	20(2π/36)
	1	0	0	1	0	0	0	21(2π/36)
	1	0	0	1	0	0	1	22(2π/36)
	1	0	0	1	0	1	0	23(2π/36)
	1	0	1	0	0	0	0	24(2π/36)
	1	0	1	0	0	0	1	25(2π/36)
	1	0	1	0	0	1	0	26(2π/36)
	1	0	1	1	0	0	0	27(2π/36)
	1	0	1	1	0	0	1	28(2π/36)
	1	0	1	1	0	1	0	29(2π/36)
	1	1	0	0	0	0	0	30(2π/36)
	1	1	0	0	0	0	1	31(2π/36)
	1	1	0	0	0	1	0	32(2π/36)
	1	1	0	1	0	0	0	33(2π/36)
	1	1	0	1	0	0	1	34(2π/36)
	1	1	0	1	0	1	0	35(2π/36)

Table 23. CDCE18005 Output Coarse Phase Adjust Settings (3)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
40	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/40)
	0	0	0	0	0	1	0	2(2π/40)
	0	0	0	0	0	1	1	3(2π/40)
	0	0	0	0	1	0	0	4(2π/40)
	0	0	0	1	0	0	0	5(2π/40)
	0	0	0	1	0	0	1	6(2π/40)
	0	0	0	1	0	1	0	7(2π/40)
	0	0	0	1	0	1	1	8(2π/40)
	0	0	0	1	1	0	0	9(2π/40)
	0	0	1	0	0	0	0	10(2π/40)
	0	0	1	0	0	0	1	11(2π/40)
	0	0	1	0	0	1	0	12(2π/40)
	0	0	1	0	0	1	1	13(2π/40)
	0	0	1	0	1	0	0	14(2π/40)
	0	0	1	1	0	0	0	15(2π/40)
	0	0	1	1	0	0	1	16(2π/40)
	0	0	1	1	0	1	0	17(2π/40)
	0	0	1	1	0	1	1	18(2π/40)
	0	0	1	1	1	0	0	19(2π/40)
	0	1	0	0	0	0	0	20(2π/40)
	0	1	0	0	0	0	1	21(2π/40)
	0	1	0	0	0	1	0	22(2π/40)
	0	1	0	0	0	1	1	23(2π/40)
	0	1	0	0	1	0	0	24(2π/40)
	0	1	0	1	0	0	0	25(2π/40)
	0	1	0	1	0	0	1	26(2π/40)
	0	1	0	1	0	1	0	27(2π/40)
	0	1	0	1	0	1	1	28(2π/40)
	0	1	0	1	1	0	0	29(2π/40)
	0	1	1	0	0	0	0	30(2π/40)
	0	1	1	0	0	0	1	31(2π/40)
	0	1	1	0	0	1	0	32(2π/40)
	0	1	1	0	0	1	1	33(2π/40)
	0	1	1	0	1	0	0	34(2π/40)
	0	1	1	1	0	0	0	35(2π/40)
	0	1	1	1	0	0	1	36(2π/40)
	0	1	1	1	0	1	0	37(2π/40)
	0	1	1	1	0	1	1	38(2π/40)
	0	1	1	1	1	0	0	39(2π/40)
42	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/42)
	0	0	0	0	0	1	0	2(2π/42)
	0	0	0	1	0	0	0	3(2π/42)
	0	0	0	1	0	0	1	4(2π/42)
	0	0	0	1	0	1	0	5(2π/42)
	0	0	1	0	0	0	0	6(2π/42)
	0	0	1	0	0	0	1	7(2π/42)
	0	0	1	0	0	1	0	8(2π/42)
	0	0	1	1	0	0	0	9(2π/42)
	0	0	1	1	0	0	1	10(2π/42)
	0	0	1	1	0	1	0	11(2π/42)
	0	1	0	0	0	0	0	12(2π/42)
	0	1	0	0	0	0	1	13(2π/42)
	0	1	0	0	0	1	0	14(2π/42)
	0	1	0	1	0	0	0	15(2π/42)
	0	1	0	1	0	0	1	16(2π/42)
	0	1	0	1	0	1	0	17(2π/42)
	0	1	1	0	0	0	0	18(2π/42)
	0	1	1	0	0	0	1	19(2π/42)
	0	1	1	0	0	1	0	20(2π/42)
	1	0	0	0	0	0	0	21(2π/42)
	1	0	0	0	0	0	1	22(2π/42)
	1	0	0	0	0	1	0	23(2π/42)
	1	0	0	1	0	0	0	24(2π/42)
	1	0	0	1	0	0	1	25(2π/42)
	1	0	0	1	0	1	0	26(2π/42)
	1	0	1	0	0	0	0	27(2π/42)
	1	0	1	0	0	0	1	28(2π/42)
	1	0	1	0	0	1	0	29(2π/42)
	1	0	1	1	0	0	0	30(2π/42)
	1	0	1	1	0	0	1	31(2π/42)
	1	0	1	1	0	1	0	32(2π/42)
	1	1	0	0	0	0	0	33(2π/42)
	1	1	0	0	0	0	1	34(2π/42)
	1	1	0	0	0	1	0	35(2π/42)
	1	1	0	1	0	0	0	36(2π/42)
	1	1	0	1	0	0	1	37(2π/42)
	1	1	0	1	0	1	0	38(2π/42)
	1	1	1	0	0	0	0	39(2π/42)
	1	1	1	0	0	0	1	40(2π/42)
	1	1	1	0	0	1	0	41(2π/42)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
48	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/48)
	0	0	0	0	0	1	0	2(2π/48)
	0	0	0	0	0	1	1	3(2π/48)
	0	0	0	1	0	0	0	4(2π/48)
	0	0	0	1	0	0	1	5(2π/48)
	0	0	0	1	0	1	0	6(2π/48)
	0	0	0	1	0	1	1	7(2π/48)
	0	0	1	0	0	0	0	8(2π/48)
	0	0	1	0	0	0	1	9(2π/48)
	0	0	1	0	0	1	0	10(2π/48)
	0	0	1	0	0	1	1	11(2π/48)
	0	0	1	1	0	0	0	12(2π/48)
	0	0	1	1	0	0	1	13(2π/48)
	0	0	1	1	0	1	0	14(2π/48)
	0	0	1	1	0	1	1	15(2π/48)
	0	1	0	0	0	0	0	16(2π/48)
	0	1	0	0	0	0	1	17(2π/48)
	0	1	0	0	0	1	0	18(2π/48)
	0	1	0	0	0	1	1	19(2π/48)
	0	1	0	1	0	0	0	20(2π/48)
	0	1	0	1	0	0	1	21(2π/48)
	0	1	0	1	0	1	0	22(2π/48)
	0	1	0	1	0	1	1	23(2π/48)
	1	0	0	0	0	0	0	24(2π/48)
	1	0	0	0	0	0	1	25(2π/48)
	1	0	0	0	0	1	0	26(2π/48)
	1	0	0	0	0	1	1	27(2π/48)
	1	0	0	1	0	0	0	28(2π/48)
	1	0	0	1	0	0	1	29(2π/48)
	1	0	0	1	0	1	0	30(2π/48)
	1	0	0	1	0	1	1	31(2π/48)
	1	0	1	0	0	0	0	32(2π/48)
	1	0	1	0	0	0	1	33(2π/48)
	1	0	1	0	0	1	0	34(2π/48)
	1	0	1	0	0	1	1	35(2π/48)
	1	0	1	1	0	0	0	36(2π/48)
	1	0	1	1	0	0	1	37(2π/48)
	1	0	1	1	0	1	0	38(2π/48)
	1	0	1	1	0	1	1	39(2π/48)
	1	1	0	0	0	0	0	40(2π/48)
	1	1	0	0	0	0	1	41(2π/48)
	1	1	0	0	0	1	0	42(2π/48)
	1	1	0	0	0	1	1	43(2π/48)
	1	1	0	1	0	0	0	44(2π/48)
	1	1	0	1	0	0	1	45(2π/48)
	1	1	0	1	0	1	0	46(2π/48)
	1	1	0	1	0	1	1	47(2π/48)

Table 24. CDCE18005 Output Coarse Phase Adjust Settings (4)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
50	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/50)
	0	0	0	0	0	1	0	2(2π/50)
	0	0	0	0	0	1	1	3(2π/50)
	0	0	0	0	1	0	0	4(2π/50)
	0	0	0	1	0	0	0	5(2π/50)
	0	0	0	1	0	0	1	6(2π/50)
	0	0	0	1	0	1	0	7(2π/50)
	0	0	0	1	0	1	1	8(2π/50)
	0	0	0	1	1	0	0	9(2π/50)
	0	0	1	0	0	0	0	10(2π/50)
	0	0	1	0	0	0	1	11(2π/50)
	0	0	1	0	0	1	0	12(2π/50)
	0	0	1	0	0	1	1	13(2π/50)
	0	0	1	0	1	0	0	14(2π/50)
	0	0	1	1	0	0	0	15(2π/50)
	0	0	1	1	0	0	1	16(2π/50)
	0	0	1	1	0	1	0	17(2π/50)
	0	0	1	1	0	1	1	18(2π/50)
	0	0	1	1	1	0	0	19(2π/50)
	0	1	0	0	0	0	0	20(2π/50)
	0	1	0	0	0	0	1	21(2π/50)
	0	1	0	0	0	1	0	22(2π/50)
	0	1	0	0	0	1	1	23(2π/50)
	0	1	0	0	1	0	0	24(2π/50)
	1	0	0	0	0	0	0	25(2π/50)
	1	0	0	0	0	0	1	26(2π/50)
	1	0	0	0	0	1	0	27(2π/50)
	1	0	0	0	0	1	1	28(2π/50)
	1	0	0	0	1	0	0	29(2π/50)
	1	0	0	1	0	0	0	30(2π/50)
	1	0	0	1	0	0	1	31(2π/50)
	1	0	0	1	0	1	0	32(2π/50)
	1	0	0	1	0	1	1	33(2π/50)
	1	0	0	1	1	0	0	34(2π/50)
	1	0	1	0	0	0	0	35(2π/50)
	1	0	1	0	0	0	1	36(2π/50)
	1	0	1	0	0	1	0	37(2π/50)
	1	0	1	0	0	1	1	38(2π/50)
	1	0	1	0	1	0	0	39(2π/50)
	1	0	1	1	0	0	0	40(2π/50)
	1	0	1	1	0	0	1	41(2π/50)
	1	0	1	1	0	1	0	42(2π/50)
	1	0	1	1	0	1	1	43(2π/50)
	1	0	1	1	1	0	0	44(2π/50)
	1	1	0	0	0	0	0	45(2π/50)
	1	1	0	0	0	0	1	46(2π/50)
	1	1	0	0	0	1	0	47(2π/50)
	1	1	0	0	0	1	1	48(2π/50)
	1	1	0	0	1	0	0	49(2π/50)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
56	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/56)
	0	0	0	0	0	1	0	2(2π/56)
	0	0	0	0	0	1	1	3(2π/56)
	0	0	0	0	1	0	0	4(2π/56)
	0	0	0	1	0	0	1	5(2π/56)
	0	0	0	1	0	1	0	6(2π/56)
	0	0	0	1	0	1	1	7(2π/56)
	0	0	1	0	0	0	0	8(2π/56)
	0	0	1	0	0	0	1	9(2π/56)
	0	0	1	0	0	1	0	10(2π/56)
	0	0	1	0	0	1	1	11(2π/56)
	0	0	1	1	0	0	0	12(2π/56)
	0	0	1	1	0	0	1	13(2π/56)
	0	0	1	1	0	1	0	14(2π/56)
	0	0	1	1	0	1	1	15(2π/56)
	0	1	0	0	0	0	0	16(2π/56)
	0	1	0	0	0	0	1	17(2π/56)
	0	1	0	0	0	1	0	18(2π/56)
	0	1	0	0	0	1	1	19(2π/56)
	0	1	0	1	0	0	0	20(2π/56)
	0	1	0	1	0	0	1	21(2π/56)
	0	1	0	1	0	1	0	22(2π/56)
	0	1	0	1	0	1	1	23(2π/56)
	0	1	1	0	0	0	0	24(2π/56)
	0	1	1	0	0	0	1	25(2π/56)
	0	1	1	0	0	1	0	26(2π/56)
	0	1	1	0	0	1	1	27(2π/56)
	1	0	0	0	0	0	0	28(2π/56)
	1	0	0	0	0	0	1	29(2π/56)
	1	0	0	0	0	1	0	30(2π/56)
	1	0	0	0	0	1	1	31(2π/56)
	1	0	0	1	0	0	0	32(2π/56)
	1	0	0	1	0	0	1	33(2π/56)
	1	0	0	1	0	1	0	34(2π/56)
	1	0	0	1	0	1	1	35(2π/56)
	1	0	1	0	0	0	0	36(2π/56)
	1	0	1	0	0	0	1	37(2π/56)
	1	0	1	0	0	1	0	38(2π/56)
	1	0	1	0	0	1	1	39(2π/56)
	1	0	1	1	0	0	0	40(2π/56)
	1	0	1	1	0	0	1	41(2π/56)
	1	0	1	1	0	1	0	42(2π/56)
	1	0	1	1	0	1	1	43(2π/56)
	1	1	0	0	0	0	0	44(2π/56)
	1	1	0	0	0	0	1	45(2π/56)
	1	1	0	0	0	1	0	46(2π/56)
	1	1	0	0	0	1	1	47(2π/56)
	1	1	0	1	0	0	0	48(2π/56)
	1	1	0	1	0	0	1	49(2π/56)
	1	1	0	1	0	1	0	50(2π/56)
	1	1	0	1	0	1	1	51(2π/56)
	1	1	1	0	0	0	0	52(2π/56)
	1	1	1	0	0	0	1	53(2π/56)
	1	1	1	0	0	1	0	54(2π/56)
	1	1	1	0	0	1	1	55(2π/56)

Table 25. CDCE18005 Output Coarse Phase Adjust Settings (5)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
60	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/60)
	0	0	0	0	0	1	0	2(2π/60)
	0	0	0	0	0	1	1	3(2π/60)
	0	0	0	0	1	0	0	4(2π/60)
	0	0	0	1	0	0	0	5(2π/60)
	0	0	0	1	0	0	1	6(2π/60)
	0	0	0	1	0	1	0	7(2π/60)
	0	0	0	1	0	1	1	8(2π/60)
	0	0	0	1	1	0	0	9(2π/60)
	0	0	1	0	0	0	0	10(2π/60)
	0	0	1	0	0	0	1	11(2π/60)
	0	0	1	0	0	1	0	12(2π/60)
	0	0	1	0	0	1	1	13(2π/60)
	0	0	1	0	1	0	0	14(2π/60)
	0	0	1	1	0	0	0	15(2π/60)
	0	0	1	1	0	0	1	16(2π/60)
	0	0	1	1	0	1	0	17(2π/60)
	0	0	1	1	0	1	1	18(2π/60)
	0	0	1	1	1	0	0	19(2π/60)
	0	1	0	0	0	0	0	20(2π/60)
	0	1	0	0	0	0	1	21(2π/60)
	0	1	0	0	0	1	0	22(2π/60)
	0	1	0	0	0	1	1	23(2π/60)
	0	1	0	0	1	0	0	24(2π/60)
	0	1	0	1	0	0	0	25(2π/60)
	0	1	0	1	0	0	1	26(2π/60)
	0	1	0	1	0	1	0	27(2π/60)
	0	1	0	1	0	1	1	28(2π/60)
	0	1	0	1	1	0	0	29(2π/60)
	1	0	0	0	0	0	0	30(2π/60)
	1	0	0	0	0	0	1	31(2π/60)
	1	0	0	0	0	1	0	32(2π/60)
	1	0	0	0	0	1	1	33(2π/60)
	1	0	0	0	1	0	0	34(2π/60)
	1	0	0	1	0	0	0	35(2π/60)
	1	0	0	1	0	0	1	36(2π/60)
	1	0	0	1	0	1	0	37(2π/60)
	1	0	0	1	0	1	1	38(2π/60)
	1	0	0	1	1	0	0	39(2π/60)
	1	0	1	0	0	0	0	40(2π/60)
	1	0	1	0	0	0	1	41(2π/60)
	1	0	1	0	0	1	0	42(2π/60)
	1	0	1	0	0	1	1	43(2π/60)
	1	0	1	0	1	0	0	44(2π/60)
	1	0	1	1	0	0	0	45(2π/60)
	1	0	1	1	0	0	1	46(2π/60)
	1	0	1	1	0	1	0	47(2π/60)
	1	0	1	1	0	1	1	48(2π/60)
	1	0	1	1	1	0	0	49(2π/60)
	1	1	0	0	0	0	0	50(2π/60)
	1	1	0	0	0	0	1	51(2π/60)
	1	1	0	0	0	1	0	52(2π/60)
	1	1	0	0	0	1	1	53(2π/60)
	1	1	0	0	1	0	0	54(2π/60)
	1	1	0	1	0	0	0	55(2π/60)
	1	1	0	1	0	0	1	56(2π/60)
	1	1	0	1	0	1	0	57(2π/60)
	1	1	0	1	0	1	1	58(2π/60)
	1	1	0	1	1	0	0	59(2π/60)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
64	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/64)
	0	0	0	0	0	1	0	2(2π/64)
	0	0	0	0	0	1	1	3(2π/64)
	0	0	0	1	0	0	0	4(2π/64)
	0	0	0	1	0	0	1	5(2π/64)
	0	0	0	1	0	1	0	6(2π/64)
	0	0	0	1	0	1	1	7(2π/64)
	0	0	1	0	0	0	0	8(2π/64)
	0	0	1	0	0	0	1	9(2π/64)
	0	0	1	0	0	1	0	10(2π/64)
	0	0	1	0	0	1	1	11(2π/64)
	0	0	1	1	0	0	0	12(2π/64)
	0	0	1	1	0	0	1	13(2π/64)
	0	0	1	1	0	1	0	14(2π/64)
	0	0	1	1	0	1	1	15(2π/64)
	0	1	0	0	0	0	0	16(2π/64)
	0	1	0	0	0	0	1	17(2π/64)
	0	1	0	0	0	1	0	18(2π/64)
	0	1	0	0	0	1	1	19(2π/64)
	0	1	0	1	0	0	0	20(2π/64)
	0	1	0	1	0	0	1	21(2π/64)
	0	1	0	1	0	1	0	22(2π/64)
	0	1	0	1	0	1	1	23(2π/64)
	0	1	1	0	0	0	0	24(2π/64)
	0	1	1	0	0	0	1	25(2π/64)
	0	1	1	0	0	1	0	26(2π/64)
	0	1	1	0	0	1	1	27(2π/64)
	0	1	1	1	0	0	0	28(2π/64)
	0	1	1	1	0	0	1	29(2π/64)
	0	1	1	1	0	1	0	30(2π/64)
	0	1	1	1	0	1	1	31(2π/64)
	1	0	0	0	0	0	0	32(2π/64)
	1	0	0	0	0	0	1	33(2π/64)
	1	0	0	0	0	1	0	34(2π/64)
	1	0	0	0	0	1	1	35(2π/64)
	1	0	0	1	0	0	0	36(2π/64)
	1	0	0	1	0	0	1	37(2π/64)
	1	0	0	1	0	1	0	38(2π/64)
	1	0	0	1	0	1	1	39(2π/64)
	1	0	1	0	0	0	0	40(2π/64)
	1	0	1	0	0	0	1	41(2π/64)
	1	0	1	0	0	1	0	42(2π/64)
	1	0	1	0	0	1	1	43(2π/64)
	1	0	1	1	0	0	0	44(2π/64)
	1	0	1	1	0	0	1	45(2π/64)
	1	0	1	1	0	1	0	46(2π/64)
	1	0	1	1	0	1	1	47(2π/64)
	1	1	0	0	0	0	0	48(2π/64)
	1	1	0	0	0	0	1	49(2π/64)
	1	1	0	0	0	1	0	50(2π/64)
	1	1	0	0	0	1	1	51(2π/64)
	1	1	0	1	0	0	0	52(2π/64)
	1	1	0	1	0	0	1	53(2π/64)
	1	1	0	1	0	1	0	54(2π/64)
	1	1	0	1	0	1	1	55(2π/64)
	1	1	1	0	0	0	0	56(2π/64)
	1	1	1	0	0	0	1	57(2π/64)
	1	1	1	0	0	1	0	58(2π/64)
	1	1	1	0	0	1	1	59(2π/64)
	1	1	1	1	0	0	0	60(2π/64)
	1	1	1	1	0	0	1	61(2π/64)
	1	1	1	1	0	1	0	62(2π/64)
	1	1	1	1	0	1	1	63(2π/64)

Table 26. CDCE18005 Output Coarse Phase Adjust Settings (6)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
70	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/70)
	0	0	0	0	0	1	0	2(2π/70)
	0	0	0	0	0	1	1	3(2π/70)
	0	0	0	0	1	0	0	4(2π/70)
	0	0	0	1	0	0	0	5(2π/70)
	0	0	0	1	0	0	1	6(2π/70)
	0	0	0	1	0	1	0	7(2π/70)
	0	0	0	1	0	1	1	8(2π/70)
	0	0	0	1	1	0	0	9(2π/70)
	0	0	1	0	0	0	0	10(2π/70)
	0	0	1	0	0	0	1	11(2π/70)
	0	0	1	0	0	1	0	12(2π/70)
	0	0	1	0	0	1	1	13(2π/70)
	0	0	1	0	1	0	0	14(2π/70)
	0	0	1	1	0	0	0	15(2π/70)
	0	0	1	1	0	0	1	16(2π/70)
	0	0	1	1	0	1	0	17(2π/70)
	0	0	1	1	0	1	1	18(2π/70)
	0	0	1	1	1	0	0	19(2π/70)
	0	1	0	0	0	0	0	20(2π/70)
	0	1	0	0	0	0	1	21(2π/70)
	0	1	0	0	0	1	0	22(2π/70)
	0	1	0	0	0	1	1	23(2π/70)
	0	1	0	0	1	0	0	24(2π/70)
	0	1	0	1	0	0	0	25(2π/70)
	0	1	0	1	0	0	1	26(2π/70)
	0	1	0	1	0	1	0	27(2π/70)
	0	1	0	1	0	1	1	28(2π/70)
	0	1	0	1	1	0	0	29(2π/70)
	0	1	1	0	0	0	0	30(2π/70)
	0	1	1	0	0	0	1	31(2π/70)
	0	1	1	0	0	1	0	32(2π/70)
	0	1	1	0	0	1	1	33(2π/70)
	0	1	1	0	1	0	0	34(2π/70)
	1	0	0	0	0	0	0	35(2π/70)
	1	0	0	0	0	0	1	36(2π/70)
	1	0	0	0	0	1	0	37(2π/70)
	1	0	0	0	0	1	1	38(2π/70)
	1	0	0	0	1	0	0	39(2π/70)
	1	0	0	1	0	0	0	40(2π/70)
	1	0	0	1	0	0	1	41(2π/70)
	1	0	0	1	0	1	0	42(2π/70)
	1	0	0	1	0	1	1	43(2π/70)
	1	0	0	1	1	0	0	44(2π/70)
	1	0	1	0	0	0	0	45(2π/70)
	1	0	1	0	0	0	1	46(2π/70)
	1	0	1	0	0	1	0	47(2π/70)
	1	0	1	0	0	1	1	48(2π/70)
	1	0	1	0	1	0	0	49(2π/70)
	1	0	1	1	0	0	0	50(2π/70)
	1	0	1	1	0	0	1	51(2π/70)
	1	0	1	1	0	1	0	52(2π/70)
	1	0	1	1	0	1	1	53(2π/70)
	1	0	1	1	1	0	0	54(2π/70)
	1	1	0	0	0	0	0	55(2π/70)
	1	1	0	0	0	0	1	56(2π/70)
	1	1	0	0	0	1	0	57(2π/70)
	1	1	0	0	0	1	1	58(2π/70)
	1	1	0	0	1	0	0	59(2π/70)
	1	1	0	1	0	0	0	60(2π/70)
	1	1	0	1	0	0	1	61(2π/70)
	1	1	0	1	0	1	0	62(2π/70)
	1	1	0	1	0	1	1	63(2π/70)
	1	1	0	1	1	0	0	64(2π/70)
	1	1	1	0	0	0	0	65(2π/70)
	1	1	1	0	0	0	1	66(2π/70)
	1	1	1	0	0	1	0	67(2π/70)
	1	1	1	0	0	1	1	68(2π/70)
	1	1	1	0	1	0	0	69(2π/70)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
80	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/80)
	0	0	0	0	0	1	0	2(2π/80)
	0	0	0	0	0	1	1	3(2π/80)
	0	0	0	0	1	0	0	4(2π/80)
	0	0	0	1	0	0	0	5(2π/80)
	0	0	0	1	0	0	1	6(2π/80)
	0	0	0	1	0	1	0	7(2π/80)
	0	0	0	1	0	1	1	8(2π/80)
	0	0	0	1	1	0	0	9(2π/80)
	0	0	1	0	0	0	0	10(2π/80)
	0	0	1	0	0	0	1	11(2π/80)
	0	0	1	0	0	1	0	12(2π/80)
	0	0	1	0	0	1	1	13(2π/80)
	0	0	1	0	1	0	0	14(2π/80)
	0	0	1	1	0	0	0	15(2π/80)
	0	0	1	1	0	0	1	16(2π/80)
	0	0	1	1	0	1	0	17(2π/80)
	0	0	1	1	0	1	1	18(2π/80)
	0	0	1	1	1	0	0	19(2π/80)
	0	1	0	0	0	0	0	20(2π/80)
	0	1	0	0	0	0	1	21(2π/80)
	0	1	0	0	0	1	0	22(2π/80)
	0	1	0	0	0	1	1	23(2π/80)
	0	1	0	0	1	0	0	24(2π/80)
	0	1	0	1	0	0	0	25(2π/80)
	0	1	0	1	0	0	1	26(2π/80)
	0	1	0	1	0	1	0	27(2π/80)
	0	1	0	1	0	1	1	28(2π/80)
	0	1	0	1	1	0	0	29(2π/80)
	0	1	1	0	0	0	0	30(2π/80)
	0	1	1	0	0	0	1	31(2π/80)
	0	1	1	0	0	1	0	32(2π/80)
	0	1	1	0	0	1	1	33(2π/80)
	0	1	1	0	1	0	0	34(2π/80)
	0	1	1	1	0	0	0	35(2π/80)
	0	1	1	1	0	0	1	36(2π/80)
	0	1	1	1	0	1	0	37(2π/80)
	0	1	1	1	0	1	1	38(2π/80)
	0	1	1	1	1	0	0	39(2π/80)
	1	0	0	0	0	0	0	40(2π/80)
	1	0	0	0	0	0	1	41(2π/80)
	1	0	0	0	0	1	0	42(2π/80)
	1	0	0	0	0	1	1	43(2π/80)
	1	0	0	0	1	0	0	44(2π/80)
	1	0	0	1	0	0	0	45(2π/80)
	1	0	0	1	0	0	1	46(2π/80)
	1	0	0	1	0	1	0	47(2π/80)
	1	0	0	1	0	1	1	48(2π/80)
	1	0	0	1	1	0	0	49(2π/80)
	1	0	1	0	0	0	0	50(2π/80)
	1	0	1	0	0	0	1	51(2π/80)
	1	0	1	0	0	1	0	52(2π/80)
	1	0	1	0	0	1	1	53(2π/80)
	1	0	1	0	1	0	0	54(2π/80)
	1	0	1	1	0	0	0	55(2π/80)
	1	0	1	1	0	0	1	56(2π/80)
	1	0	1	1	0	1	0	57(2π/80)
	1	0	1	1	0	1	1	58(2π/80)
	1	0	1	1	1	0	0	59(2π/80)
	1	1	0	0	0	0	0	60(2π/80)
	1	1	0	0	0	0	1	61(2π/80)
	1	1	0	0	0	1	0	62(2π/80)
	1	1	0	0	0	1	1	63(2π/80)
	1	1	0	0	1	0	0	64(2π/80)
	1	1	0	1	0	0	0	65(2π/80)
	1	1	0	1	0	0	1	66(2π/80)
	1	1	0	1	0	1	0	67(2π/80)
	1	1	0	1	0	1	1	68(2π/80)
	1	1	0	1	1	0	0	69(2π/80)
	1	1	1	0	0	0	0	70(2π/80)
	1	1	1	0	0	0	1	71(2π/80)
	1	1	1	0	0	1	0	72(2π/80)
	1	1	1	0	0	1	1	73(2π/80)
	1	1	1	0	1	0	0	74(2π/80)
	1	1	1	1	0	0	0	75(2π/80)
	1	1	1	1	0	0	1	76(2π/80)
	1	1	1	1	0	1	0	77(2π/80)
	1	1	1	1	0	1	1	78(2π/80)
	1	1	1	1	1	0	0	79(2π/80)

Crystal Input Interface

Fundamental mode is the recommended oscillation mode of operation for the input crystal and parallel resonance is the recommended type of circuit for the crystal.

A crystal load capacitance refers to all capacitances in the oscillator feedback loop. It is equal to the amount of capacitance seen between the terminals of the crystal in the circuit. For parallel resonant mode circuits, the correct load capacitance is necessary to ensure the oscillation of the crystal within the expected parameters.

The CDCE18005 implements an input crystal oscillator circuitry, known as the Colpitts oscillator, and requires one pad of the crystal to interface with the AUX_IN pin; the other pad of the crystal is tied to ground. In this crystal interface, it is important to account for all sources of capacitance when calculating the correct value for the discrete capacitor component, C_L, for a design.

The CDCE18005 has been characterized with 10-pF parallel resonant crystals. The input crystal oscillator stage in the CDCE18005 is designed to oscillate at the correct frequency for all parallel resonant crystals with low-pull capability and rated with a load capacitance that is equal to the sum of the on-chip load capacitance at the AUX_IN pin (10-pF), crystal stray capacitance, and board parasitic capacitance between the crystal and AUX_IN pin.

The normalized frequency error of the crystal, as a result of load capacitance mismatch, can be calculated as Equation 4:

$$\frac{\Delta f}{f} = \frac{C_S}{2\left(C_{L,R} + C_O\right)} - \frac{C_S}{2\left(C_{L,A} + C_O\right)} \quad (4)$$

Where:

- C_S is the motional capacitance of the crystal
- C_O is the shunt capacitance of the crystal
- $C_{L,R}$ is the rated load capacitance for the crystal
- $C_{L,A}$ is the actual load capacitance in the implemented PCB for the crystal
- Δf is the frequency error of the crystal
- f is the rated frequency of the crystal

The first three parameters can be obtained from the crystal vendor.

In order to minimize the frequency error of the crystal to meet application requirements, the difference between the rated load capacitance and the actual load capacitance should be minimized and a crystal with low-pull capability (low C_S) should be used.

For example, if an application requires less than ±50 ppm frequency error and a crystal with less than ±50 ppm frequency tolerance is picked, the characteristics are as follows: C_O = 7 pF, CS = 10 Δf, and $C_{L,R}$ = 12 pF. In order to meet the required frequency error, calculate $C_{L,A}$ using Equation 2 to be 17 pF. Subtracting $C_{L,R}$ from $C_{L,A}$, results in 5 pF; care must be taken during printed circuit board (PCB) layout with the crystal and the CDCE18005 to ensure that the sum of the crystal stray capacitance and board parasitic capacitance is less than the calculated 5 pF. Good layout practices are fundamental to the correct operation and reliability of the oscillator. It is critical to locate the crystal components very close to the XIN pin to minimize routing distances. Long traces in the oscillator circuit are a common source of problems. Do not route other signals across the oscillator circuit. Also, make sure power and high-frequency traces are routed as far away as possible to avoid crosstalk and noise coupling. Avoid the use of vias; if the routing becomes very complex, it is better to use 0-Ω resistors as bridges to go over other signals. Vias in the oscillator circuit should only be used for connections to the ground plane. Do not share ground connections; instead, make a separate connection to ground for each component that requires grounding. If possible, place multiple vias in parallel for each connection to the ground plane. Especially in the Colpitts oscillator configuration, the oscillator is very sensitive to capacitance in parallel with the crystal. Therefore, the layout must be designed to minimize stray capacitance across the crystal to less than 5 pF total under all circumstances to ensure proper crystal oscillation. Be sure to take into account both PCB and crystal stray capacitance.

Auxiliary Output

Figure 26 shows the auxiliary output port. Table 27 lists how the auxiliary output port is controlled. The output buffer supports a maximum output frequency of 250 MHz and drives at LVCMOS levels. See Table 20 for the list of divider settings that establishes the output frequency.

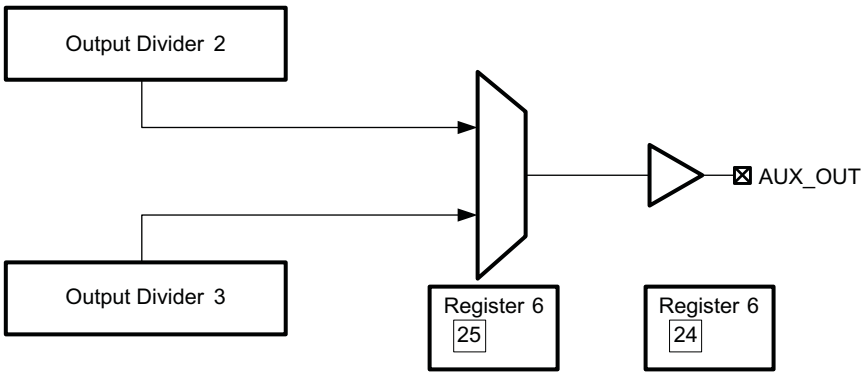


Figure 26. CDCE18005 Auxiliary Output

Table 27. CDCE18005 Auxiliary Output Settings

Bit Name →	AUXFEEDSEL	AUXOUTEN	AUX_OUT SOURCE
Register.Bit →	6.25	6.24	
	X	0	OFF
	0	1	Divider 2
	1	1	Divider 3

DEVICE POWER CALCULATION AND THERMAL MANAGEMENT

The CDCE18005 is a high performance device, therefore careful attention must be paid to device configuration and printed circuit board layout with respect to power consumption. Table 28 provides the power consumption for the individual blocks within the CDCE18005. To estimate total power consumption, calculate the sum of the products of the number of blocks used and the power dissipated of each corresponding block.

Provide Sample Calculation Here after numbers become available.

Table 28. CDCE18005 Power Consumption

Internal Block Power at 3.3V (typ)		Power Dissipated per Block	Number of Blocks
Input and Control Circuit		450 mW	1
Output Dividers	Divider = 1	60 mW	5
	Divider > 1	140 mW	5
LVPECL Output Buffer		75 mW(1)	5
LVDS Output Buffer		76 mW	5
LVCMOS Output Buffer	Static	7 mW	10
	Transient, 'C_L' load, 'f_{OUT}' MHz output frequency, 'V' output swing	$3.3 \times V \times f_{OUT} \times (C_L + 20 \times 10^{-12}) \times 10^3$	10

(1) Approximately 50 mW power dissipates externally at termination resistors per LVPECL output pair.

This power estimate determines the degree of thermal management required for a specific design. Employing the thermally enhanced printed circuit board layout shown in Figure 28 insures that the thermal performance curves shown in Figure 27 apply. Observing good thermal layout practices enables the thermal pad on the backside of the QFN-48 package to provide a good thermal path between the die contained within the package and the ambient air. This thermal pad also serves as the ground connection the device; therefore, a low inductance connection to the ground plane is essential.

Figure 28 shows a layout optimized for good thermal performance and a good power supply connection as well. The 7×7 filled via patter facilitates both considerations. Finally, the recommended layout achieves θ_{JA} = 27.3°C/W in still air and 20.3°C/W in an environment with 100 LFM airflow if implemented on a JEDEC compliant thermal test board.

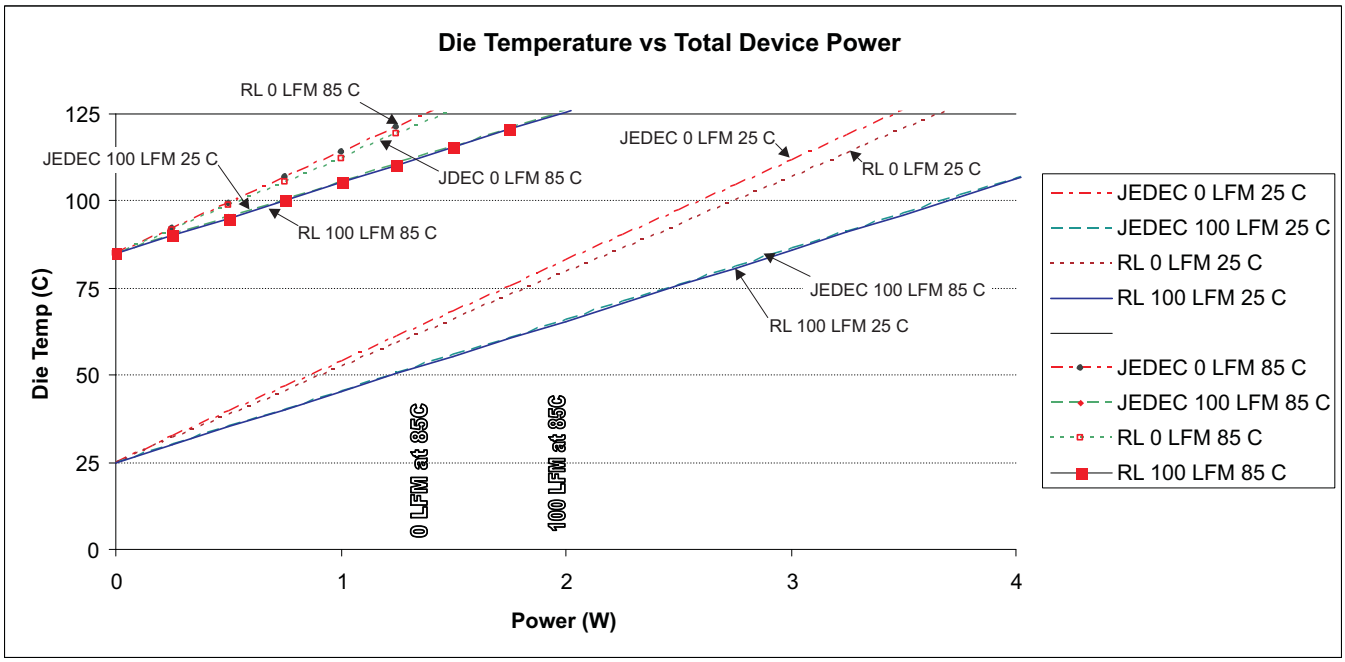


Figure 27. CDCE18005 Die Temperature vs Device Power

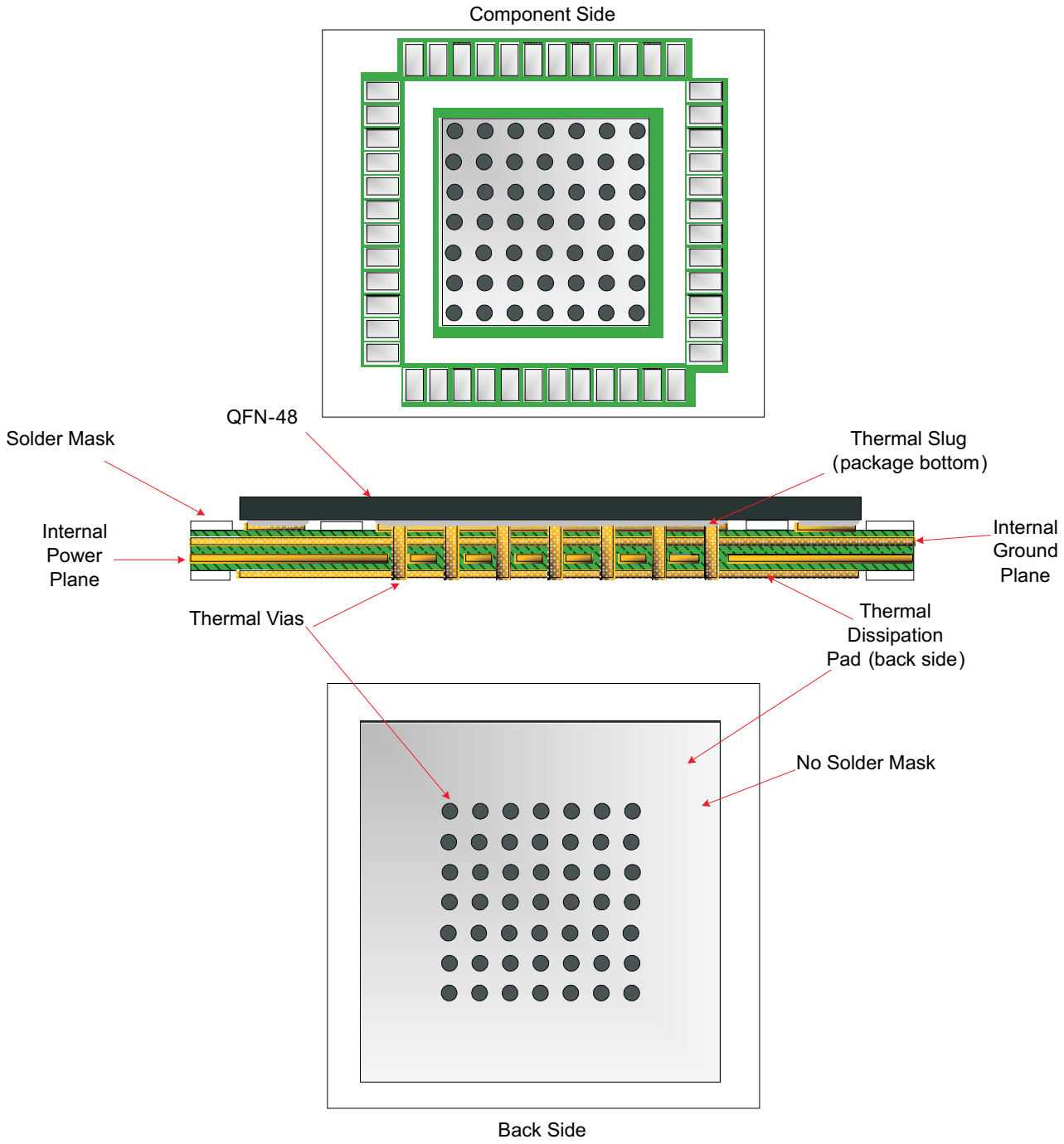


Figure 28. CDCE18005 Recommended PCB Layout

CDCE18005 Power Supply Bypassing – Recommended Layout

Figure 29 shows two conceptual layouts detailing recommended placement of power supply bypass capacitors. If the capacitors are mounted on the back side, 0402 components can be employed; however, soldering to the Thermal Dissipation Pad can be difficult. For component side mounting, use 0201 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible.

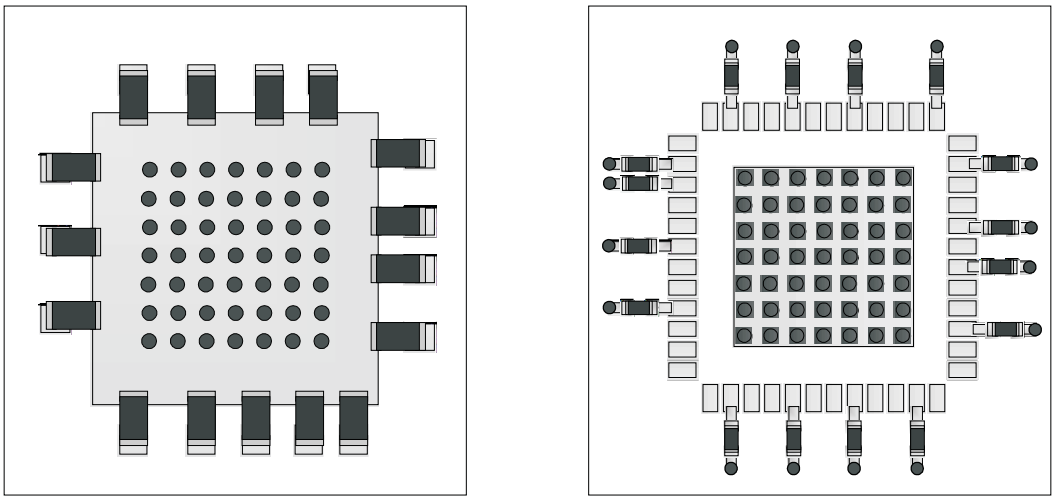


Figure 29. CDCE18005 Power Supply Bypassing

APPLICATION INFORMATION AND GENERAL USAGE HINTS

Fan-out Buffer

Each output of the CDCE18005 can be configured as a fan-out buffer (divider bypassed) or fan-out buffer with divide and skew control functionality.

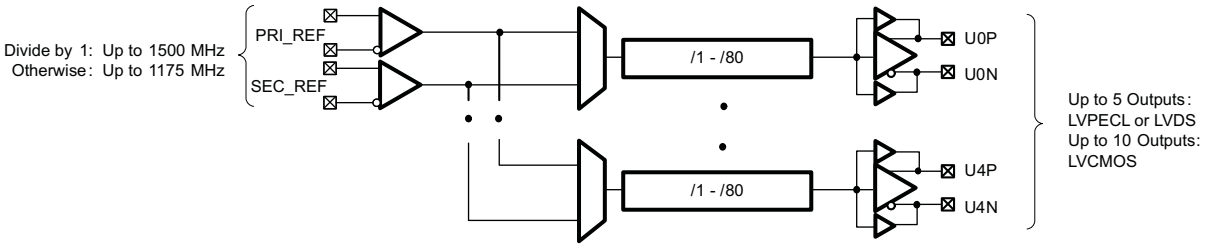


Figure 30. CDCE18005 Fan-out Buffer Mode

Clock Buffer with Crystal Input

The CDCE18005 can distribute 5–10 low noise clocks from a single crystal as follows:

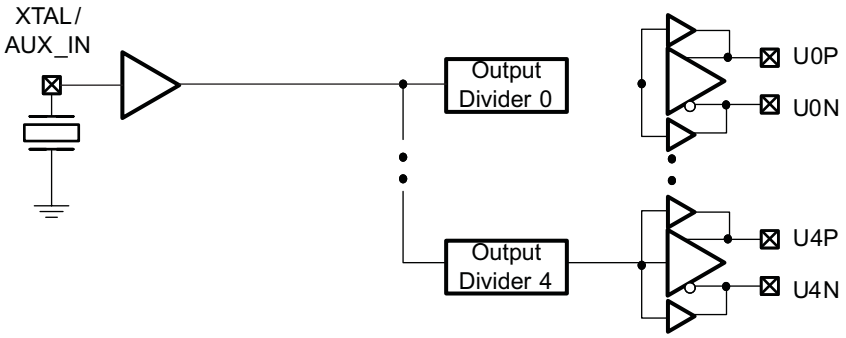


Figure 31. CDCE18005 Clock Generator Mode

Clock Distribution – Mixed Mode

The following table presents a common scenario where the CDCE18005 can function as a clock switch that accepts LVDS and crystal inputs and drives LVDS, LVPECL and LVCMOS outputs.

CLOCK FREQUENCY	INPUT/OUTPUT	FORMAT	NUMBER	CDCE18005 PORT	COMMENT
491.52 MHz	Input	LVDS	1	SEC_IN	Reference
125 MHz	Input	LVDS	1	PRI_IN	Reference from backplane
10 MHz	Input	AT-Cut	1	AUX_IN	Low end crystal oscillator
122.88 MHz	Output	LVDS	1	U0	SerDes Clock
491.52 MHz	Output	LVPECL	1	U1	ASIC
125 MHz	Output	LVPECL	1	U2	FPGA
30.72 MHz	Outputs	LVCMOS	2	U3	ASIC
10 MHz	Outputs	LVCMOS	2	U4	CPU, DSP

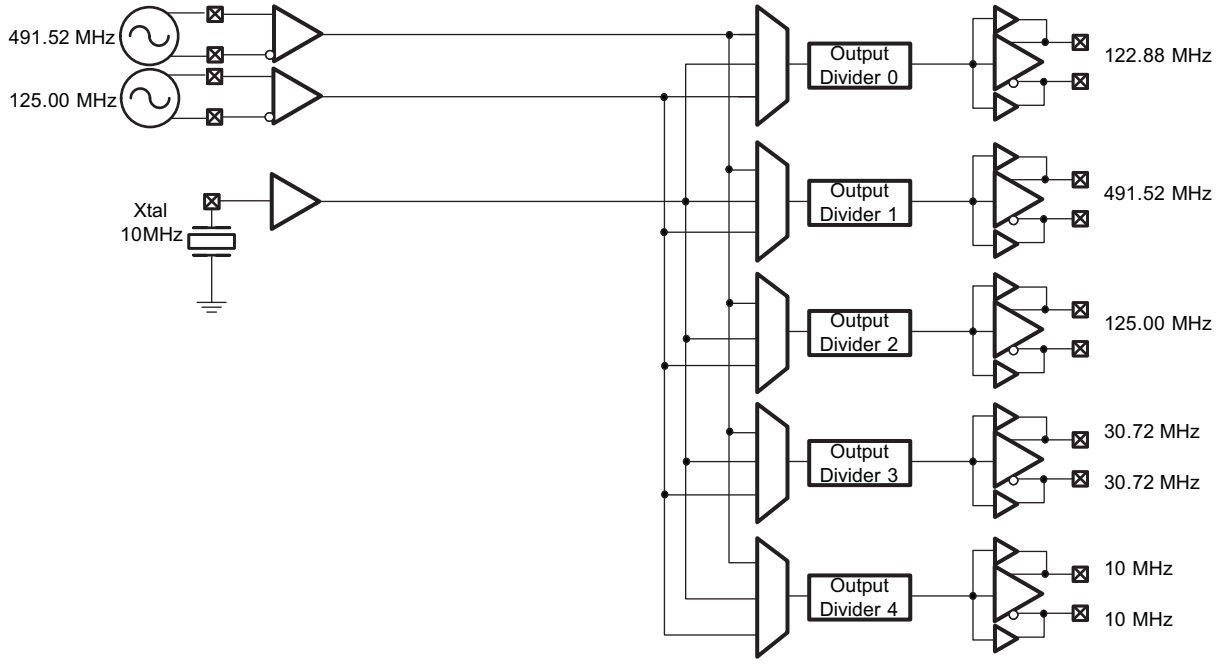


Figure 32. CDCE18005 Mixed Mode Clock Distribution Example

REVISION HISTORY

Changes from Original (November 2008) to Revision A **Page**

- Changed Title From: Five/Ten Output Clock Generator/Buffer To: Five/Ten Output Clock Programmable/Buffer 1
- Changed Flexible Inputs in the Features list 1
- Deleted Integrated EEPROM item from Features list 1
- Added the Pin Out drawing and updated the Pin Functions table 2
- Added note (1) to the Pin Functions table 3
- Added under bar in Pin Names (43, 13, 45, 46, 3 and 2) and deleted space 3
- Changed PRI_IN To PRI_REF and SEC_IN to SEC_REF in images and text throughout the data sheet 4
- Changed the ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS table 9
- Changed the TIMING REQUIREMENTS table 14
- Changed From: Jitter RMS 10k≈5MHz To: Jitter RMS 10k–20MH in Table 1 14
- Deleted the Reference 25.00 MHz column from Table 2 and changed Jitter RMS From: 10k≈20 Mhz To: 10k–5MHz. ... 14
- Deleted the SPI Control Interface Timing section 14
- Deleted Figure CDCE18005 Interface and Control block illustration 15
- Deleted Figure CDCE18005 SPI Communications Format 15
- Added new section SPI Interface Master 16
- Deleted the last row of the Register Default Setting table - (REG0008 (RAM) 19
- Deleted the first four rows of Table 5 through Table 13 - Bit Names A0, A1, A2, and A3. Added a note to Table 5 through Table 9 20
- Changed Table 12 RAM BIT 26 From: Read only; always reads "1" 27
- Changed Table 12 RAM BIT 27 From: EEPROM Status 27
- Added note to Table 13 28
- Changed Table 14 - Output Buffer coulmn From: Disbled or Enabled To: Hi-Z or From: Enable or Disabled To: Hi-Z 29
- Added Table 20 - CDCE18005 Output Divider Settings 35
- Changed Figure 25 Clock IN label From: Cloclk IN (from SMART_MUX) 36
- Changed Equation 3 36
- Added new section - Cystal Input Interface 44
- Changed Table 28 45

Changes from Revision A (June 2011) to Revision B **Page**

- Changed pin 2 From: SEC_REF+ To SEC_REF- and pin 3 From SEC_REF- To: SEC_REF+ 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCE18005RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCE 18005	Samples
CDCE18005RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCE 18005	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

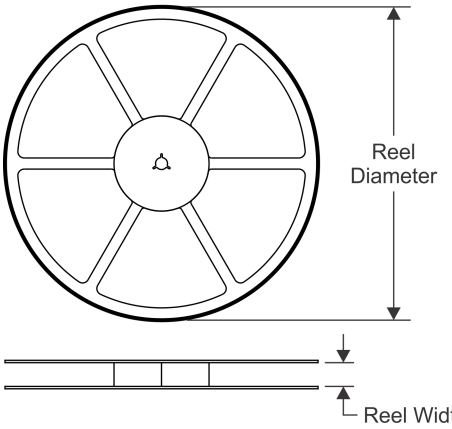
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

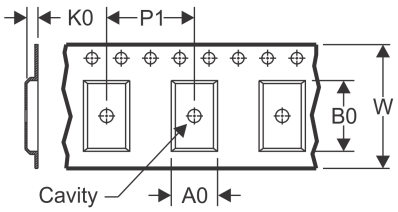
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

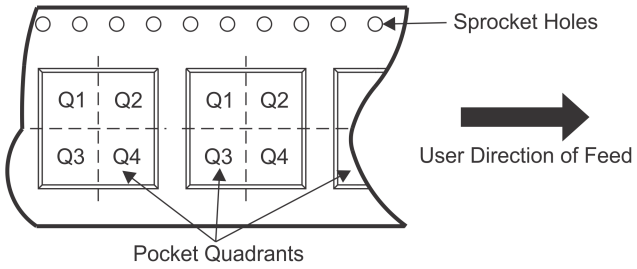


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

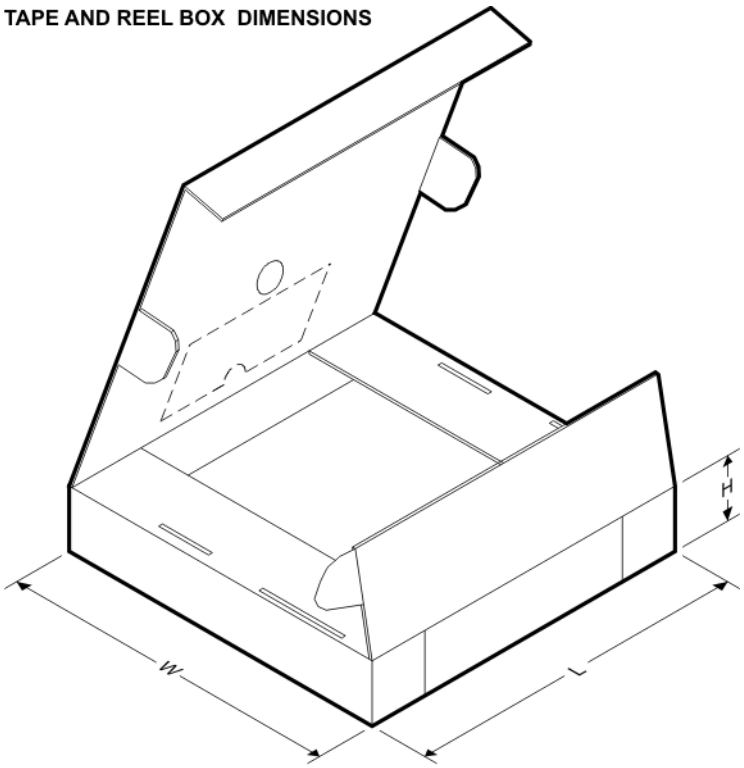
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE18005RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CDCE18005RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE18005RGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
CDCE18005RGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

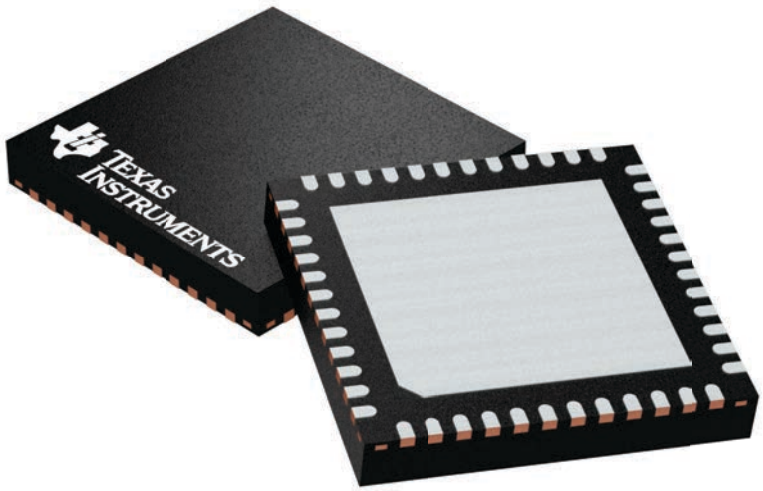
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

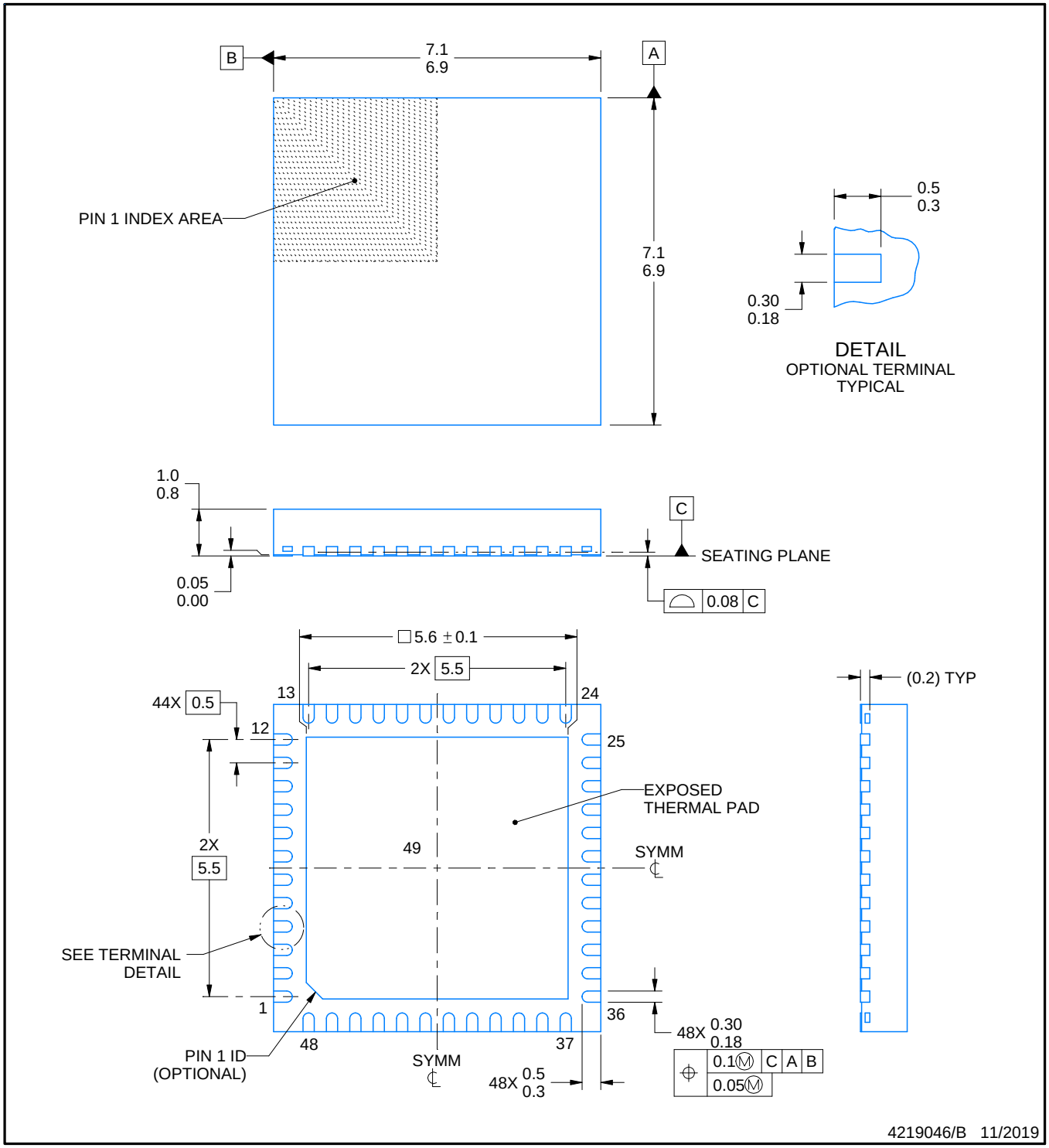
4224671/A

PACKAGE OUTLINE

RGZ0048D

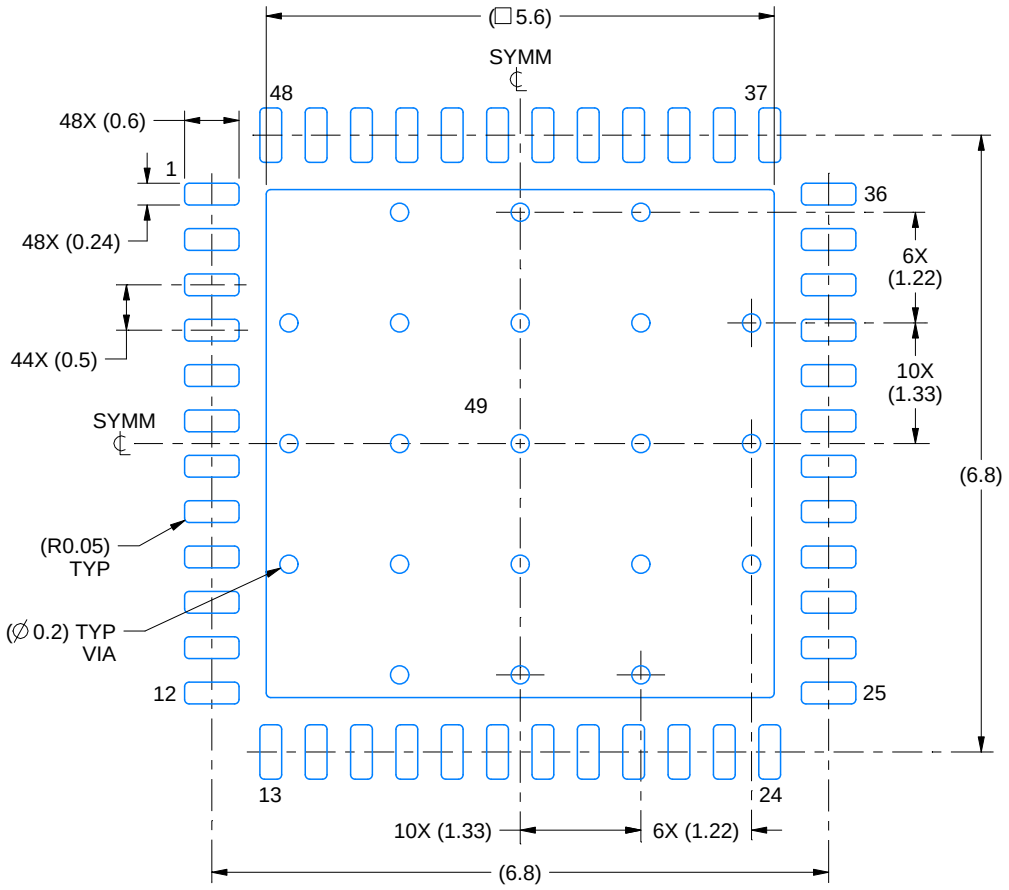
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

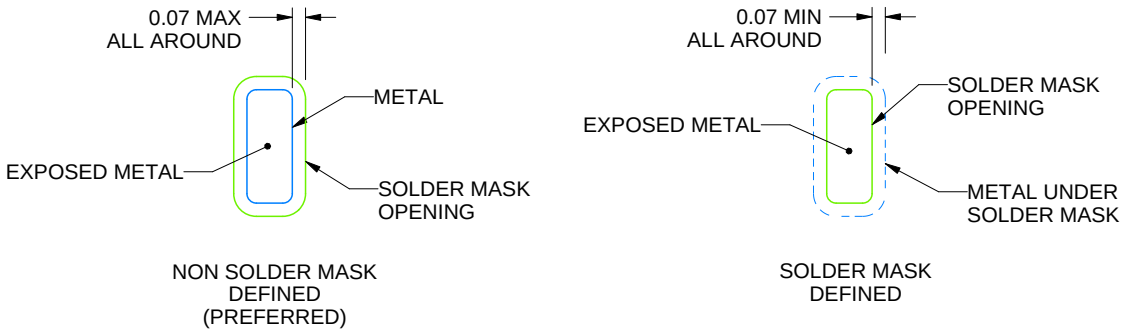


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

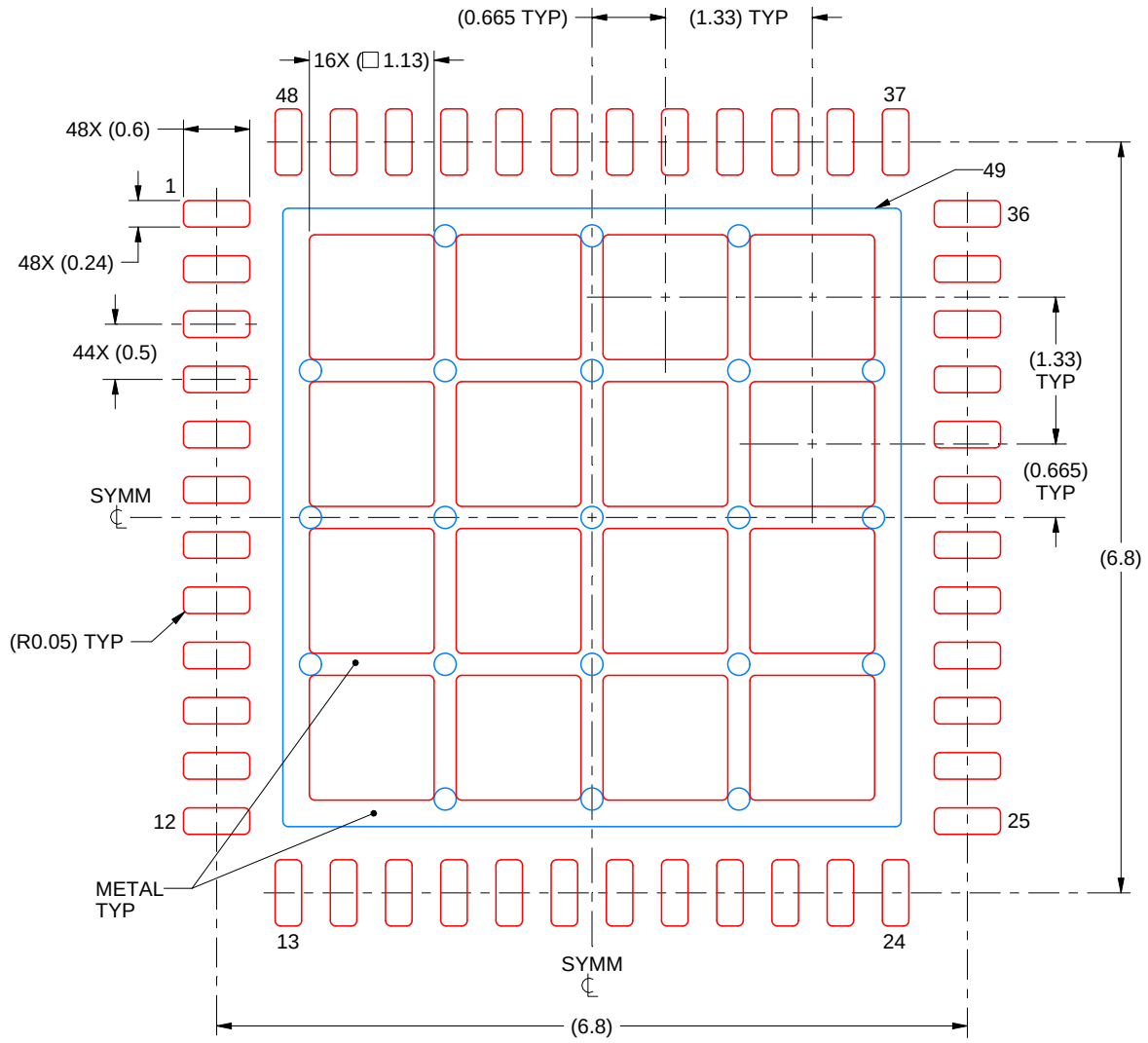


SOLDER MASK DETAILS

4219046/B 11/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4219046/B 11/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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