Data Sheet | September 15, 2008 | FN7186.5

12MHz Rail-to-Rail Input-Output Op Amps

The EL5120, EL5220, and EL5420 are low power, high voltage, rail-to-rail input-output amplifiers. The EL5120 contains a single amplifier, the EL5220 contains two amplifiers, and the EL5420 contains four amplifiers. Operating on supplies ranging from 5V to 15V, while consuming only 500µA per amplifier, the EL5120, EL5220, and EL5420 have a bandwidth of 12MHz (-3dB). They also provide common mode input ability beyond the supply rails, as well as rail-to-rail output capability. This enables these amplifiers to offer maximum dynamic range at any supply voltage.

The EL5120, EL5220, and EL5420 also feature fast slewing and settling times, as well as a high output drive capability of 30mA (sink and source). These features make these amplifiers ideal for use as voltage reference buffers in Thin Film Transistor Liquid Crystal Displays (TFT-LCD). Other applications include battery power, portable devices, and anywhere low power consumption is important.

The EL5420 is available in the space-saving 14 Ld TSSOP package, the industry-standard 14 Ld SOIC package, as well as the 16 Ld QFN package. The EL5220 is available in the 8 Ld MSOP package and the 8Ld DFN package. The EL5120 is available in the 5 Ld TSOT and 8 Ld HMSOP packages. All feature a standard operational amplifier pin out. These amplifiers are specified for operation over the full -40°C to +85°C temperature range.

Features

- 12MHz -3dB bandwidth
- Supply voltage = 4.5V to 16.5V
- Low supply current (per amplifier) = 500µA
- High slew rate = 10V/µs
- Unity-gain stable
- Beyond the rails input capability
- Rail-to-rail output swing
- Ultra-small package
- Pb-free available (RoHS compliant)

Applications

- TFT-LCD drive circuits
- Electronics notebooks
- Electronics games
- Touch-screen displays
- Personal communication devices
- Personal digital assistants (PDA)
- Portable instrumentation
- Sampling ADC amplifiers
- Wireless LANs
- Office automation
- Active filters
- ADC/DAC buffer

Ordering Information

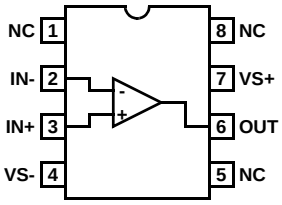
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
EL5120IWT-T7 (Note 1)	K	-40 to +85	5 Ld TSOT Tape and Reel	MDP0049
EL5120IWT-T7A (Note 1)	K	-40 to +85	5 Ld TSOT Tape and Reel	MDP0049
EL5120IWTZ-T7 (Notes 1, 2)	BKAA	-40 to +85	5 Ld TSOT Tape and Reel (Pb-free)	MDP0049
EL5120IWTZ-T7A (Notes 1, 2)	BKAA	-40 to +85	5 Ld TSOT Tape and Reel (Pb-free)	MDP0049
EL5120IYE	8	-40 to +85	8 Ld HMSOP	MDP0050
EL5120IYE-T7	8	-40 to +85	8 Ld HMSOP Tape and Reel	MDP0050
EL5120IYE-T13	8	-40 to +85	8 Ld HMSOP Tape and Reel	MDP0050
EL5120IYEZ (Note 2)	BACAA	-40 to +85	8 Ld HMSOP (Pb-free)	MDP0050
EL5120IYEZ-T7 (Notes 1, 2)	BACAA	-40 to +85	8 Ld HMSOP Tape and Reel (Pb-free)	MDP0050
EL5120IYEZ-T13 (Notes 1, 2)	BACAA	-40 to +85	8 Ld HMSOP Tape and Reel (Pb-free)	MDP0050
EL5220ILZ-T13 (Notes 1, 2)	20Z	-40 to +85	8 Ld DFN Tape and Reel (Pb-free)	L8.2x3
EL5220CY	D	0 to +70	8 Ld MSOP	MDP0043
EL5220CY-T7	D	0 to +70	8 Ld MSOP Tape and Reel	MDP0043
EL5220CY-13	D	0 to +70	8 Ld MSOP Tape and Reel	MDP0043
EL5220CYZ (Note 2)	BBAAA	0 to +70	8 Ld MSOP (Pb-free)	MDP0043
EL5220CYZ-T7 (Notes 1, 2)	BBAAA	0 to +70	8 Ld MSOP Tape and Reel (Pb-free)	MDP0043
EL5220CYZ-T13 (Notes 1, 2)	BBAAA	0 to +70	8 Ld MSOP Tape and Reel (Pb-free)	MDP0043
EL5420CL	5420CL	0 to +70	16 Ld QFN	MDP0046
EL5420CL-T7	5420CL	0 to +70	16 Ld QFN Tape and Reel	MDP0046
EL5420CL-T13	5420CL	0 to +70	16 Ld QFN Tape and Reel	MDP0046
EL5420CLZ (Note 2)	5420CLZ	0 to +70	16 Ld QFN (Pb-free)	MDP0046
EL5420CLZ-T7 (Notes 1, 2)	5420CLZ	0 to +70	16 Ld QFN Tape and Reel (Pb-free)	MDP0046
EL5420CLZ-T13 (Notes 1, 2)	5420CLZ	0 to +70	16 Ld QFN Tape and Reel (Pb-free)	MDP0046
EL5420CS	5420CS	0 to +70	14 Ld SOIC	MDP0027
EL5420CS-T7	5420CS	0 to +70	14 Ld SOIC Tape and Reel	MDP0027
EL5420CS-T13	5420CS	0 to +70	14 Ld SOIC Tape and Reel	MDP0027
EL5420CSZ (Note 2)	5420CSZ	0 to +70	14 Ld SOIC (Pb-free)	MDP0027
EL5420CSZ-T7 (Notes 1, 2)	5420CSZ	0 to +70	14 Ld SOIC Tape and Reel (Pb-free)	MDP0027
EL5420CSZ-T13 (Notes 1, 2)	5420CSZ	0 to +70	14 Ld SOIC Tape and Reel (Pb-free)	MDP0027
EL5420CR	5420CR	0 to +70	14 Ld TSSOP	MDP0044
EL5420CR-T7	5420CR	0 to +70	14 Ld TSSOP Tape and Reel	MDP0044
EL5420CR-T13	5420CR	0 to +70	14 Ld TSSOP Tape and Reel	MDP0044
EL5420CRZ (Note 2)	5420CRZ	0 to +70	14 Ld TSSOP (Pb-free)	M14.173
EL5420CRZ-T7 (Notes 1, 2)	5420CRZ	0 to +70	14 Ld TSSOP Tape and Reel (Pb-free)	M14.173
EL5420CRZ-T13 (Notes 1, 2)	5420CRZ	0 to +70	14 Ld TSSOP Tape and Reel (Pb-free)	M14.173

NOTES:

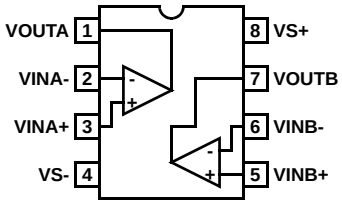
1. Please refer to TB347 for details on reel specifications.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

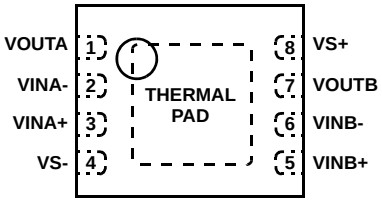
EL5120
(8 LD HMSOP)
TOP VIEW



EL5220
(8 LD MSOP)
TOP VIEW

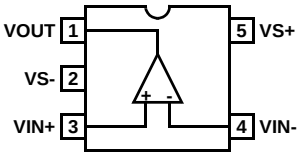


EL5220
(8 LD DFN)
TOP VIEW

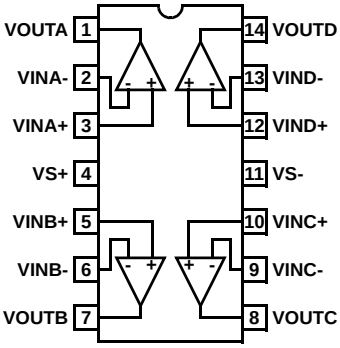


THERMAL PAD
CONNECTS TO VS-

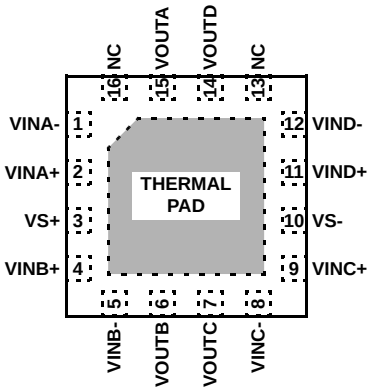
EL5120
(5 LD TSOT)
TOP VIEW



EL5420
(14 LD TSSOP, SOIC)
TOP VIEW



EL5420
(16 LD QFN)
TOP VIEW



THERMAL PAD
CONNECTS TO VS-

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- . . . . . .+18V
Input Voltage . . . . . V_S- - 0.5V, V_S +0.5V
Maximum Continuous Output Current 30mA
Maximum Die Temperature . . . . . .+125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
5 Ld TSOT (Note 3)	214
8 Ld HMSOP (Note 4)	64
8 Ld DFN (Note 4)	110
8 Ld MSOP (Note 3)	115
16 Ld QFN (Note 4)	44
14 Ld SOIC (Note 3)	82
14 Ld TSSOP (Note 3)	113

Storage Temperature . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Power Dissipation . . . . . See Curves
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 10kΩ and C_L = 10pF to 0V, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		2	12	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 5)		5		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
CMIR	Common-Mode Input Range		-5.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -5.5V to +5.5V	50	70		dB
A_{VOL}	Open Loop Gain	-4.5V ≤ V_{OUT} ≤ +4.5V	75	95		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		-4.92	-4.85	V
V_{OH}	Output Swing High	I_L = 5mA	4.85	4.92		V
I_{SC}	Short Circuit Current			±120		mA
I_{OUT}	Output Current			±30		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±2.25V to ±7.75V	60	80		dB
I_S	Supply Current (Per Amplifier)	No load		500	750	µA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 6)	-4.0V ≤ V_{OUT} ≤ +4.0V, 20% to 80%		10		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		500		ns
BW	-3dB Bandwidth	R_L = 10kΩ, C_L = 10pF		12		MHz
GBWP	Gain-Bandwidth Product	R_L = 10kΩ, C_L = 10pF		8		MHz

Electrical Specifications $V_S+ = +5V$, $V_S- = -5V$, $R_L = 10k\Omega$ and $C_L = 10pF$ to 0V, $T_A = +25°C$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
PM	Phase Margin	$R_L = 10k\Omega$, $C_L = 10pF$		50		°
CS	Channel Separation	f = 5MHz (EL5220 and EL5420 only)		75		dB

NOTES:

5. Measured over operating temperature range.
6. Slew rate is measured on rising and falling edges.

Electrical Specifications $V_S+ = +5V$, $V_S- = 0V$, $R_L = 10k\Omega$ and $C_L = 10pF$ to 2.5V, $T_A = +25°C$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 2.5V$		2	10	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 7)		5		µV/°C
I_B	Input Bias Current	$V_{CM} = 2.5V$		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
CMIR	Common-Mode Input Range		-0.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.5V to +5.5V	45	66		dB
A_{VOL}	Open Loop Gain	$0.5V \le V_{OUT} \le +4.5V$	75	95		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -5mA$		80	150	mV
V_{OH}	Output Swing High	$I_L = +5mA$	4.85	4.92		V
I_{SC}	Short Circuit Current			±120		mA
I_{OUT}	Output Current			±30		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current (Per Amplifier)	No load		500	750	µA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 8)	$1V \le V_{OUT} \le 4V$, 20% to 80%		10		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 10pF$		12		MHz
GBWP	Gain-Bandwidth Product	$R_L = 10k\Omega$, $C_L = 10pF$		8		MHz
PM	Phase Margin	$R_L = 10k\Omega$, $C_L = 10pF$		50		°
CS	Channel Separation	f = 5MHz (EL5220 and EL5420 only)		75		dB

NOTES:

7. Measured over operating temperature range.
8. Slew rate is measured on rising and falling edges.

Electrical Specifications $V_S+ = +15V$, $V_S- = 0V$, $R_L = 10k\Omega$ and $C_L = 10pF$ to 7.5V, $T_A = +25°C$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 7.5V$		2	14	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 9)		5		µV/°C
I_B	Input Bias Current	$V_{CM} = 7.5V$		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
CMIR	Common-Mode Input Range		-0.5		+15.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.5V to +15.5V	53	72		dB
A_{VOL}	Open Loop Gain	$0.5V \le V_{OUT} \le 14.5V$	75	95		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -5mA$		80	150	mV
V_{OH}	Output Swing High	$I_L = +5mA$	14.85	14.92		V
I_{SC}	Short Circuit Current			±120		mA
I_{OUT}	Output Current			±30		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current (Per Amplifier)	No load		500	750	µA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 10)	$1V \le V_{OUT} \le 14V$, 20% to 80%		10		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 10pF$		12		MHz
GBWP	Gain-Bandwidth Product	$R_L = 10k\Omega$, $C_L = 10pF$		8		MHz
PM	Phase Margin	$R_L = 10k\Omega$, $C_L = 10pF$		50		°
CS	Channel Separation	f = 5MHz (EL5220 and EL5420 only)		75		dB

NOTES:

9. Measured over operating temperature range

10. Slew rate is measured on rising and falling edges

Typical Performance Curves

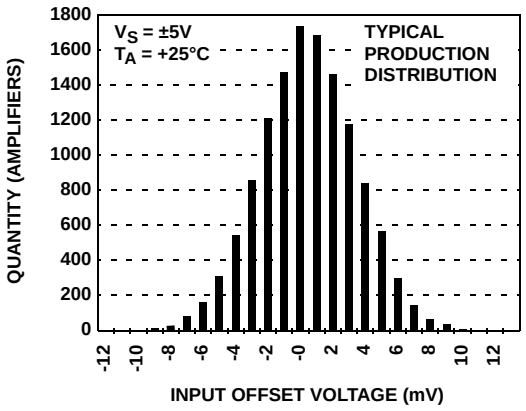


FIGURE 1. EL5420 INPUT OFFSET VOLTAGE DISTRIBUTION

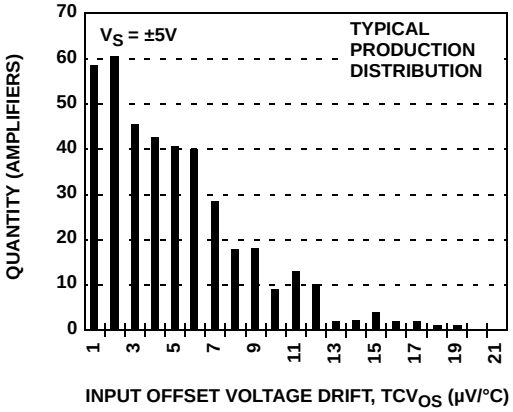


FIGURE 2. EL5420 INPUT OFFSET VOLTAGE DRIFT

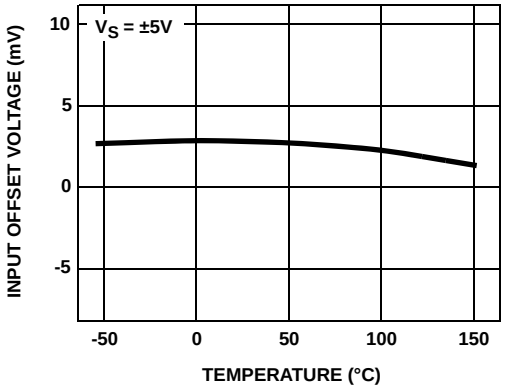


FIGURE 3. INPUT OFFSET VOLTAGE vs TEMPERATURE

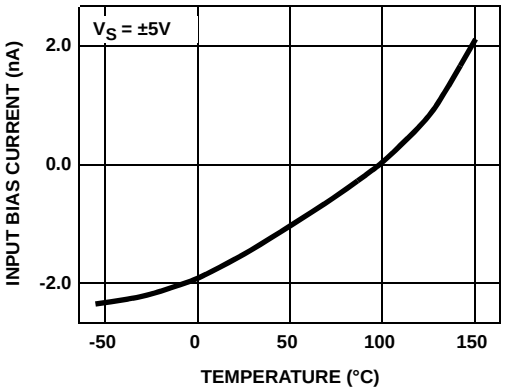


FIGURE 4. INPUT BIAS CURRENT vs TEMPERATURE

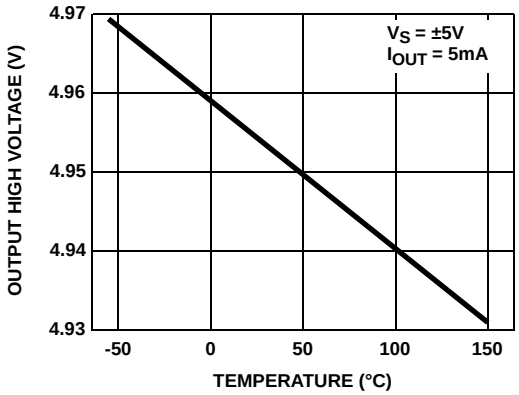


FIGURE 5. OUTPUT HIGH VOLTAGE vs TEMPERATURE

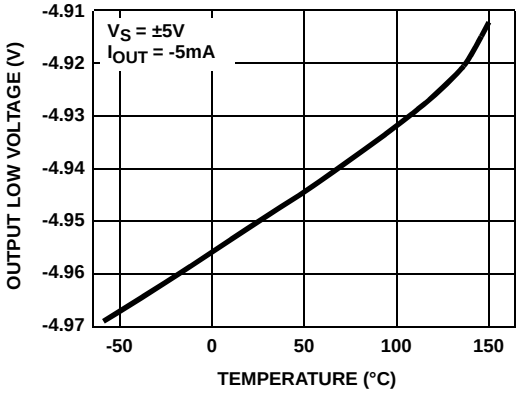


FIGURE 6. OUTPUT LOW VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

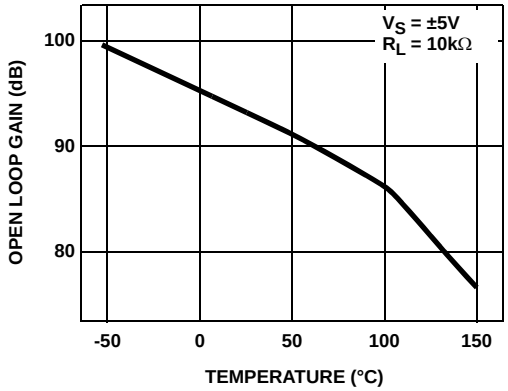


FIGURE 7. OPEN LOOP GAIN vs TEMPERATURE

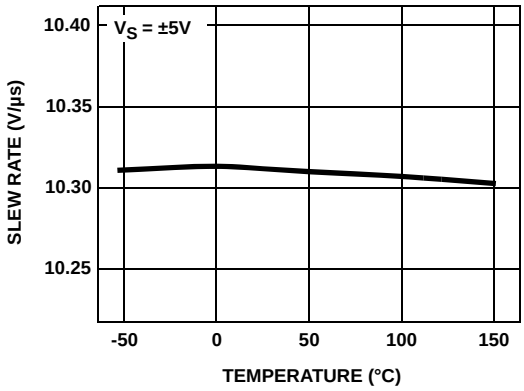


FIGURE 8. SLEW RATE vs TEMPERATURE

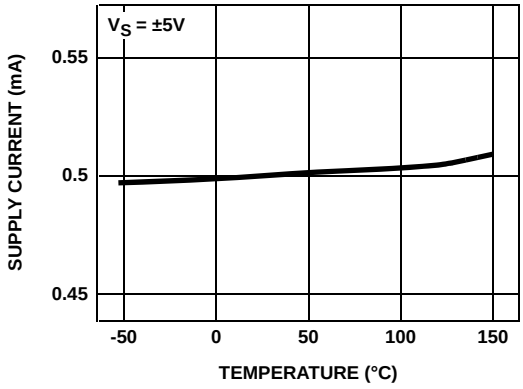


FIGURE 9. EL5420 SUPPLY CURRENT PER AMPLIFIER vs TEMPERATURE

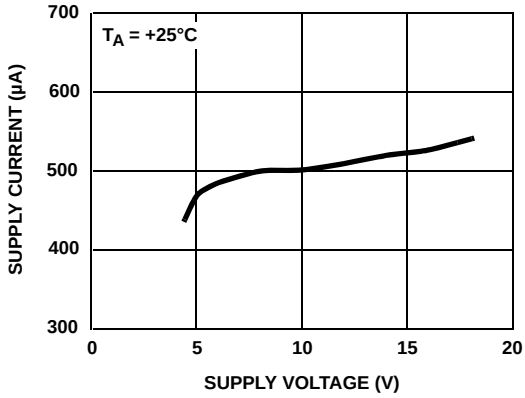


FIGURE 10. EL5420 SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

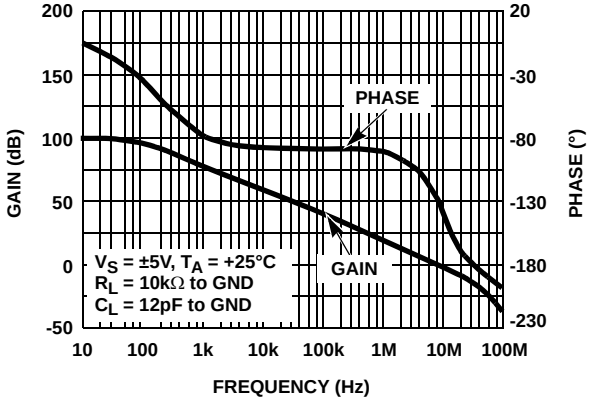


FIGURE 11. OPEN LOOP GAIN AND PHASE vs FREQUENCY

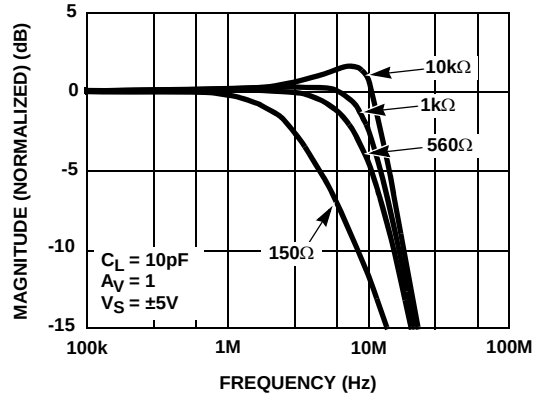


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS R_L

Typical Performance Curves (Continued)

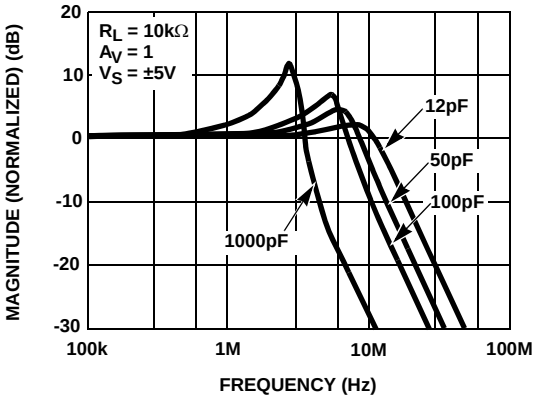


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS C_L

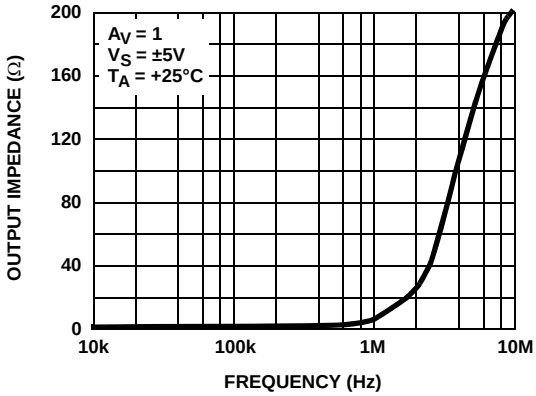


FIGURE 14. CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

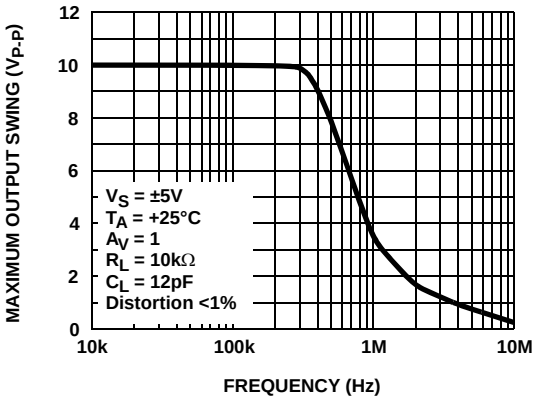


FIGURE 15. MAXIMUM OUTPUT SWING vs FREQUENCY

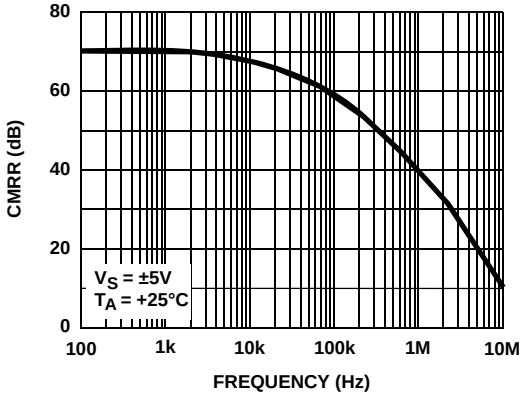


FIGURE 16. CMRR vs FREQUENCY

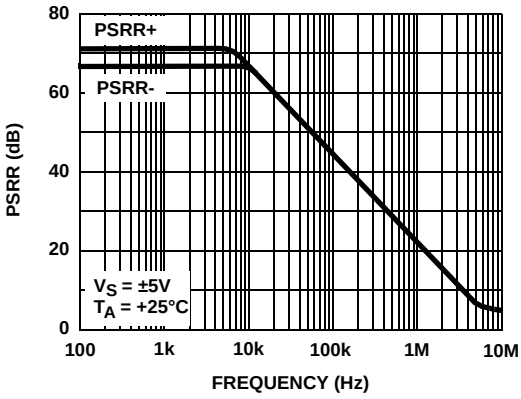


FIGURE 17. PSRR vs FREQUENCY

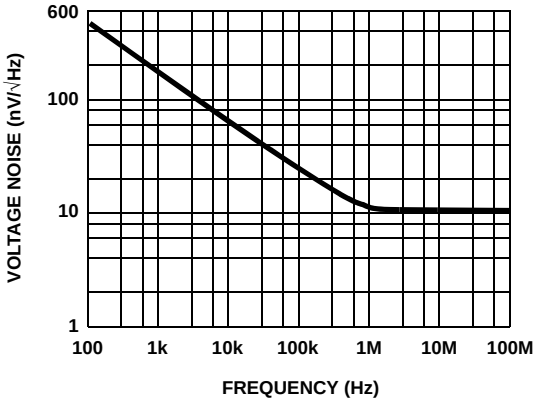


FIGURE 18. INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

Typical Performance Curves (Continued)

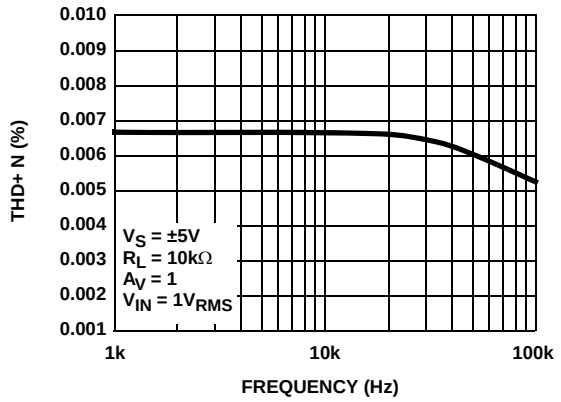


FIGURE 19. TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

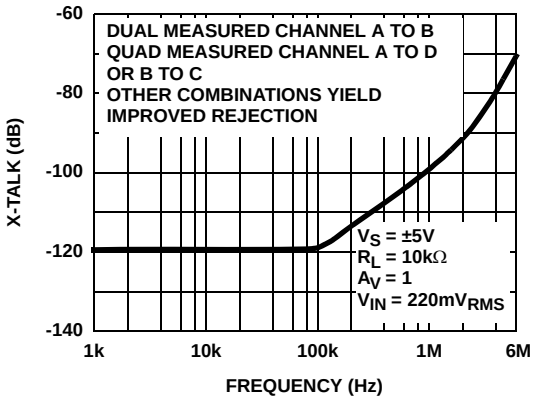


FIGURE 20. CHANNEL SEPARATION vs FREQUENCY RESPONSE

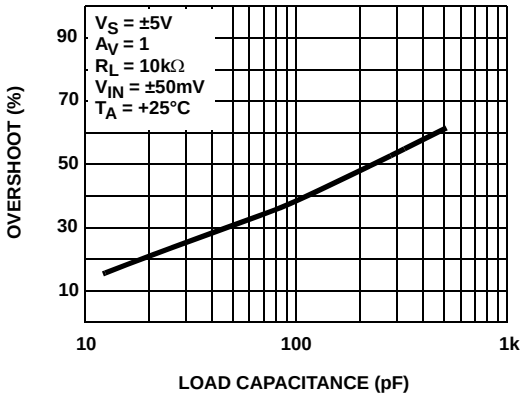


FIGURE 21. SMALL SIGNAL OVERSHOOT vs LOAD CAPACITANCE

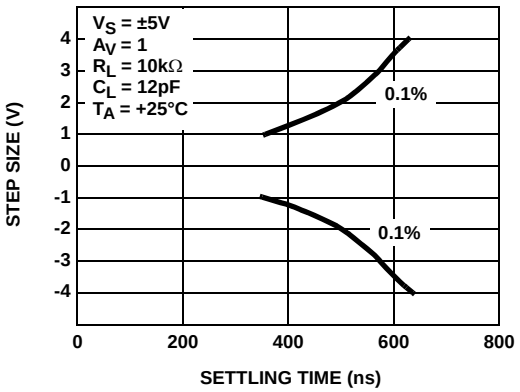


FIGURE 22. SETTLING TIME vs STEP SIZE

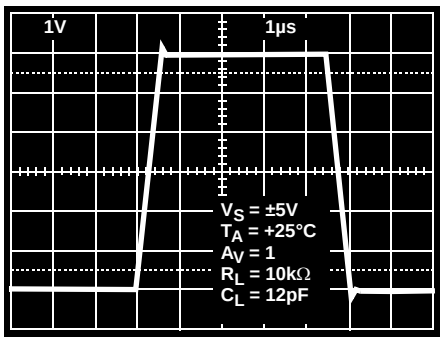


FIGURE 23. LARGE SIGNAL TRANSIENT RESPONSE

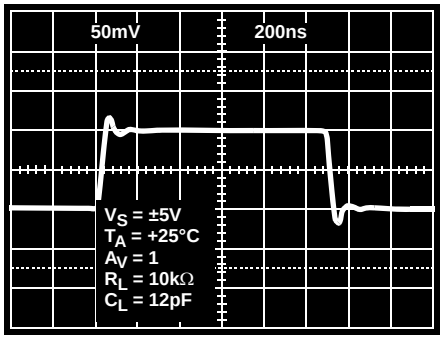
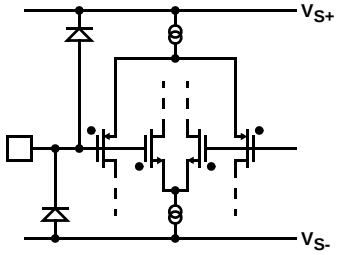


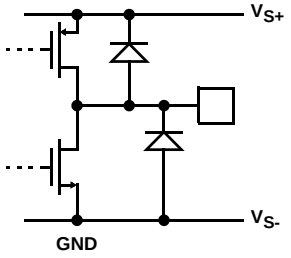
FIGURE 24. SMALL SIGNAL TRANSIENT RESPONSE

Pin Descriptions

EL5120		EL5220	EL5420				
5 LD TSOT	8 LD HMSOP	8 LD MSOP, 8 LD DFN	14 LD TSSOP, 14 LD SOIC	16 LD QFN	PIN NAME	PIN FUNCTION	EQUIVALENT CIRCUIT
	1, 5, 8			13, 16	NC	No Connect	
	3				IN+	Amplifier Non-Inverting Input	(Reference Circuit 1)
	2				IN-	Amplifier Inverting Input	(Reference Circuit 1)
	6				OUT	Amplifier Output	(Reference Circuit 2)
3					VIN+	Amplifier Non-Inverting Input	(Reference Circuit 1)
4					VIN-	Amplifier Inverting Input	(Reference Circuit 1)
1					VOUT	Amplifier Output	(Reference Circuit 2)
		1	1	15	VOUTA	Amplifier A Output	(Reference Circuit 2)
		2	2	1	VINA-	Amplifier A Inverting Input	(Reference Circuit 1)
		3	3	2	VINA+	Amplifier A Non-Inverting Input	(Reference Circuit 1)
5	7	8	4	3	VS+	Positive Power Supply	
		5	5	4	VINB+	Amplifier B Non-Inverting Input	(Reference Circuit 1)
		6	6	5	VINB-	Amplifier B Inverting Input	(Reference Circuit 1)
		7	7	6	VOUTB	Amplifier B Output	(Reference Circuit 2)
			8	7	VOUTC	Amplifier C Output	(Reference Circuit 2)
			9	8	VINC-	Amplifier C Inverting Input	(Reference Circuit 1)
			10	9	VINC+	Amplifier C Non-Inverting Input	(Reference Circuit 1)
2	4	4	11	10	VS-	Negative Power Supply	
			12	11	VIND+	Amplifier D Non-Inverting Input	(Reference Circuit 1)
			13	12	VIND-	Amplifier D Inverting Input	(Reference Circuit 1)
			14	14	VOUTD	Amplifier D Output	(Reference Circuit 2)



Circuit 1



Circuit 2

Applications Information

Product Description

The EL5120, EL5220, and EL5420 voltage feedback amplifiers are fabricated using a high voltage CMOS process. They exhibit rail-to-rail input and output capability, they are unity gain stable, and have low power consumption (500µA per amplifier). These features make the EL5120, EL5220, and EL5420 ideal for a wide range of general-purpose applications. Connected in voltage follower mode and driving a load of 10kΩ and 12pF, the EL5120, EL5220, and EL5420 have a -3dB bandwidth of 12MHz while maintaining a 10V/µs slew rate. The EL5120 is a single amplifier, the EL5220 is a dual amplifier, and the EL5420 is a quad amplifier.

Operating Voltage, Input, and Output

The EL5120, EL5220, and EL5420 are specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range of 4.5V to 16.5V. Most EL5120, EL5220, and EL5420 specifications are stable over both the full supply range and operating temperatures of -40°C to +85°C. Parameter variations with operating voltage and/or temperature are shown in the typical performance curves.

The input common-mode voltage range of the EL5120, EL5220, and EL5420 extends 500mV beyond the supply rails. The output swings of the EL5120, EL5220, and EL5420 typically extend to within 80mV of positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 25 shows the input and output waveforms for the device in the unity-gain configuration. Operation is from ±5V supply with a 10kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid. The output voltage is approximately $9.985V_{P-P}$.

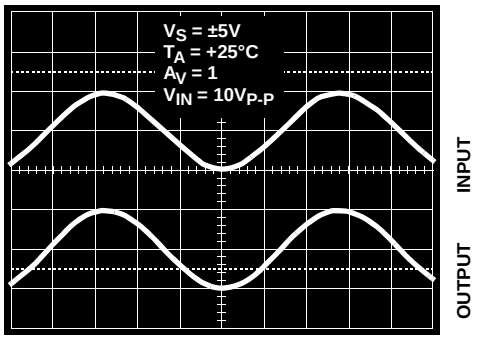


FIGURE 25. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Short Circuit Current Limit

The EL5120, EL5220, and EL5420 will limit the short circuit current to ±120mA if the output is directly shorted to the positive or the negative supply. If an output is shorted indefinitely, the power dissipation could easily increase such that the device may be damaged. Maximum reliability is maintained if the output continuous current never exceeds ±30mA. This limit is set by the design of the internal metal interconnects.

Output Phase Reversal

The EL5120, EL5220, and EL5420 are immune to phase reversal as long as the input voltage is limited from (V_S-) -0.5V to (V_S+) +0.5V. Figure 26 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and overvoltage damage could occur.

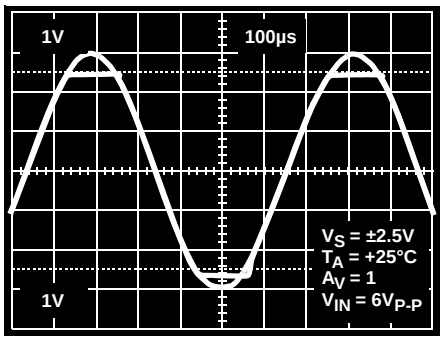


FIGURE 26. OPERATION WITH BEYOND-THE-RAILS INPUT

Power Dissipation

With the high-output drive capability of the EL5120, EL5220, and EL5420 amplifiers, it is possible to exceed the 125°C “absolute-maximum junction temperature” under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 1)}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i \times [V_S \times I_{SMAX} + (V_S + - V_{OUT}i) \times I_{LOAD}i] \quad \text{(EQ. 2)}$$

when sourcing, and:

$$P_{DMAX} = \Sigma i \times [V_S \times I_{SMAX} + (V_{OUT}i - V_S) \times I_{LOAD}i] \quad \text{(EQ. 3)}$$

when sinking.

where:

- i = 1 to 2 for dual and 1 to 4 for quad
- V_S = Total supply voltage
- I_{SMAX} = Maximum supply current per amplifier
- $V_{OUT}i$ = Maximum output voltage of the application
- $I_{LOAD}i$ = Load current

If we set the two P_{DMAX} equations equal to each other, we can solve for $R_{LOAD}i$ to avoid device overheat. Figures 27 and 28 provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves. To ensure proper operation, it is important to observe the recommended derating curves in Figures 27 and 28.

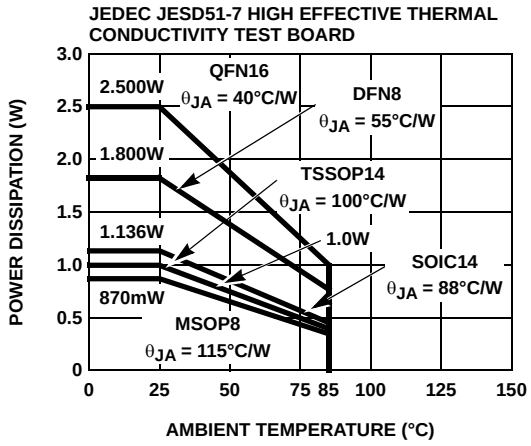


FIGURE 27. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

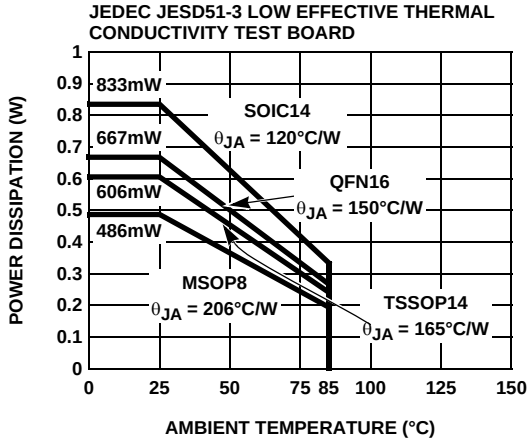


FIGURE 28. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Unused Amplifiers

It is recommended that any unused amplifiers in a dual and a quad package be configured as a unity gain follower. The inverting input should be directly connected to the output and the non-inverting input tied to the ground plane.

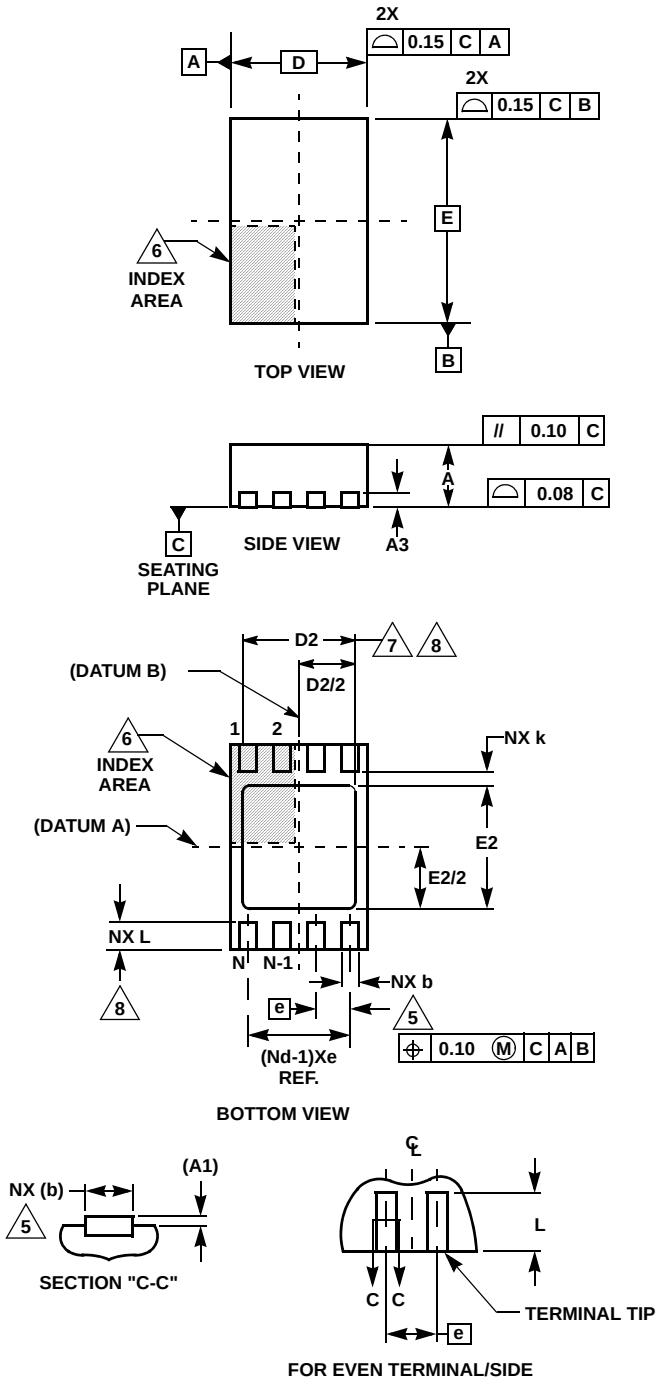
Driving Capacitive Loads

The EL5120, EL5220, and EL5420 can drive a wide range of capacitive loads. As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking will increase. The amplifiers drive 10pF loads in parallel with 10kΩ with just 1.5dB of peaking, and 100pF with 6.4dB of peaking. If less peaking is desired in these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output. However, this will obviously reduce the gain slightly. Another method of reducing peaking is to add a “snubber” circuit at the output. A snubber is a shunt load consisting of a resistor in series with a capacitor. Values of 150Ω and 10nF are typical. The advantage of a snubber is that it does not draw any DC load current or reduce the gain

Power Supply Bypassing and Printed Circuit Board Layout

The EL5120, EL5220, and EL5420 can provide gain at high frequency. As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the VS- pin is connected to ground, a 0.1µF ceramic capacitor should be placed from VS+ to pin to VS- pin. A 4.7µF tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

Dual Flat No-Lead Plastic Package (DFN)



L8.2x3

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

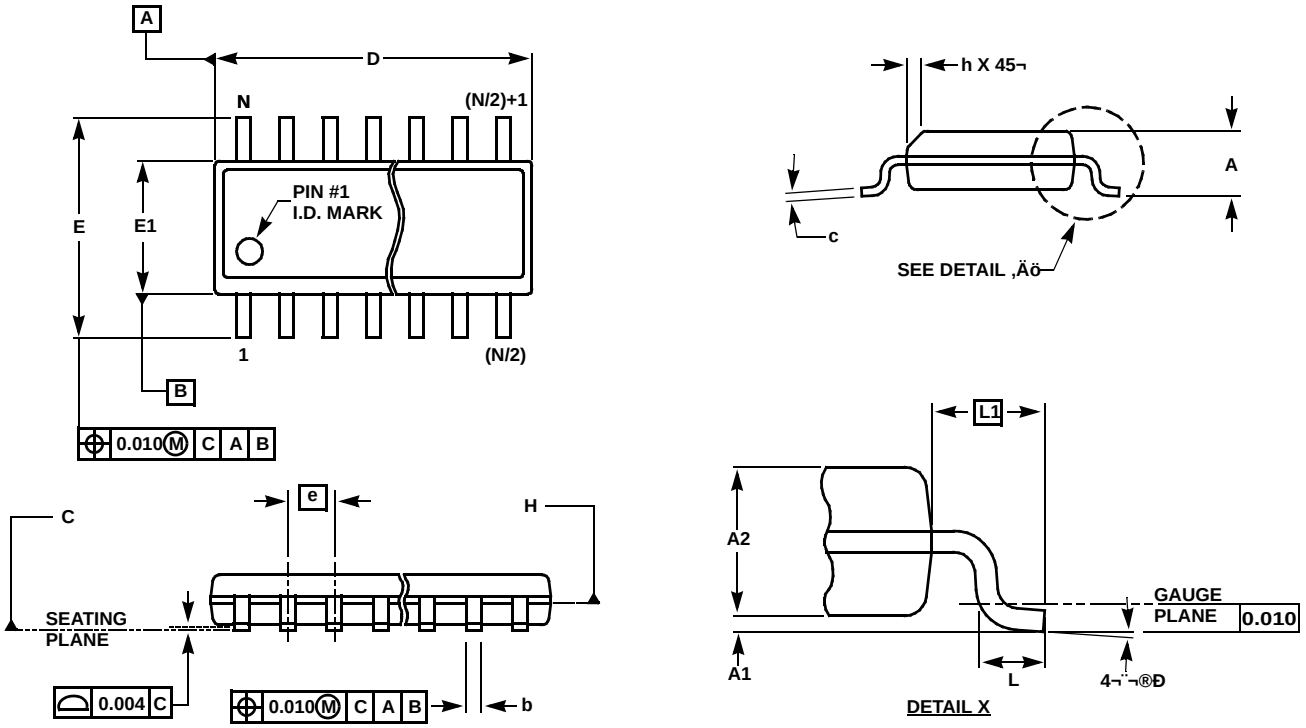
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.32	5,8
D		2.00 BSC		-
D2	1.50	1.65	1.75	7,8
E		3.00 BSC		-
E2	1.65	1.80	1.90	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		8		2
Nd		4		3

Rev. 0 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

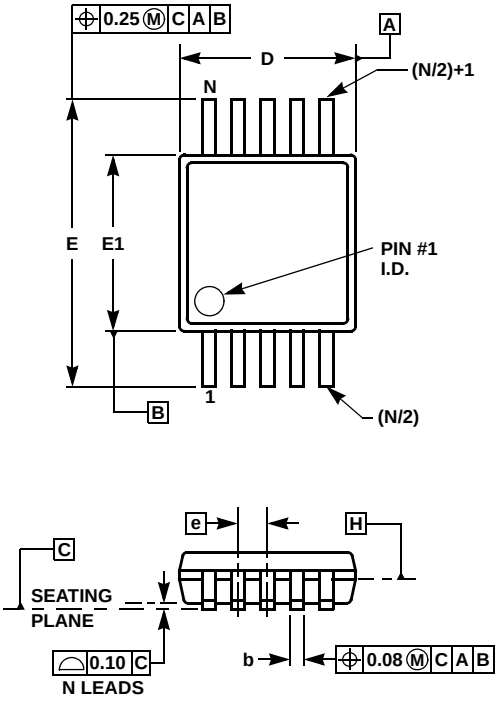
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

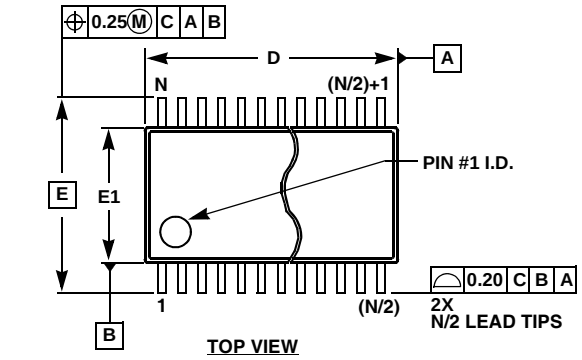
SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

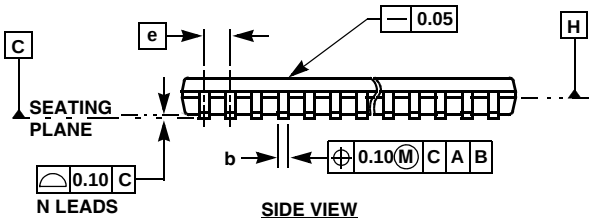
NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

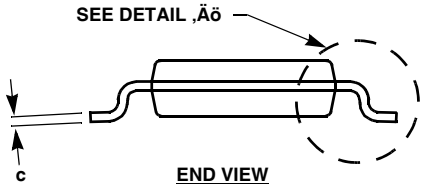
Thin Shrink Small Outline Package Family (TSSOP)



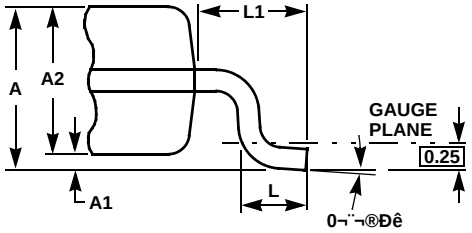
TOP VIEW



SIDE VIEW



END VIEW



DETAIL X

MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

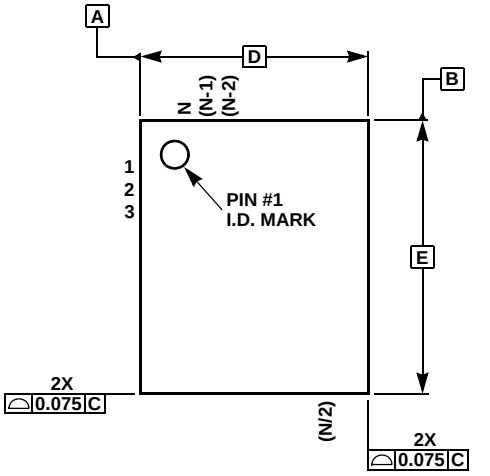
SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

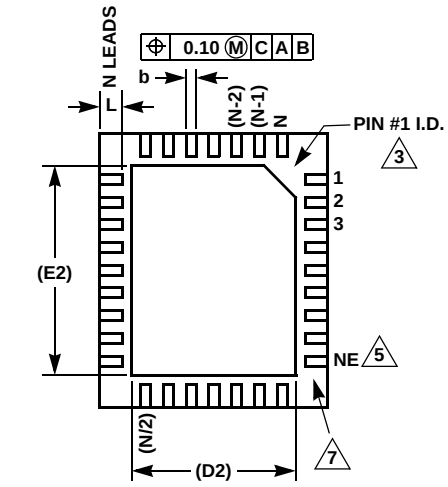
NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions “D” and “E1” are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

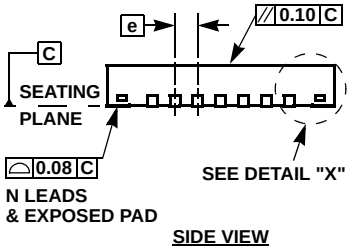
QFN (Quad Flat No-Lead) Package Family



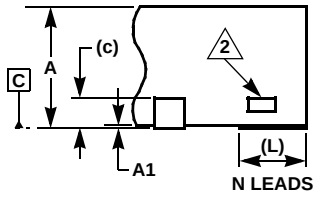
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL X

MDP0046

QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY (COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS				TOLERANCE	NOTES
	QFN44	QFN3	QFN32			
A	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.23	0.22	±0.02	-
c	0.20	0.20	0.20	0.20	Reference	-
D	7.00	5.00	8.00	5.00	Basic	-
D2	5.10	3.80	5.80	3.60/2.48	Reference	8
E	7.00	7.00	8.00	6.00	Basic	-
E2	5.10	5.80	5.80	4.60/3.40	Reference	8
e	0.50	0.50	0.80	0.50	Basic	-
L	0.55	0.40	0.53	0.50	±0.05	-
N	44	38	32	32	Reference	4
ND	11	7	8	7	Reference	6
NE	11	12	8	9	Reference	5

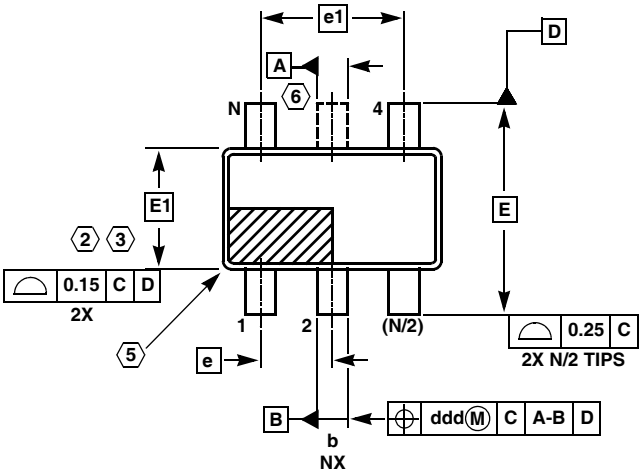
SYMBOL	MILLIMETERS					TOLERANCE	NOTES
	QFN28	QFN2	QFN20		QFN16		
A	0.90	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	0.02	+0.03/ -0.02	-
b	0.25	0.25	0.30	0.25	0.33	±0.02	-
c	0.20	0.20	0.20	0.20	0.20	Reference	-
D	4.00	4.00	5.00	4.00	4.00	Basic	-
D2	2.65	2.80	3.70	2.70	2.40	Reference	-
E	5.00	5.00	5.00	4.00	4.00	Basic	-
E2	3.65	3.80	3.70	2.70	2.40	Reference	-
e	0.50	0.50	0.65	0.50	0.65	Basic	-
L	0.40	0.40	0.40	0.40	0.60	±0.05	-
N	28	24	20	20	16	Reference	4
ND	6	5	5	5	4	Reference	6
NE	8	7	5	5	4	Reference	5

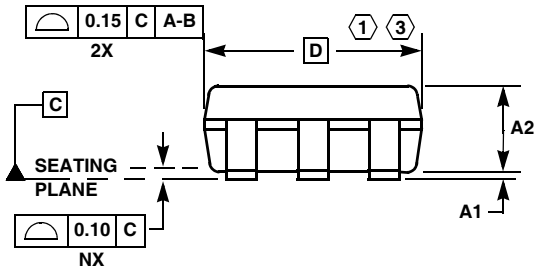
Rev 11 2/07

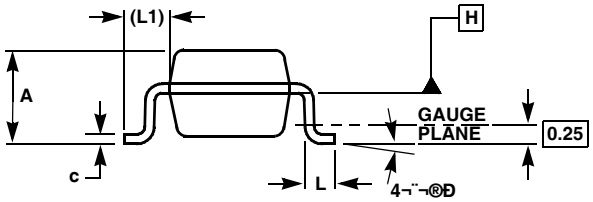
NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.

TSOT Package Family







MDP0049

TSOT PACKAGE FAMILY

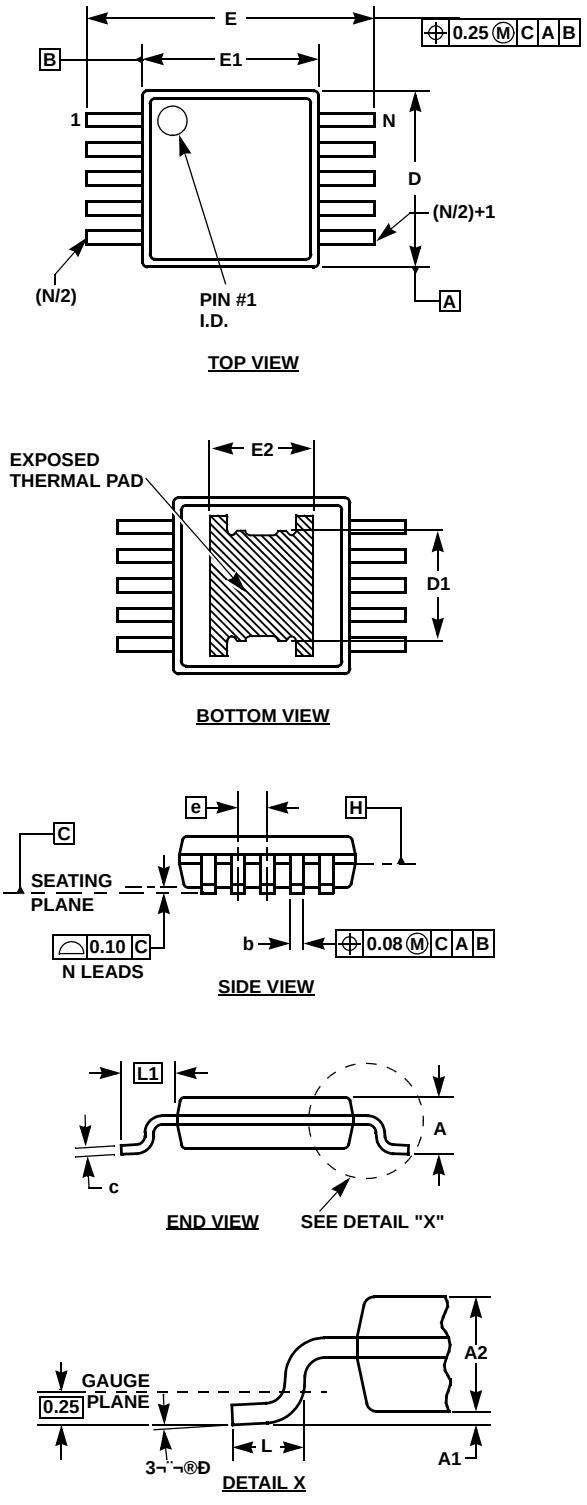
SYMBOL	MILLIMETERS			TOLERANCE
	TSOT5	TSOT6	TSOT8	
A	1.00	1.00	1.00	Max
A1	0.05	0.05	0.05	±0.05
A2	0.87	0.87	0.87	±0.03
b	0.38	0.38	0.29	±0.07
c	0.127	0.127	0.127	+0.07/-0.007
D	2.90	2.90	2.90	Basic
E	2.80	2.80	2.80	Basic
E1	1.60	1.60	1.60	Basic
e	0.95	0.95	0.65	Basic
e1	1.90	1.90	1.95	Basic
L	0.40	0.40	0.40	±0.10
L1	0.60	0.60	0.60	Reference
ddd	0.20	0.20	0.13	-
N	5	6	8	Reference

Rev. B 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.15mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (TSOT6 AND TSOT8 only).
6. TSOT5 version has no center lead (shown as a dashed line).

HMSOP (Heat-Sink MSOP) Package Family



MDP0050

HMSOP (HEAT-SINK MSOP) PACKAGE FAMILY

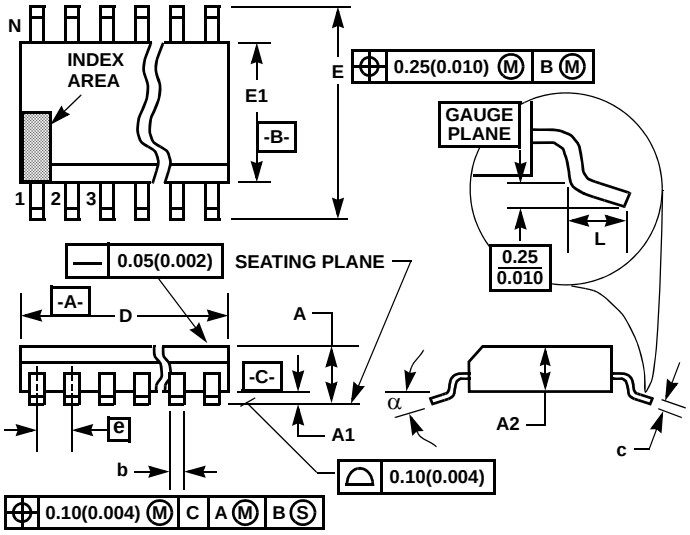
SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	HMSOP8	HMSOP10		
A	1.00	1.00	Max.	-
A1	0.075	0.075	+0.025/-0.050	-
A2	0.86	0.86	±0.09	-
b	0.30	0.20	+0.07/-0.08	-
c	0.15	0.15	±0.05	-
D	3.00	3.00	±0.10	1, 3
D1	1.85	1.85	Reference	-
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
E2	1.73	1.73	Reference	-
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. 1 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

Rev. 2 4/06