July 2015

# FSUSB42 — Low-Power, Two-Port, High-Speed, USB2.0 (480Mbps) UART Switch

## Features

- Low On Capacitance: 3.7 pF Typical
- Low On Resistance: 3.9 Ω Typical
- Low Power Consumption: 1 µA Maximum
  - 15 µA Maximum $I_{CCT}$ over an Expanded Voltage Range ($V_{IN}$=1.8 V, $V_{CC}$=4.4 V)
- Wide -3 db Bandwidth: > 720 MHz
- Packaged in:
  - 10-Lead UMLP (1.4 x 1.8 mm)
  - 10-Lead MSOP
- 8 kV ESD Rating, >16 kV Power / GND ESD Rating
- Over-Voltage Tolerance (OVT) on all USB Ports Up to 5.25 V without External Components

## Applications

- Cell phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

## Description

The FSUSB42 is a bi-directional, low-power, two-port, high-speed, USB2.0 switch. Configured as a double-pole, double-throw switch (DPDT) switch, it is optimized for switching between any combination of high-speed (480 Mbps) or Full-Speed (12 Mbps) sources.

The FSUSB42 is compatible with the requirements of USB2.0 and features an extremely low on capacitance ($C_{ON}$) of 3.7 pF. The wide bandwidth of this device (720 MHz) exceeds the bandwidth needed to pass the third harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk also minimizes interference.

The FSUSB42 contains special circuitry on the switch I/O pins for applications where the $V_{CC}$ supply is powered-off ($V_{CC}$=0 V), which allows the device to withstand an over-voltage condition. This device is designed to minimize current consumption even when the control voltage applied to the SEL pin is lower than the supply voltage ($V_{CC}$). This feature is especially valuable to ultra-portable applications, such as cell phones, allowing for direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

## Ordering Information

| Part Number | Top Mark | Operating Temperature Range | Package |
|---|---|---|---|
| FSUSB42UMX | HE | -40 to +85°C | 10-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8 mm |
| FSUSB42MUX | FSUSB42 | -40 to +85°C | 10-Lead, Molded Small-Outline Package (MSOP) JEDEC MO-187, 3.0 mm Wide |

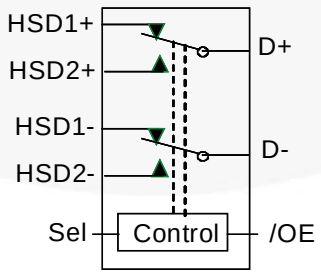



**Figure 1. Analog Symbol**

## Pin Assignments

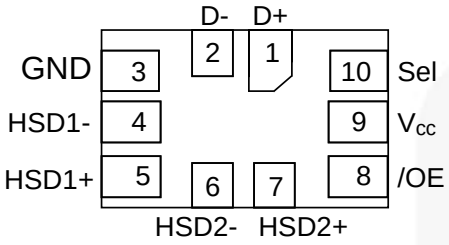



**Figure 2. 10-Lead UMLP (Top-Through View)**

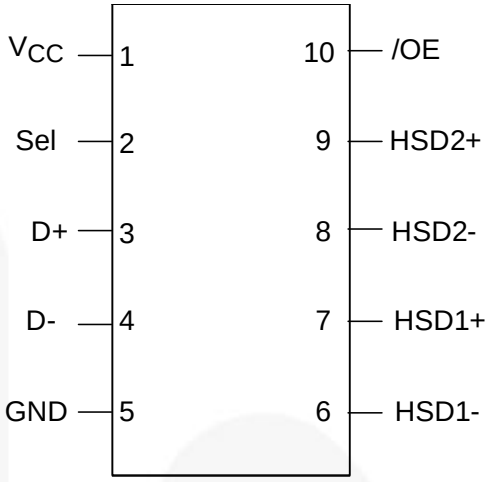



**Figure 3. 10-Lead MSOP (Top-Through View)**

## Pin Definitions

| UMLP Pin# | MSOP Pin# | Name | Description |
|---|---|---|---|
| 1 | 3 | D+ | Common USB Data Bus |
| 2 | 4 | D- | Common USB Data Bus |
| 3 | 5 | GND | Ground |
| 4 | 6 | HSD1- | Multiplexed Source Input 1 |
| 5 | 7 | HSD1+ | Multiplexed Source Input 1 |
| 6 | 8 | HSD2- | Multiplexed Source Input 2 |
| 7 | 9 | HSD2+ | Multiplexed Source Input 2 |
| 8 | 10 | /OE | Switch Enable |
| 9 | 1 | $V_{CC}$ | Supply Voltage |
| 10 | 2 | Sel | Switch Select |

## Truth Table

| SEL | /OE | Function |
|---|---|---|
| X | HIGH | Disconnect |
| LOW | LOW | D+= HSD1+, D-= HSD1- |
| HIGH | LOW | D+= HSD2+, D-= HSD2- |

**Notes:**
1. LOW ≤$V_{IL}$.
2. HIGH ≥$V_{IH}$.
3. X=Don't Care.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | -0.5 | 5.6 | V |
| $V_{CNTRL}$ | DC Input Voltage (S, /OE)[4] | | -0.5 | $V_{CC}$ | V |
| $V_{SW}$ | DC Switch I/O Voltage[4] (VCC=0V) | | -0.50 | 5.25 | V |
| $I_{IK}$ | DC Input Diode Current | | -50 | | mA |
| $I_{OUT}$ | DC Output Current | | | 100 | mA |
| $T_{STG}$ | Storage Temperature | | -65 | +150 | °C |
| MSL | Moisture Sensitivity Level (JEDEC J-STD-020A) | | | 1 | Level |
| ESD | Human Body Model, JEDEC: JESD22-A114 | All Pins | 7 | | kV |
| | | I/O to GND | 8 | | |
| | | Power to GND | 16 | | |
| | | D+/D- | 9 | | |
| | IEC 61000-4-2 System on USB Connector Pins D+ & D- | Air Discharge | 15 | | |
| | | Contact | 8 | | |
| | Charged Device Model, JEDEC: JESD22-C101 | | 2 | | |

**Note:**

4. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2.4 | 4.4 | V |
| $V_{CNTRL}$ | Control Input Voltage (S, /OE)[5] | 0 | $V_{CC}$ | V |
| $V_{SW}$ | Switch I/O Voltage | -0.5 | 4.5 | V |
| $T_A$ | Operating Temperature | -40 | +85 | °C |

**Note:**

5. The control input must be held HIGH or LOW and it must not float.

## DC Electrical Characteristics

All typical value are at $T_A$=25°C unless otherwise specified.

| Symbol | Parameter | Condition | $V_{CC}$ (V) | $T_A$=- 40°C to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{IK}$ | Clamp Diode Voltage | $I_{IN}$=-18mA | 3.0 | | | -1.2 | V |
| $V_{IH}$ | Input Voltage High | | 2.4 to 3.6 | 1.3 | | | V |
| | | | 4.3 | 1.7 | | | |
| $V_{IL}$ | Input Voltage Low | | 2.4 to 3.6 | | | 0.5 | V |
| | | | 4.3 | | | 0.7 | |
| $I_{IN}$ | Control Input Leakage | $V_{SW}$=0 to $V_{CC}$ | 0 to 4.3 | -1 | | 1 | µA |
| $I_{OZ}$ | Off State Leakage | 0 ≤ Dn, HSD1n, HSD2n ≤ 3.6 V | 4.3 | -2 | | 2 | µA |
| $I_{OFF}$ | Power-Off Leakage Current (All I/O Ports) | $V_{SW}$=0 V to 4.3 V, $V_{CC}$=0 V Figure 5 | 0 | -2 | | 2 | µA |
| $R_{ON}$ | HS Switch On Resistance(6) | $V_{SW}$=0.4 V, $I_{ON}$=-8 mA Figure 4 | 2.4 | | 4.5 | 7.5 | Ω |
| | | | 3.0 | | 3.9 | 6.5 | |
| $\Delta R_{ON}$ | HS Delta $R_{ON}$(7) | $V_{SW}$=0.4 V, $I_{ON}$=-8 mA | 3.0 | | 0.65 | | Ω |
| $I_{CC}$ | Quiescent Supply Current | $V_{CNTRL}$=0 or $V_{CC}$, $I_{OUT}$=0 | 4.3 | | | 1 | µA |
| $I_{CCT}$ | Increase in $I_{CC}$ Current per Control Voltage and $V_{CC}$ | $V_{CNTRL}$=2.6 V, $V_{CC}$=4.3 V | 4.3 | | | 10 | µA |
| | | $V_{CNTRL}$=1.8 V, $V_{CC}$=4.3 V | 4.3 | | | 15 | µA |

**Notes:**

6. Measured by the voltage drop between HSDn and Dn pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (HSDn or Dn ports).
7. Guaranteed by characterization.

## AC Electrical Characteristics

All typical value are for $V_{CC}$=3.3 V at $T_A$=25°C unless otherwise specified.

| Symbol | Parameter | Condition | $V_{CC}$ (V) | $T_A$=- 40°C to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $t_{ON}$ | Turn-On Time<br>S, /OE to Output | $R_L$=50 Ω, $C_L$=5 pF, $V_{SW}$=0.8 V, Figure 6, Figure 7 | 2.4 | | 24 | 40 | ns |
| | | | 3.0 to 3.6 | | 13 | 30 | |
| $t_{OFF}$ | Turn-Off Time<br>S, /OE to Output | $R_L$=50 Ω, $C_L$=5 pF, $V_{SW}$=0.8 V, Figure 6, Figure 7 | 2.4 | | 15 | 35 | ns |
| | | | 3.0 to 3.6 | | 12 | 25 | |
| $t_{PD}$ | Propagation Delay[8] | $C_L$=5 pF, $R_L$=50 Ω, Figure 6, Figure 8 | 3.3 | | 0.25 | | ns |
| $t_{BBM}$ | Break-Before-Make | $R_L$=50 Ω, $C_L$=5 pF, $V_{SW1}$=$V_{SW2}$=0.8 V, Figure 10 | 2.4 | 2.0 | | 10 | ns |
| | | | 3.0 to 3.6 | 2.0 | | 6.5 | |
| $O_{IRR}$ | Off Isolation | $R_L$=50 Ω, f=240 MHz, Figure 12 | 3.0 to 3.6 | | -30 | | dB |
| Xtalk | Non-Adjacent Channel Crosstalk | $R_L$=50 Ω, f=240 MHz, Figure 13 | 3.0 to 3.6 | | -45 | | dB |
| BW | -3db Bandwidth | $R_L$=50 Ω, $C_L$=0 pF, Figure 11 | 3.0 to 3.6 | | 720 | | MHz |
| | | $R_L$=50 Ω, $C_L$=5 pF, Figure 11 | | | 550 | | MHz |

**Note:**

8. Guaranteed by characterization.

## USB High-Speed-Related AC Electrical Characteristics

All typical value are for $V_{CC}$=3.3 V at $T_A$=25°C unless otherwise specified.

| Symbol | Parameter | Condition | $V_{CC}$ (V) | $T_A$=- 40ºC to +85ºC | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $t_{SK(P)}$ | Skew of Opposite Transitions of the Same Output[(9)] | $C_L$=5 pF, $R_L$=50 Ω, Figure 9 | | | 20 | | ps |
| $t_J$ | Total Jitter[(9)] | $R_L$=50 Ω, $C_L$=5 pF, $t_R$=$t_F$=500 ps (10-90%) at 480 Mbps (PRBS=$2^{15}$ – 1) | | | 200 | | ps |

**Note:**

9. Guaranteed by characterization.

## Capacitance

| Symbol | Parameter | Condition | $T_A$=- 40°C to +85°C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $C_{IN}$ | Control Pin Input Capacitance | $V_{CC}$=0 V | | 1.5 | | pF |
| $C_{ON}$ | D+/D- On Capacitance | $V_{CC}$=3.3 V, /OE=0 V, f=240 MHz, Figure 15 | | 3.7 | | |
| $C_{OFF}$ | D1n, D2n Off Capacitance | $V_{CC}$ and /OE=3.3 V, Figure 14 | | 2.0 | | |

## Test Diagrams

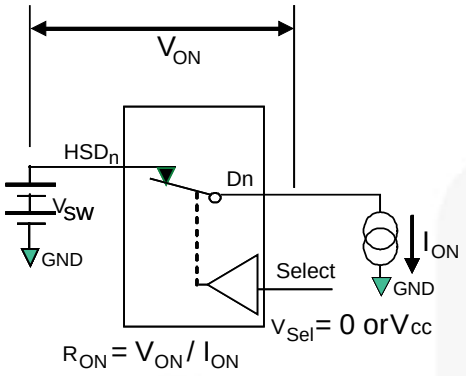
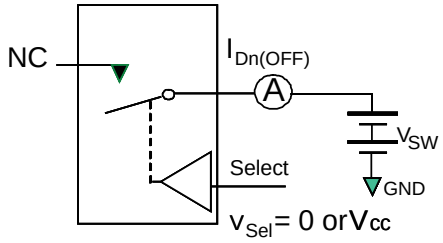
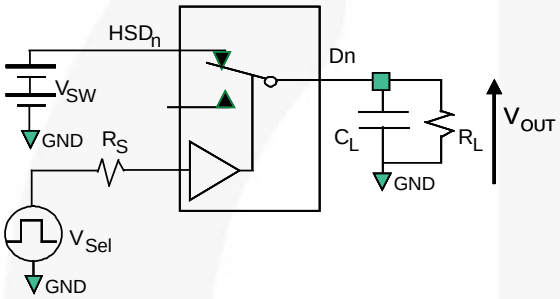



**Figure 4. On Resistance**




**Each switch port is tested separately

**Figure 5. Off Leakage**




$R_L$, $R_S$, and $C_L$ are functions of the application environment (see AC Tables for specific values)
$C_L$ includes test fixture and stray capacitance.

**Figure 6. AC Test Circuit Load**

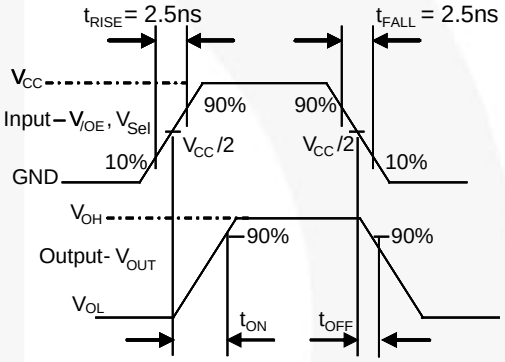



**Figure 7. Turn-On / Turn-Off Waveforms**

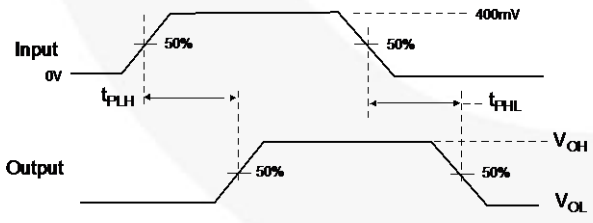



**Figure 8. Propagation Delay ($t_R t_F$ – 500 ps)**

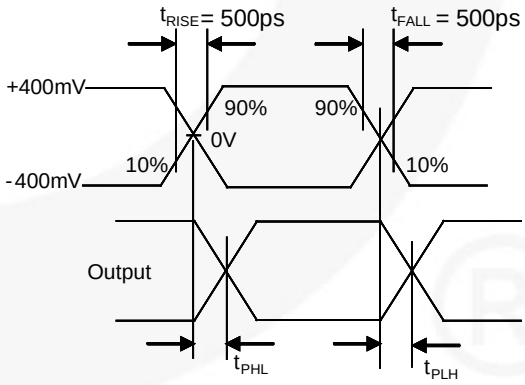
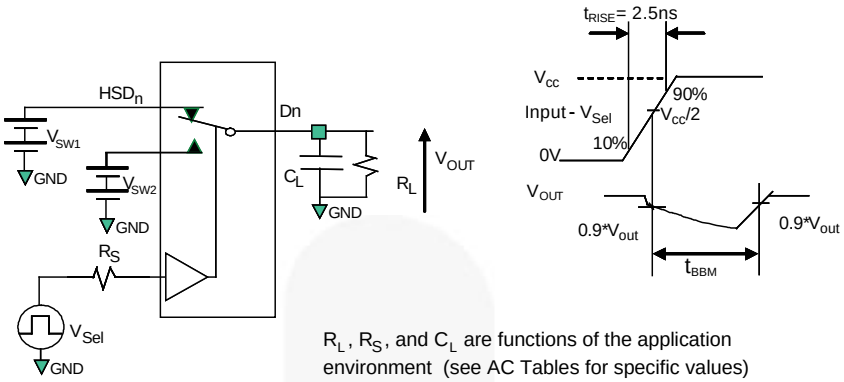


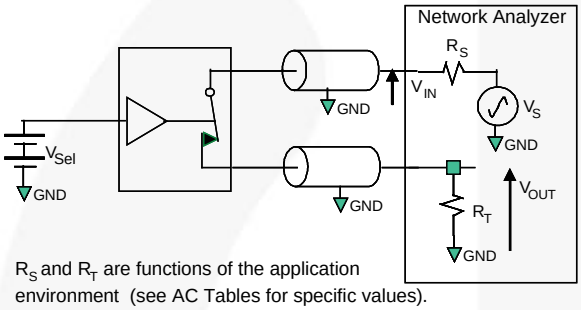

**Figure 9. Intra-Pair Skew Test $t_{SK(P)}$**

## Test Diagrams (Continued)



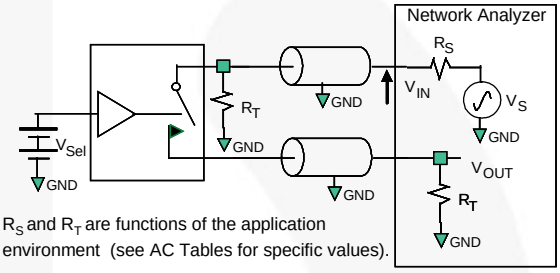

$R_L$, $R_S$, and $C_L$ are functions of the application environment (see AC Tables for specific values)
$C_L$ includes test fixture and stray capacitance.

**Figure 10. Break-Before-Make Interval Timing**




$R_S$ and $R_T$ are functions of the application environment (see AC Tables for specific values).

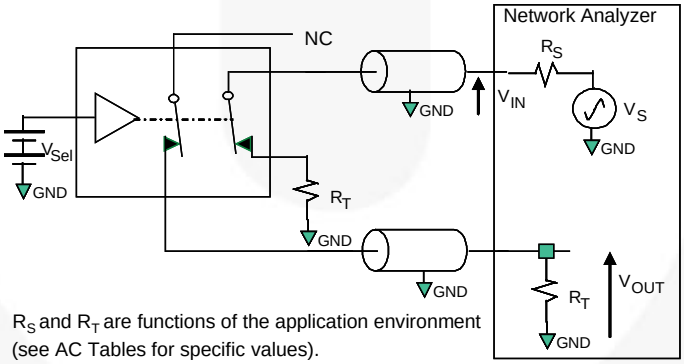
**Figure 11. Bandwidth**




$R_S$ and $R_T$ are functions of the application environment (see AC Tables for specific values).

Off isolation = 20 Log ($V_{OUT}$ / $V_{IN}$)

**Figure 12. Channel Off Isolation**




$R_S$ and $R_T$ are functions of the application environment (see AC Tables for specific values).

Crosstalk = 20 Log ($V_{OUT}$ / $V_{IN}$)

**Figure 13. Non-Adjacent Channel-to-Channel Crosstalk**

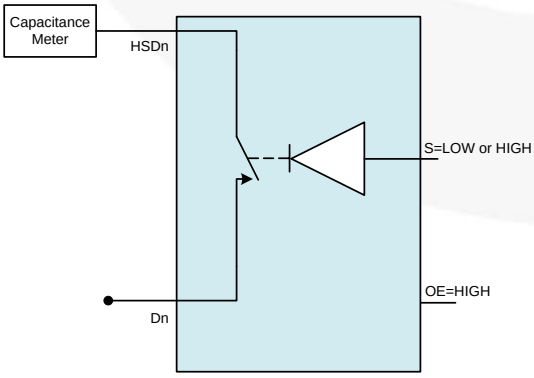



**Figure 14. Channel Off Capacitance**

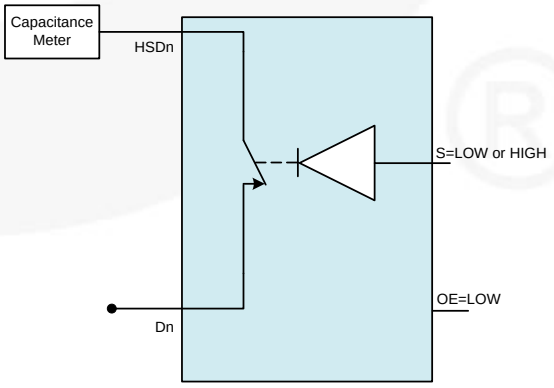
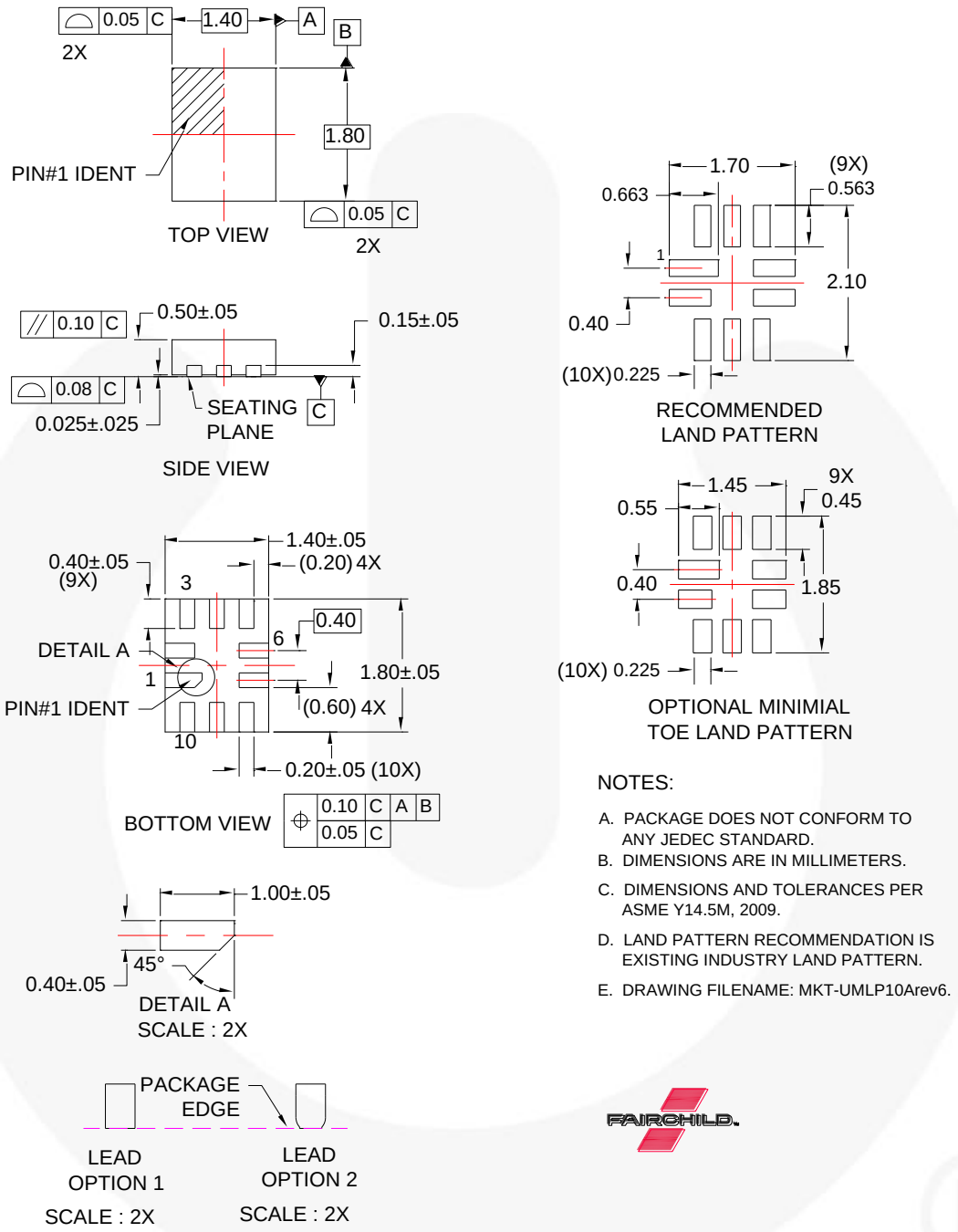



**Figure 15. Channel On Capacitance**

## Physical Dimensions




NOTES:

A. PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
E. DRAWING FILENAME: MKT-UMLP10Arev6.

**Figure 16. 10-Lead, Ultrathin Molded Leadless Package (UMLP)**

## Physical Dimensions (Continued)

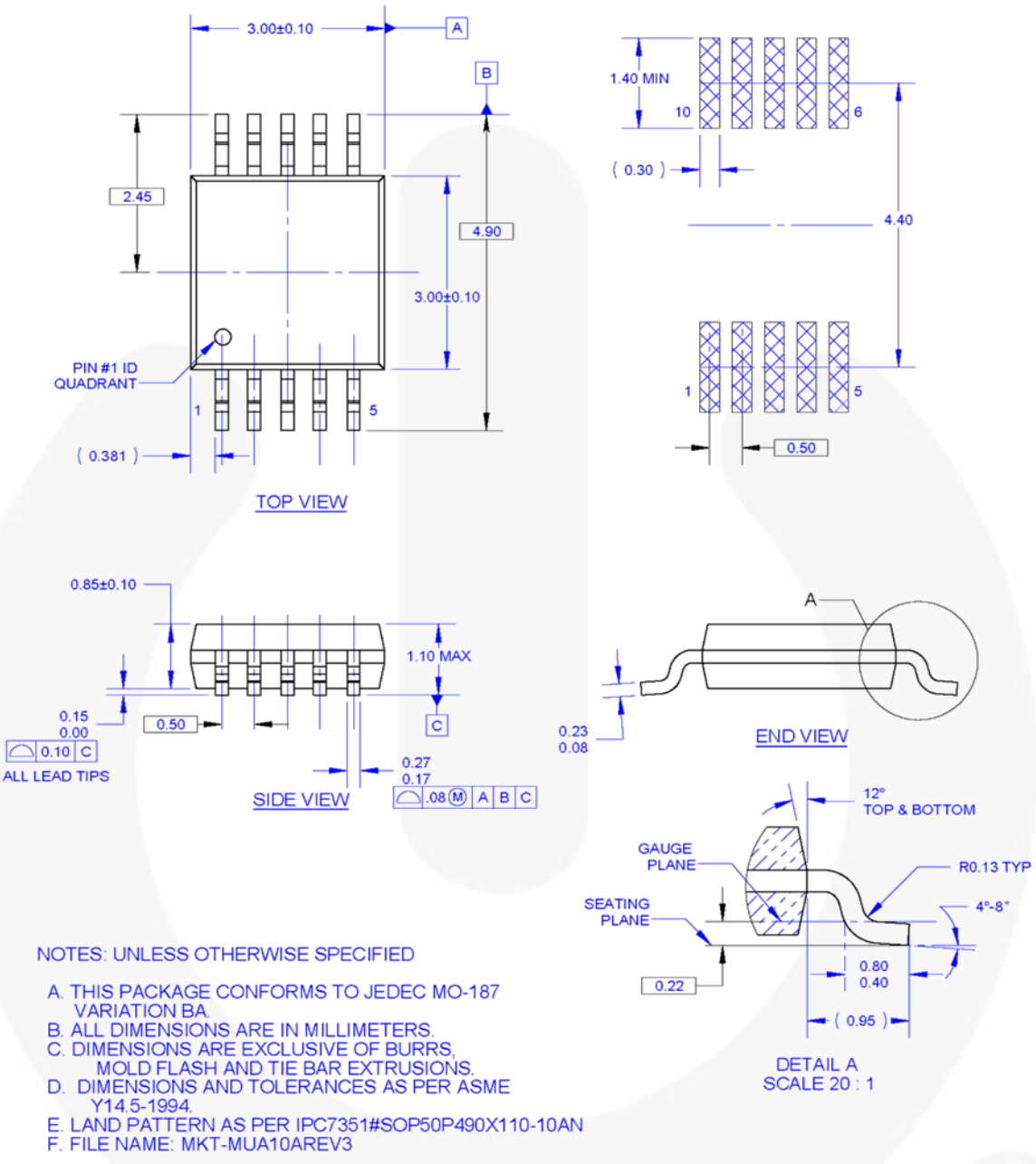



**Figure 17. 10-Lead, Molded Small Outline Package (MSOP)**

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