



Advanced
Micro
Devices

PALCE20V8 Family

EE CMOS 24-Pin Universal Programmable Array Logic

DISTINCTIVE CHARACTERISTICS

- Pin, function and fuse-map compatible with all GAL 20V8/As
- Electrically erasable CMOS technology provides reconfigurable logic and full testability
- High-speed CMOS technology
 - 10 ns propagation delay for "-10" version
 - 15 ns propagation delay for "-15" version
- Direct plug-in replacement for a wide range of 24-pin PAL devices
- Outputs individually programmable as registered or combinatorial
- Programmable output polarity
- Programmable enable/disable control
- Preloadable output registers for testability
 - Automatic register reset on power-up
- Cost-effective 24-pin plastic SKINNYDIP and 28-pin PLCC packages
- Extensive third-party software and programmer support through FusionPLD partners
- Fully tested for 100% programming and functional yields and high reliability

GENERAL DESCRIPTION

The PALCE20V8 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. Its macrocells provide a universal device architecture. The PALCE20V8 is fully compatible with the GAL20V8 and can directly replace PAL20R8 series devices and most 24-pin combinatorial PAL devices.

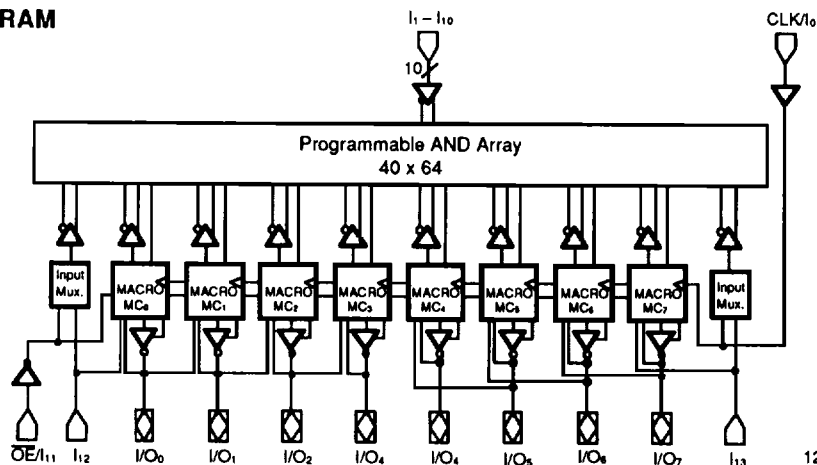
Device logic is automatically configured according to the user's design specification. A design is implemented using any of a number of popular design software packages, allowing automatic creation of a programming file based on Boolean or state equations. Design software also verifies the design and can provide test vectors for the finished device. Programming can be accomplished on standard PAL device programmers.

The PALCE20V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement

complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

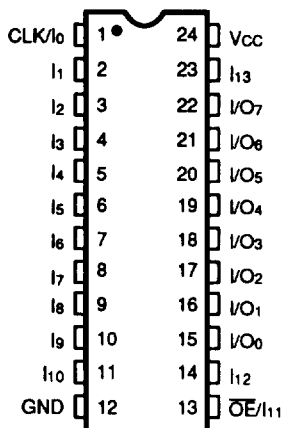
BLOCK DIAGRAM



12197-001B

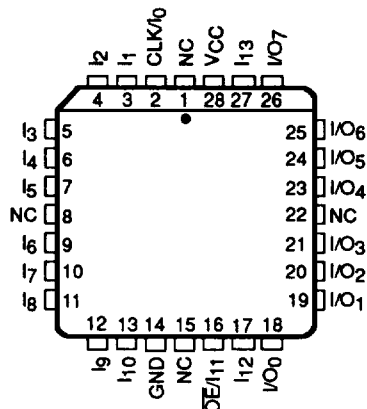
**CONNECTION DIAGRAMS
(Top View)**

SKINNYDIP



12197-002B

PLCC/LCC



12197-003A

Note: Pin 1 is marked for orientation.

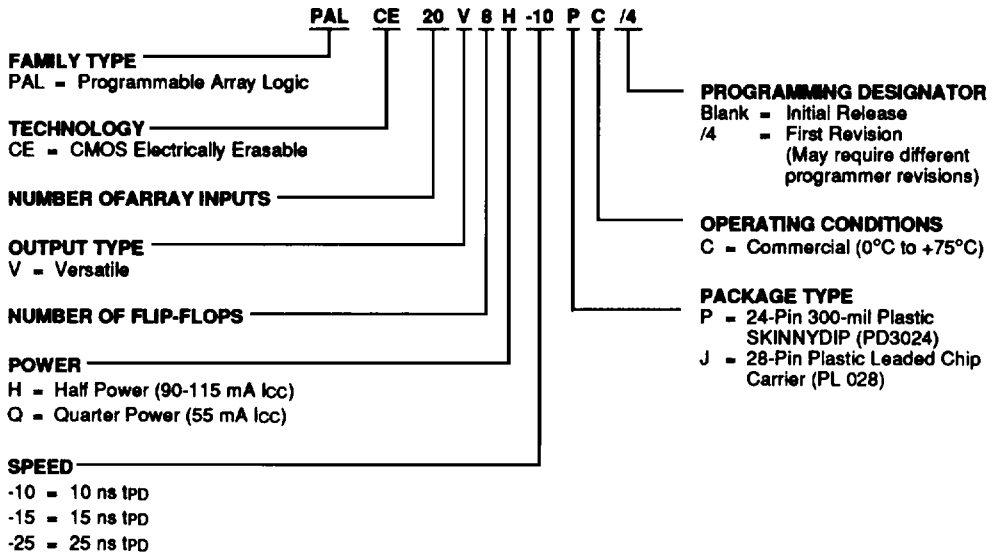
PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- NC = No Connect
- OE = Output Enable
- V_{cc} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE20V8H-10	PC, JC	/4
PALCE20V8H-15		Blank, /4
PALCE20V8H-25		
PALCE20V8Q-15		
PALCE20V8Q-25		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

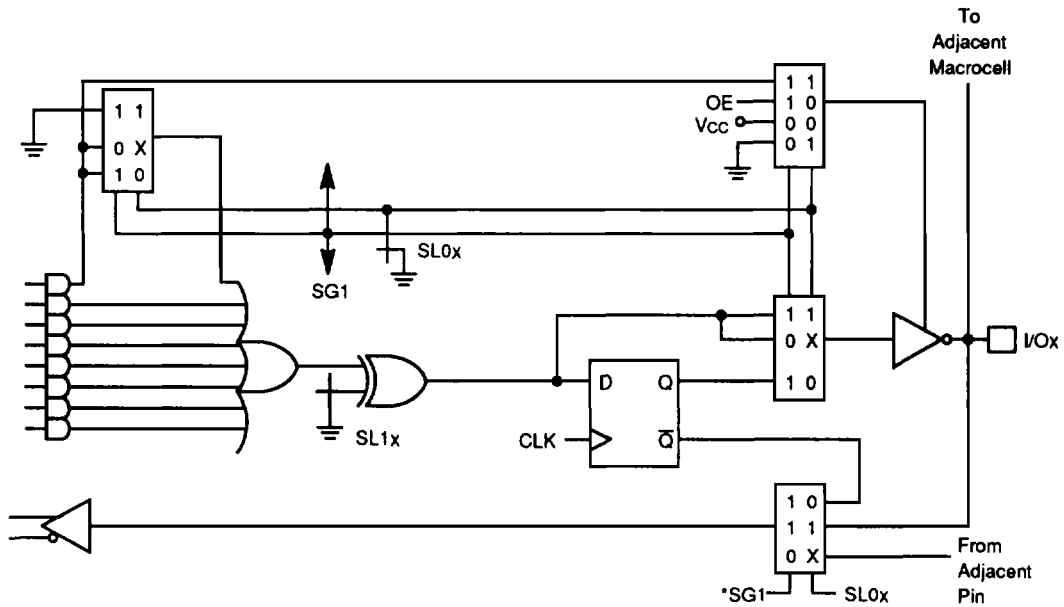
The PALCE20V8 is a universal PAL device. It has eight independently configurable macrocells (MC₀..MC₇). Each macrocell can be configured as a registered output, combinatorial output, combinatorial I/O, or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 13 serve either as array inputs or as clock (CLK) and output enable (\overline{OE}) for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE20V8 are automatically configured from the user's design specification, which can be in a number of formats. The design

specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE20V8. First, it can be programmed as an emulated PAL device. This includes the PAL20R8 series and most 24-pin combinatorial PAL devices. The PAL device programmer manufacturer will supply device codes for the standard PAL architectures to be used with the PALCE20V8. The programmer will program the PALCE20V8 to the corresponding PAL device architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed directly as a PALCE20V8. Here the user must use the PALCE20V8 device code. This option provides full utilization of the macrocells, allowing non-standard architectures to be built.



15027B-001B

* In Macrocells MC₀ and MC₇, SG₁ is replaced by $\overline{SG_0}$ on the feedback multiplexer.

Figure 1. PALCE20V8 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O or dedicated input. In the registered output configuration, the output buffer is enabled by the \overline{OE} pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, the buffer is always disabled. A macrocell configured as a dedicated input derives the input signal from an adjacent I/O.

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits (SL0₀ through SL0₇ and SL1₀ through SL1₇). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE20V8 will emulate a PAL20R8 family or a combinatorial device. Within each macrocell, SL0_x, in conjunction with SG1, selects the configuration of the macrocell and SL1_x sets the output as either active low or active high.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and SL0_x are the control signals for all four multiplexers. In MC₀ and MC₇, $\overline{SG0}$ replaces SG1 on the feedback multiplexer.

These configurations are summarized in table 1 and illustrated in figure 2.

If the PALCE20V8 is configured as a combinatorial device, the CLK and \overline{OE} pins may be available as inputs to the array. If the device is configured with registers, the CLK and \overline{OE} pins cannot be used as data inputs.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and SL0_x = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by SL1_x. SL1_x is an input to the exclusive-OR gate which is the D input to the flip-flop. SL1_x is programmed as 1 for inverted output or 0 for non-inverted output. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from \overline{Q} on the register. The output buffer is enabled by \overline{OE} .

Combinatorial Configurations

The PALCE20V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 0, and SL0_x = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of pins 18(21) and 19(23). Pins 18(21) and 19(23) do not use feedback in this mode.

Dedicated Input in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and SL0_x = 1. The output buffer is disabled. The feedback signal is an adjacent I/O pin.

Combinatorial I/O in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 1, and SL0_x = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Combinatorial I/O in a Registered Device

The control bit settings are SG0=0, SG1=1 and SL0_x=1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

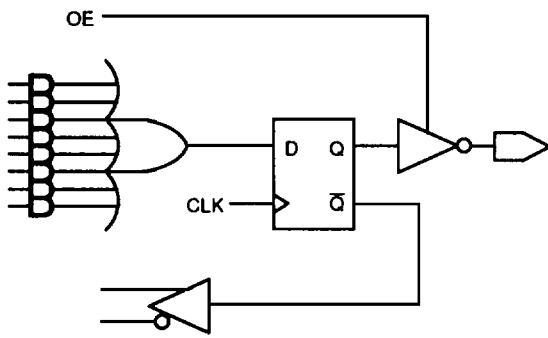
Table 1. Macrocell Configurations

SG0	SG1	SL0 _x	Cell Configuration	Devices Emulated
Device has registers				
0	1	0	Registered Output	PAL20R8, 20R6, 20R4
0	1	1	Combinatorial I/O	PAL20R6, 20R4
Device has no registers				
1	0	0	Combinatorial Output	PAL20L2, 18L4, 16L6, 14L8
1	0	1	Dedicated Input	PAL20L2, 18L4, 16L6
1	1	1	Combinatorial I/O	PAL20L8

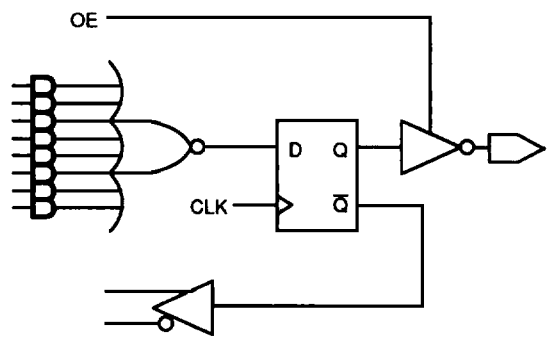
Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

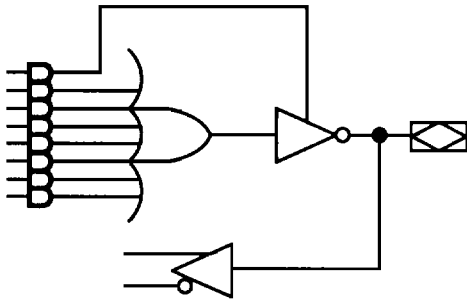
Selection is made through a programmable bit SL1_x which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if SL1_x is a 0 and active low if SL1_x is a 1.



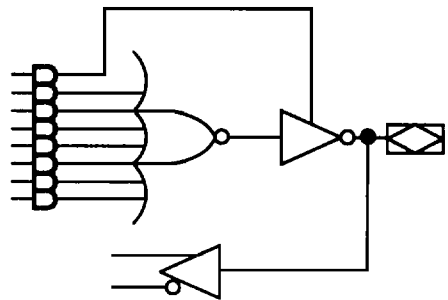
Registered Active Low



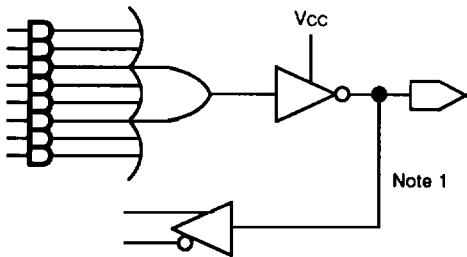
Registered Active High



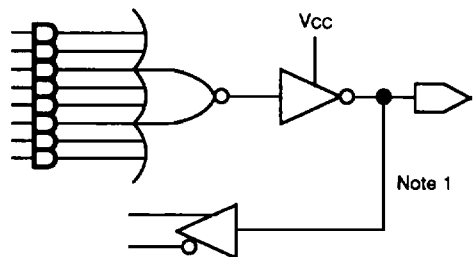
Combinatorial I/O Active Low



Combinatorial I/O Active High



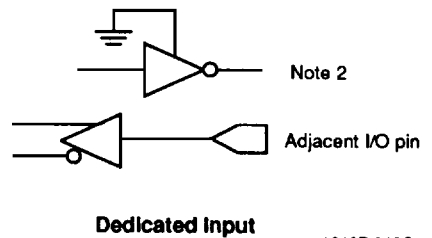
Combinatorial Output Active Low



Combinatorial Output Active High

Notes:

1. Feedback is not available on pins 18 (21) and 19 (23) in the combinatorial output mode.
2. This macrocell configuration is not available on pins 18 (21) and 19 (23).



Dedicated Input

12197-012C

Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE20V8 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE20V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE20V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback and verification of the programmed pattern by a device programmer, securing proprietary designs from competitors. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE20V8. It consists of 64 bits of programmable

memory that can contain any user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE20V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

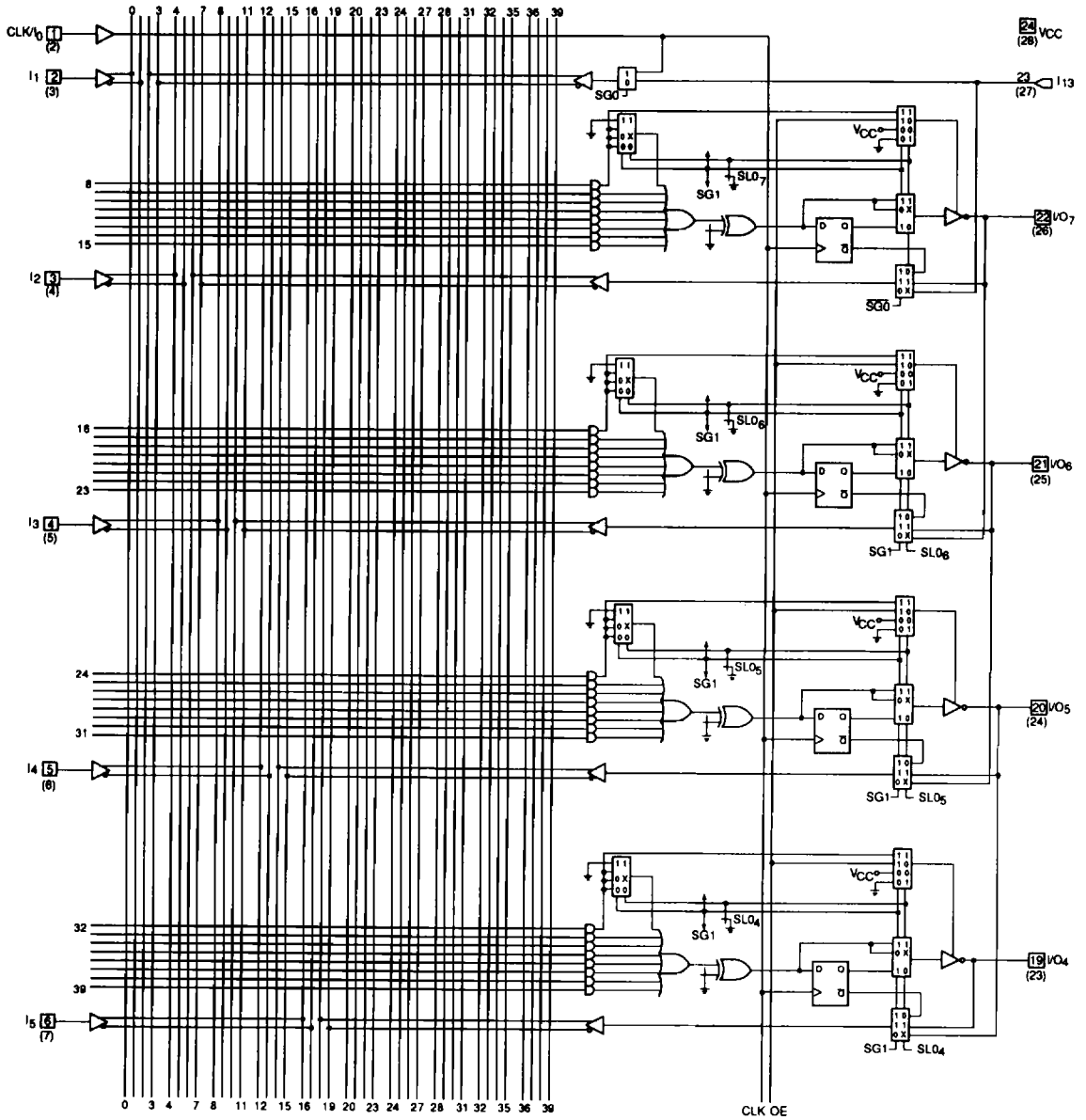
The PALCE20V8 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming and post-programming functional yields in the industry.

Technology

The high-speed PALCE20V8H is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

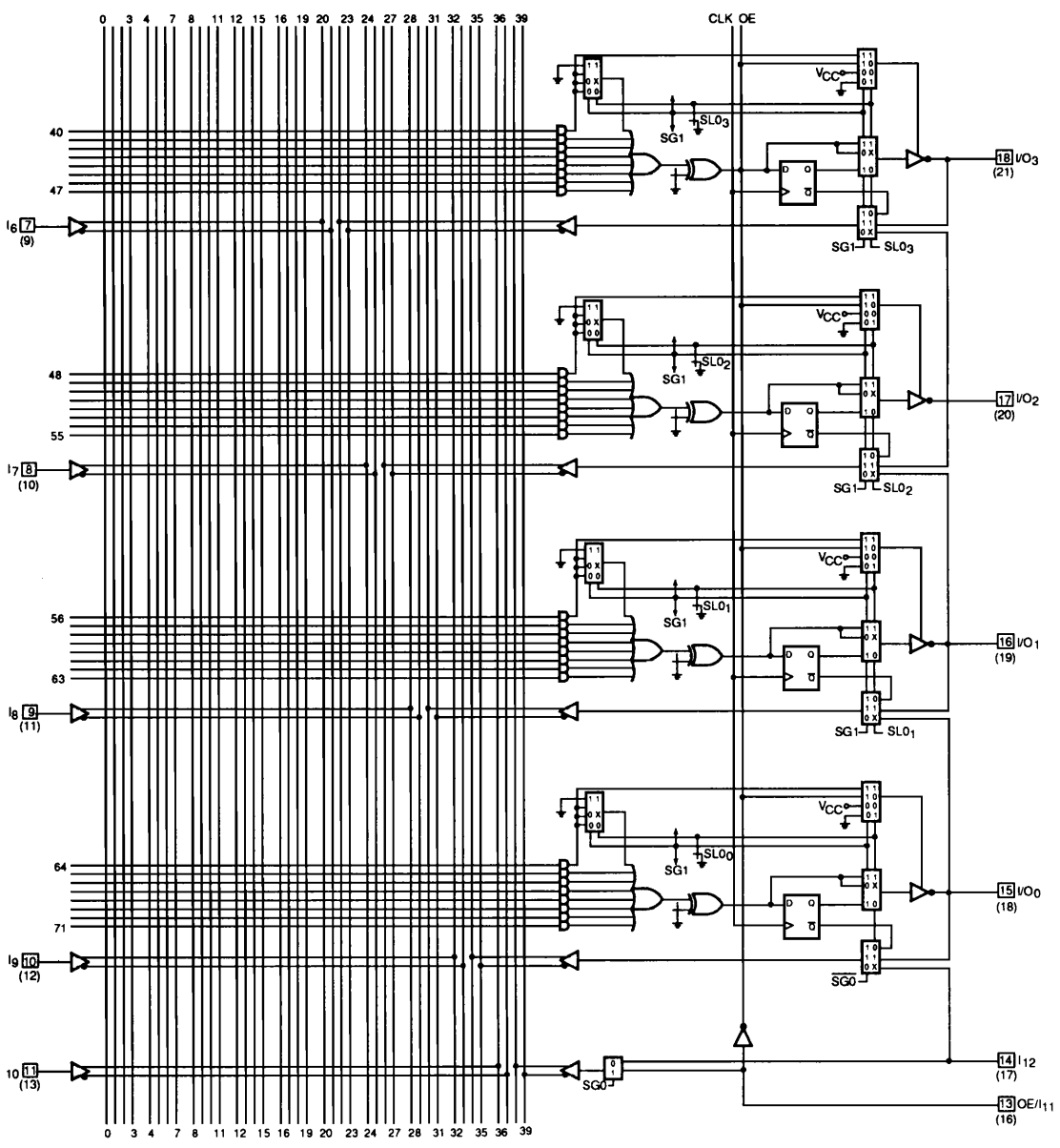


LOGIC DIAGRAM SKINNYDIP (PLCC and LCC) Pinouts



15027B-002A

LOGIC DIAGRAM (Continued)
SKINNYDIP (PLCC and LCC) Pinouts



15027B-002A
 concluded

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V
Latchup Current ($T_A = 0^\circ\text{C}$ to 75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to 75°C
Supply Voltage (V_{CC}) with Respect to Ground	4.75 V to 5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max.}$ (Note 2)		10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max.}$ (Note 2)		-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		10	μA
I_{OLZ}	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-150	mA
I_{CC}	Supply Current (Dynamic)	$V_{IN} = 0$ V, Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$, $f = 25$ MHz		115	mA

Notes:

- These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OLZ} (or I_{IH} and I_{OZH}).
- Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V, T _A = 25°C,	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description		Min.	Max.	Unit
t _{PD}	Input or Feedback to Combinatorial Output			10	ns
t _S	Setup Time from Input or Feedback to Clock		7.5		
t _H	Hold Time		0		ns
t _{CO}	Clock to Output			7.5	ns
t _{WL}	Clock Width	LOW	6		ns
t _{WH}		HIGH	6		ns
f _{MAX}	Maximum Frequency (Note 3)	External Feedback 1/(t _S +t _{CO})	66.7		MHz
		Internal Feedback (f _{CNT})	71.4		MHz
		No Feedback 1/(t _{WH} +t _{WL})	83.3		MHz
t _{PZX}	OE to Output Enable			10	ns
t _{PXZ}	OE to Output Disable			10	ns
t _{EA}	Input to Output Enable Using Product Term Control			10	ns
t _{ER}	Input to Output Disable Using Product Term Control			10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V
Latchup Current ($T_A = 0^\circ\text{C}$ to $+75^\circ\text{C}$)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max.}$ (Note 2)		10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max.}$ (Note 2)		-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-150	mA
I_{CC}	Supply Current	Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$, $f = 15$ MHz			
		H		90	mA
		Q		55	mA

Notes:

- These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V, T _A = 25°C, f = 1 MHz	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description		-15		-25		Unit
			Min.	Max.	Min.	Max.	
t _{PD}	Input or Feedback to Combinatorial Output			15		25	ns
t _S	Setup Time from Input or Feedback to Clock		12		15		ns
t _H	Hold Time		0		0		ns
t _{CO}	Clock to Output			10		12	ns
t _{WL}	Clock Width	LOW	8		12		ns
t _{WH}		HIGH	8		12		ns
f _{MAX}	Maximum Frequency (Note 3)	External Feedback 1/(t _S +t _{CO})	45.5		37		MHz
		Internal Feedback (f _{CNT})	50		40		MHz
		No Feedback 1/(t _{WH} +t _{WL})	62.5		41.6		MHz
t _{PZX}	\overline{OE} to Output Enable			15		20	ns
t _{PXZ}	\overline{OE} to Output Disable			15		20	ns
t _{EA}	Input to Output Enable Using Product Term Control			15		25	ns
t _{ER}	Input to Output Disable Using Product Term Control			15		25	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-85°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to $V_{CC} + 1.0$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 1.0$ V
Static Discharge Voltage	2001 V
Latchup Current ($T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	-55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	4.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at $T_C = +25^\circ\text{C}$, $+125^\circ\text{C}$ and -55°C , per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -2.0$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 12$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$ (Note 4)		10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max.}$ (Note 4)		-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.5$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$ (Note 5)	-30	-150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$, $f = 25$ MHz		130	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V, T _A = 25°C,	8	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description		-15		Unit
			Min.	Max.	
t _{PD}	Input or Feedback to Combinatorial Output			15	ns
t _S	Setup Time from Input or Feedback to Clock		12		
t _H	Hold Time		0		ns
t _{CO}	Clock to Output			12	ns
t _{WL}	Clock Width	LOW	10		ns
t _{WH}		HIGH	10		ns
f _{MAX}	Maximum Frequency (Note 3)	External Feedback 1/(t _S +t _{CO})	41.6		MHz
		Internal Feedback (f _{CNT})	45.5		MHz
		No Feedback 1/(t _{WH} +t _{WL})	50.0		MHz
t _{PZX}	\overline{OE} to Output Enable			15	ns
t _{PXZ}	\overline{OE} to Output Disable			15	ns
t _{EA}	Input to Output Enable Using Product Term Control (Note 4)			15	ns
t _{ER}	Input to Output Disable Using Product Term Control (Note 4)			15	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V
Latchup Current ($T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	-55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at $T_C = +25^\circ\text{C}$, $+125^\circ\text{C}$ and -55°C , per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -2.0$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 12$ mA $V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = \text{Min.}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$ (Note 4)		10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max.}$ (Note 4)		-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.5$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		10	μA
I_{OLZ}	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$ (Note 5)	-30	-150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$, $f = 25$ MHz		130	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OLZ} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V, T _A = 25°C,	8	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

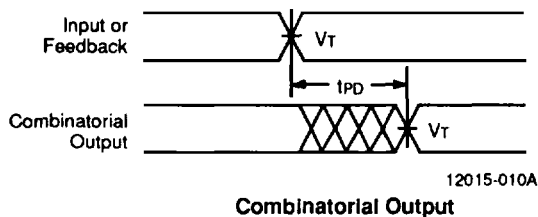
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description		-20		-25		Unit
			Min.	Max.	Min.	Max.	
t _{PD}	Input or Feedback to Combinatorial Output			20		25	ns
t _s	Setup Time from Input or Feedback to Clock		15		20		ns
t _H	Hold Time (Note 5)		0		0		ns
t _{CO}	Clock to Output			15		20	ns
t _{WL}	Clock Width	LOW	12		15		ns
t _{WH}		HIGH	12		15		ns
f _{MAX}	Maximum Frequency (Note 3)	External Feedback 1/(t _s +t _{CO})	33.3		25		MHz
		Internal Feedback (f _{CNT})	35.7		26.3		MHz
		No Feedback 1/(t _{WH} +t _{WL})	41.7		33.3		MHz
t _{PZX}	\overline{OE} to Output Enable (Note 3)			18		20	ns
t _{PXZ}	\overline{OE} to Output Disable (Note 3)			18		20	ns
t _{EA}	Input to Output Enable Using Product Term Control (Note 3)			20		25	ns
t _{ER}	Input to Output Disable Using Product Term Control (Note 3)			20		25	ns

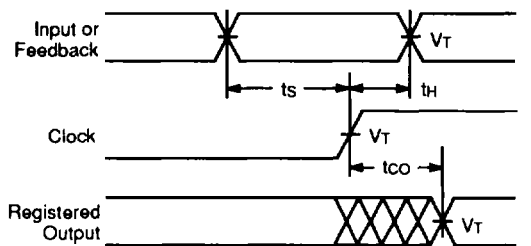
Notes:

2. See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

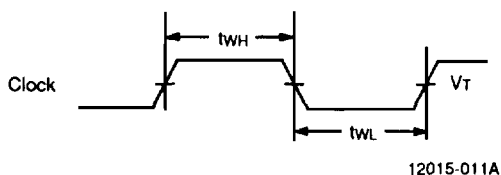
SWITCHING WAVEFORMS



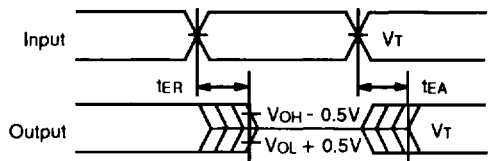
Combinatorial Output



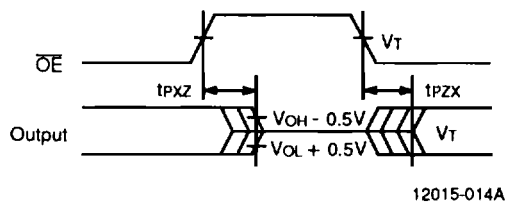
Registered Output



Clock Width



Input to Output Disable/Enable





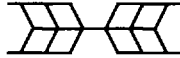


\overline{OE} to Output Disable/Enable

Notes:

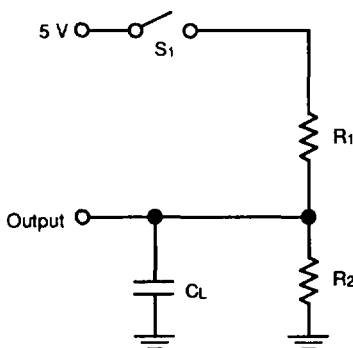
1. $V_T = 1.5\text{ V}$
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



Switching Test Circuit

12197-007A

Specification	S ₁	C _L	Commercial		Military		Measured Output Value
			R ₁	R ₂	R ₁	R ₂	
t _{PD} , t _{CO}	Closed	50 pF	200 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t _{PZX} , t _{EA}	Z → H: Open Z → L: Closed	50 pF	200 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t _{PXZ} , t _{ER}	H → Z: Open L → Z: Closed	5 pF	200 Ω	390 Ω	390 Ω	750 Ω	H → Z: V _{OH} - 0.5 V L → Z: V _{OL} + 0.5 V

ENDURANCE CHARACTERISTICS

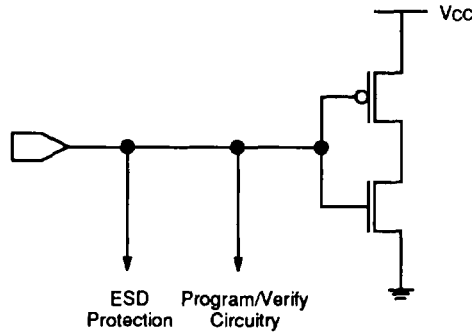
The PALCE20V8 is manufactured using AMD's advanced electrically erasable process. This technology uses an EE cell to replace the fuse link used in bipolar

parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

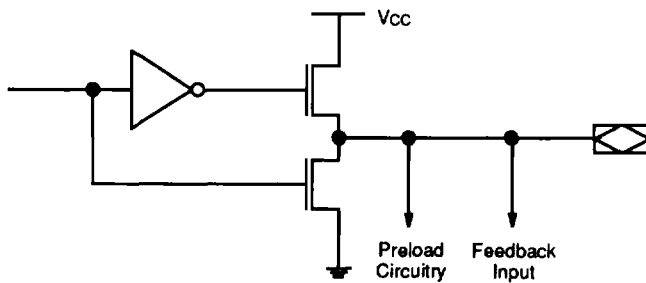
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
tDR	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (Military)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

12197-013A

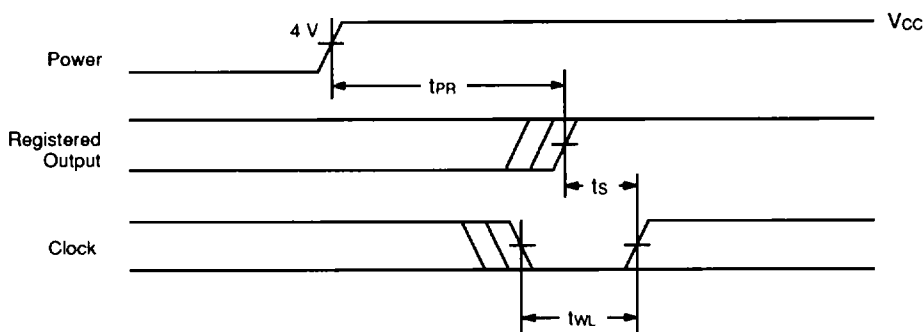
POWER-UP RESET

The PALCE20V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset

and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_s	Input or Feedback Setup Time	See Switching Characteristics		
t_{wL}	Clock Width LOW			



12197-009A

Power-Up Reset Waveforms