National Semiconductor

NMC2148H 1024 x 4-Bit Static RAM

General Description

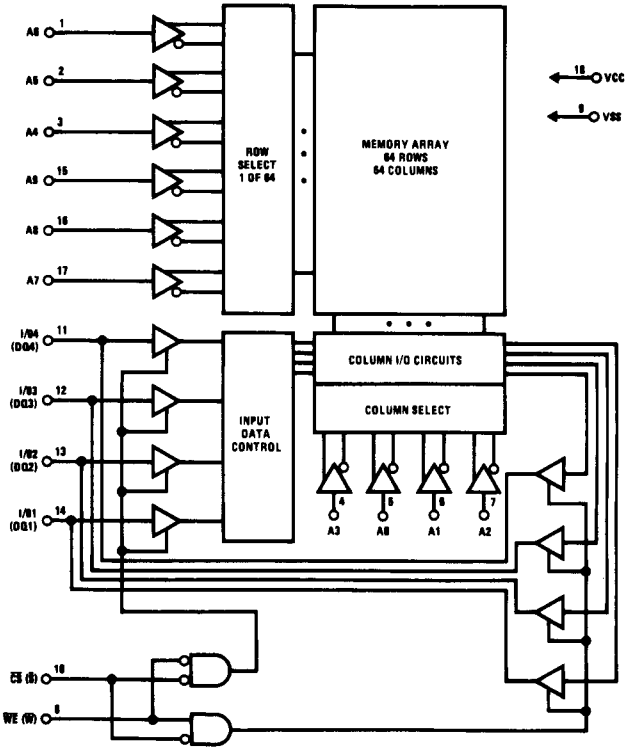
The NMC2148H is a 1024-word by 4-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

The separate chip select input automatically switches the part to its low power standby mode when it goes high. Common input/output pins are provided.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power-down
- High-speed—down to 45 ns access time
- TRI-STATE® output for bus interface
- Common data I/O pins
- Single +5V supply
- Standard 18-pin dual-in-line package

Block Diagram*



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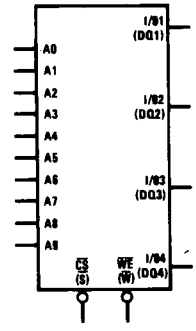
Logic Symbol*



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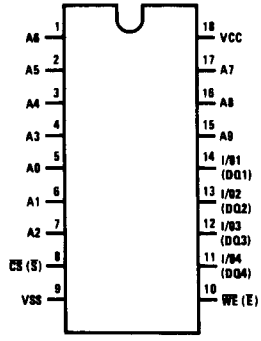
Connection Diagram*

Dual-In-Line Package



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Top View

Pin Names*

A0–A9	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS}$ ($\overline{S}$)	Chip Select
1/01–1/04 (DQ1–DQ4)	Data Input/Output
VCC	Power (5V)
VSS	Ground

Order Number NMC2148HJ-L, NMC2148HJ-3L, NMC2148HJ, NMC2148HJ-2 or NMC2148HJ-3
See NS Package Number J18A

*Symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin with Respect to VSS	−3.5V to +7V
Storate Temperature	−65°C to +150°C
Temperature with Bias	−10°C to +85°C
DC Output Current	20 mA
Power Dissipation	1.2W
Lead Temperature (Soldering, 10 sec.)	300°C

Truth Table

$\overline{CS}$	$\overline{WE}$	I/O	Mode	Power
H	X	Hi-Z	Standby	Standby
L	L	H	Write 1	Active
L	L	L	Write 0	Active
L	H	DOUT	Read	Active

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ± 10% (Notes 1 and 2)

Symbol	Parameter	Conditions	NMC2148H-L NMC2148H-3L		NMC2148H NMC2148H-2 NMC2148H-3		Units
			Min	Max	Min	Max	
|ILI|	Input Load Current (All Input Pins)	VIN = 0V to 5.5V, VCC = Max		10		10	μA
|ILO|	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = GND to 4.5V, VCC = Max		50		50	μA
VIL	Input Low Voltage		−2.5	0.8	−2.5	0.8	V
VIH	Input High Voltage		2.1	6.0	2.1	6.0	V
VOL	Output Low Voltage	IOL = 8.0 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −4.0 mA	2.4		2.4		V
ICC	Power Supply Current	VIN = 5.5V, TA = 0°C, Output Open		125		180	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		20		30	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min, $\overline{CS}$ = Lower of VCC or VIH Min		30		40	mA
|IOS|	Output Short Circuit Current	VOUT = GND to VCC		250		250	mA

Capacitance TA = 25°C, f = 1.0 MHz (Note 3)

Symbol	Parameter	Conditions	Min	Max	Units
CIN	Address/Control Capacitance	VIN = 0V		5	pF
CI/O	Input/Output Capacitance	VI/O = 0V		7	pF

Note 1: The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

Note 2: These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper operation after power-on. This allows the internally generated substrate bias to reach its functional level.

Note 3: This parameter is guaranteed by periodic testing.

AC Test Conditions

Input Test Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Level	1.5V
Output Timing Reference Levels	0.8V and 2.0V
Output Load	See *Figure 1*

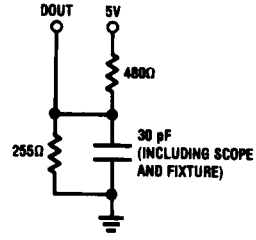

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FIGURE 1. Output Load

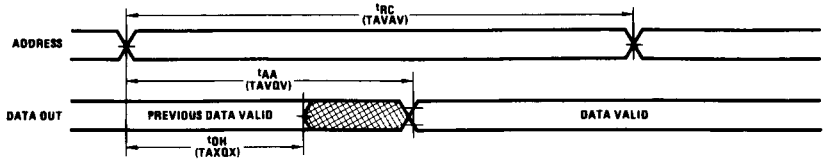
Read Cycle AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Note 1)

Symbol		Parameter	NMC2148H-2		NMC2148H-3 NMC2148H-3L		NMC2148H NMC2148H-L		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	45		55		70		ns
t_{AA}	TAVQV	Address Access Time		45		55		70	ns
t_{ACS1}	TSLQV1	Chip Select Access Time (Notes 4 and 5)		45		55		70	ns
t_{ACS2}	TLSQV2	Chip Select Access Time (Notes 4 and 6)		55		65		80	ns
t_{LZ}	TSLQX	Chip Select to Output Active (Note 7)	20		20		20		ns
t_{HZ}	TSHQZ	Chip Deselect to Output TRI-STATE (Note 7)	0	20	0	20	0	20	ns
t_{OH}	TAXQX	Output Hold from Address Change	5		5		5		ns
t_{PU}	TSLIH	Chip Select to Power-Up	0		0		0		ns
t_{PD}	TSHIL	Chip Deselect to Power-Down		30		30		30	ns

Max Access/Current	NMC2148H-2	NMC2148H-3	NMC2148H	NMC2148H-3L	NMC2148H-L
Access (TAVQV—ns)	45	55	70	55	70
Active Current (ICC—mA)	180	180	180	125	125
Standby Current (ISB—mA)	30	30	30	20	20

Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)



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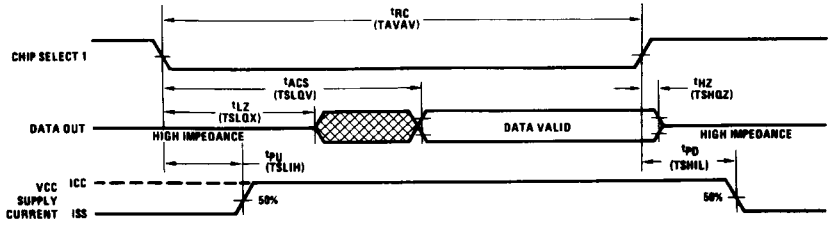
Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 4)



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Note 4: Addresses must be valid coincident with or prior to the chip select transition from high to low.

Note 5: Chip deselected longer than 55 ns.

Note 6: Chip deselected less than 55 ns.

Note 7: Measured ±50 mV from steady state voltage. This parameter is sampled and not 100% tested.

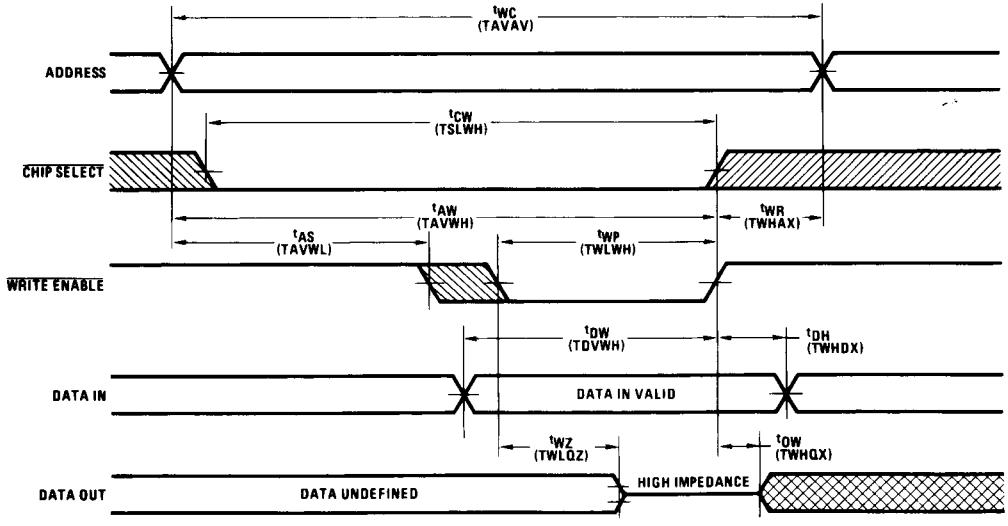
*The symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2148H-2		NMC2148H-3 NMC2148H-3L		NMC2148H NMC2148H-L		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	45		55		70		ns
t_{CW}	TSLWH	Chip Select to End of Write	40		50		65		ns
t_{AW}	TAVWH	Address Valid to End of Write	40		50		65		ns
t_{AS}	TAVSL TAVWL	Address Set-Up Time	0		0		0		ns
t_{WP}	TWLWH	Write Pulse Width	35		40		50		ns
t_{WR}	TWHAX	Write Recovery Time	5		5		5		ns
t_{DW}	TDVWH	Data Set-Up Time	20		20		25		ns
t_{DH}	TWHDX	Data Hold Time	0		0		0		ns
t_{WZ}	TWLQZ	Write Enable to Output TRI-STATE (Note 7)	0	15	0	20	0	25	ns
t_{OW}	TWHQX	Output Active from End of Write (Note 7)	0		0		0		ns

Write Cycle Waveforms* (Note 8)

Write Cycle 1 (Write Enable Limited)



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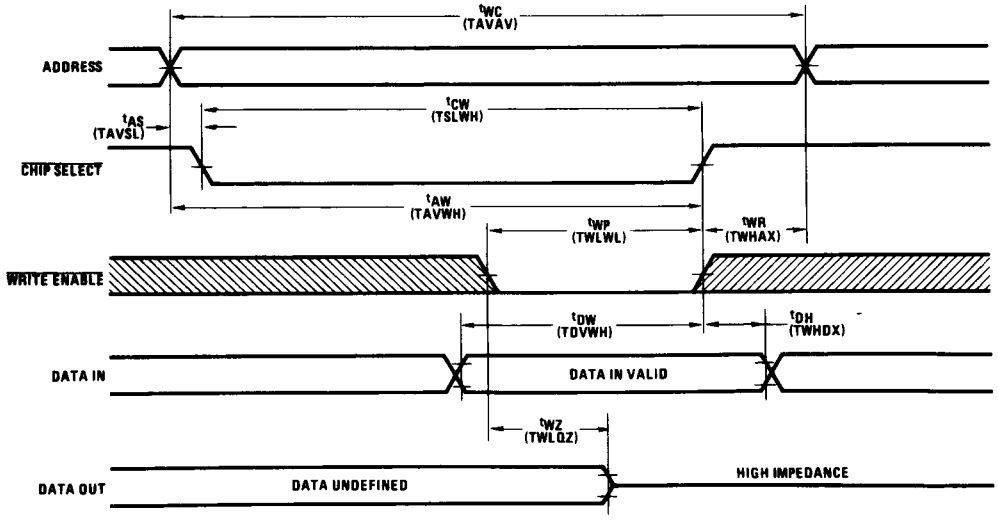
Write Cycle Waveforms* (Note 8) (Continued)

Write Cycle 2 (Chip Select Limited)



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Note 8: The output remains TRI-STATE if the $\overline{CS}$ and $\overline{WE}$ go high simulataneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions to prevent an erroneous write.

*Symbols in parentheses are proposed industry standard.