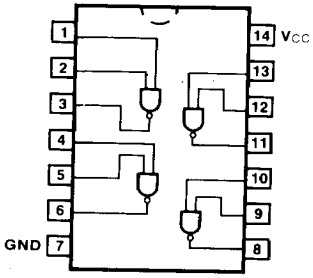
# 54/7400 011065
# 54H/74H00 011069
# 54S/74S00 011574
# 54LS/74LS00 011068

## QUAD 2-INPUT NAND GATE

**CONNECTION DIAGRAMS**
PINOUT A

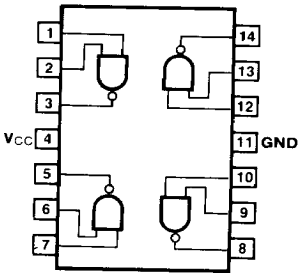





**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE<br>$V_{CC}$ = +5.0 V ±5%,<br>$T_A$ = 0°C to +70°C | MILITARY GRADE<br>$V_{CC}$ = +5.0 V ±10%,<br>$T_A$ = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 7400PC, 74H00PC<br>74LS00PC, 74S00PC | | 9A |
| Ceramic DIP (D) | A | 7400DC, 74H00DC<br>74LS00DC, 74S00DC | 5400DM, 54H00DM<br>54LS00DM, 54S00DM | 6A |
| Flatpak (F) | A | 74LS00FC, 74S00FC | 54LS00FM, 54S00FM | 3I |
| | B | 7400FC, 74H00FC | 5400FM, 54H00FM | |

PINOUT B




**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PINS | 54/74 (U.L.) HIGH/LOW | 54/74H (U.L.) HIGH/LOW | 54/74S (U.L.) HIGH/LOW | 54/74LS (U.L.) HIGH/LOW |
|---|---|---|---|---|
| Inputs | 1.0/1.0 | 1.25/1.25 | 1.25/1.25 | 0.5/0.25 |
| Outputs | 20/10 | 12.5/12.5 | 25/12.5 | 10/5.0 (2.5) |

**DC AND AC CHARACTERISTICS:** See Section 3*

| SYMBOL | PARAMETER | 54/74 Min | 54/74 Max | 54/74H Min | 54/74H Max | 54/74S Min | 54/74S Max | 54/74LS Min | 54/74LS Max | UNITS | CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CCH}$ | Power Supply | | 8.0 | | 16.8 | | 16 | | 1.6 | mA | $V_{IN}$ = Gnd | $V_{CC}$ = Max |
| $I_{CCL}$ | Current | | 22 | | 40 | | 36 | | 4.4 | | $V_{IN}$ = Open | |
| $t_{PLH}$ | Propagation Delay | | 22 | | 10 | 2.0 | 4.5 | | 10 | ns | Figs. 3-1, 3-4 | |
| $t_{PHL}$ | | | 15 | | 10 | 2.0 | 5.0 | | 10 | | | |

*DC limits apply over operating temperature range; AC limits apply at $T_A$ = +25°C and $V_{CC}$ = +5.0 V.



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