

December 1996

Fast CMOS 3.3V 16-Bit Buffer/Line Driver

Features

- Advanced 0.6 micron CMOS Technology
- Advanced Low Power CMOS Operation
- Can Serve as a 5V to 3V Translator
- Excellent Output Drive Capability:
 - Balanced Drives (24mA Sink and Source)
 - Compatible with LVC™ Class of Products
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Inputs Can Be Driven by 3.3V or 5V Devices
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Ordering Information

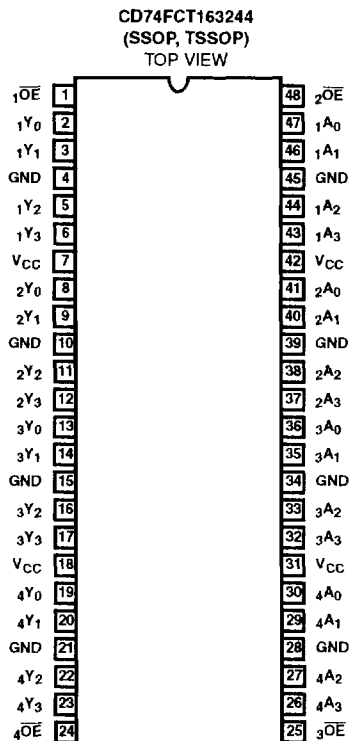
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT163244AMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163244ASM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT163244CMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163244CSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT163244MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163244SM	-40 to 85	48 Ld SSOP	M48.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

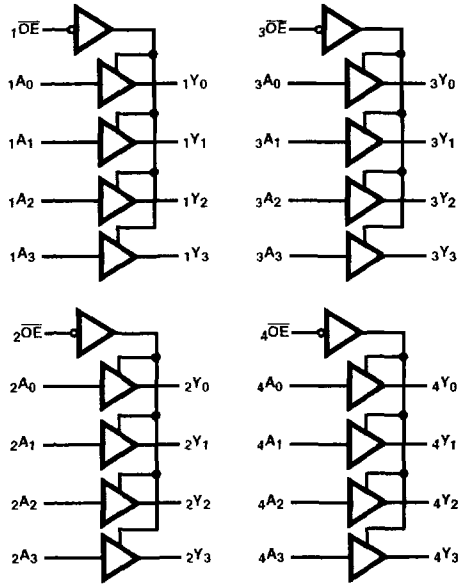
The CD74FCT163244 is a 16-bit buffer/line driver designed for applications driving high capacitive loads and low impedance backplanes. This high-speed, low power device offers bus/backplane interface capability and a flow-through organization for ease of board layout. This device is designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

Pinout



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Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
\overline{xOE}	xAx	xYx
L	L	L
L	H	H
H	X	Z

NOTE:

- 1. H = High Voltage Level
- L = Low Voltage Level
- X = Don't Care
- Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
\overline{xOE}	Three-State Output Enable Inputs (Active LOW)
xAx	Inputs
xYx	Three-State Outputs
GND	Ground
V_{CC}	Power

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS	MIN	(NOTE 4) TYP	MAX	UNITS	
Short Circuit Current (Note 6)	I_{OS}	$V_{CC} = \text{Max (Note 5)}$, $V_{OUT} = \text{GND}$	-60	-85	-240	mA	
Input Hysteresis	V_H		-	150	-	mV	
CAPACITANCE $T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$							
Input Capacitance (Note 7)	C_{IN}	$V_{IN} = 0\text{V}$	-	4.5	6	pF	
Output Capacitance (Note 7)	C_{OUT}	$V_{OUT} = 0\text{V}$	-	5.5	8	pF	
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$ or V_{CC}	-	0.1	10	μA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	$V_{CC} = \text{Max}$	$V_{IN} = V_{CC} - 0.6\text{V}$ (Note 9)	-	2.0	30	μA
Dynamic Power Supply Current (Note 10)	I_{CCD}	$V_{CC} = \text{Max}$, Outputs Open $\overline{x}OE = \text{GND}$ One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	50	75	$\mu\text{A}/\text{MHz}$
Total Power Supply Current (Note 12)	I_C	$V_{CC} = \text{Max}$, Outputs Open $f_1 = 10\text{MHz}$, 50% Duty Cycle $\overline{x}OE = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC} - 0.6\text{V}$ $V_{IN} = \text{GND}$	-	0.5	0.8	mA
		$V_{CC} = \text{Max}$, Outputs Open $f_1 = 2.5\text{MHz}$, 50% Duty Cycle $\overline{x}OE = \text{GND}$ 16 Bits Toggling	$V_{IN} = V_{CC} - 0.6\text{V}$ $V_{IN} = \text{GND}$	-	2.0	3.3 (Note 11)	mA

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Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74FCT163244		CD74FCT163244A		CD74FCT163244C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
CD74FCT16244, CD74FCT162244									
Propagation Delay xAX to xYX	t_{PLH} t_{PHL}	$C_L = 50pF$ $R_L = 500\Omega$	1.5	6.5	1.5	4.8	1.5	4.1	ns
Output Enable Time xOE to xYX	t_{PZH} t_{PZL}		1.5	8.0	1.5	6.2	1.5	5.8	ns
Output Disable Time (Note 16) xOE to xYX	t_{PHZ} t_{PLZ}		1.5	7.0	1.5	5.6	1.5	5.2	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

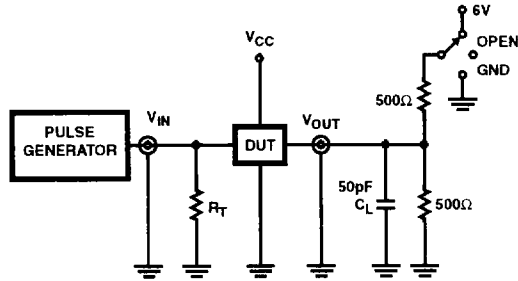
NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at $V_{CC} = 3.3V$, $25^\circ C$ ambient and maximum loading
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. This parameter is determined by device characterization but is not production tested.
8. $V_{OH} = V_{CC} - 0.6V$ at rated current.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 N_{CP} = Number of Clock Inputs at f_{CP}
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3V \pm 0.3V$, normal range. For $V_{CC} = 2.7V$, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuits and waveforms.
15. Minimum limits are guaranteed but not tested on Propagation Delays
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

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Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
t_{PLZ} , t_{PZL} , Open Drain	6V
t_{PHZ} , t_{PZH}	GND
t_{PLH} , t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate \leq 1.0MHz; $Z_{OUT} \leq$ 50Ω;
 t_r , $t_f \leq$ 2.5ns.

FIGURE 1. TEST CIRCUIT

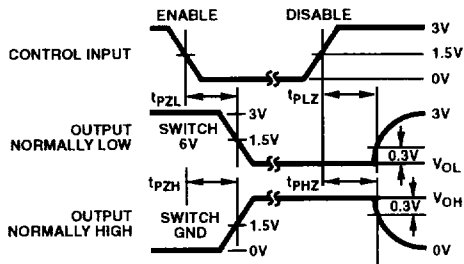


FIGURE 2. ENABLE AND DISABLE TIMING

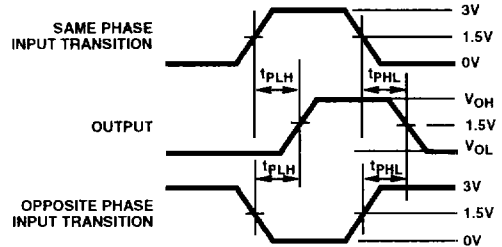


FIGURE 3. PROPAGATION DELAY