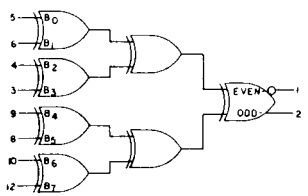
EIGHT-BIT PARITY CHECKER and GENERATOR

MECL II MC1000/1200 series

MC1046
MC1246

Advance Information

POSITIVE LOGIC



DC INPUT LOADING FACTOR = 1
DC OUTPUT LOADING FACTOR = 25
POWER DISSIPATION = 205 mW TYP

Seven Exclusive-OR gates in a single package, interconnected to provide simultaneous ODD-EVEN parity generation or checking.

TRUTH TABLE

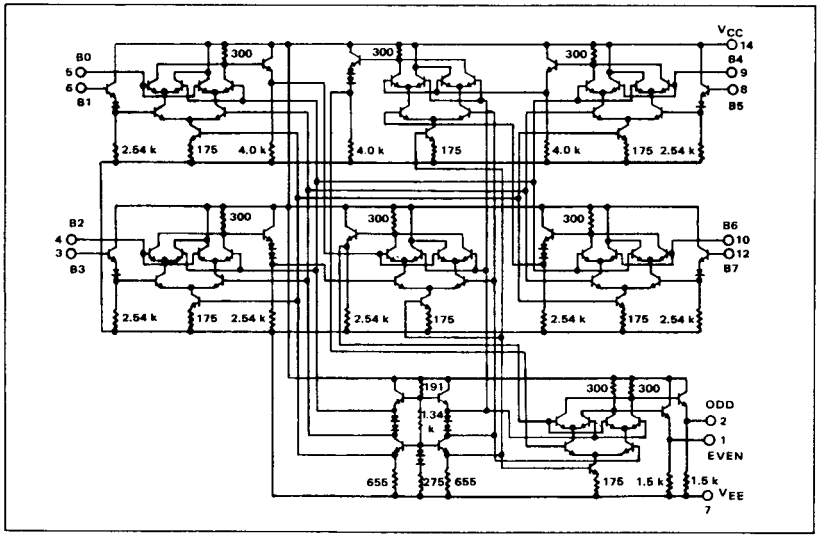
	INPUTS								OUTPUTS	
	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	ODD	EVEN
PIN NO	5	6	4	3	9	8	10	12	2	1
	0	0	0	0	0	0	0	0	0	1
	1	0	0	0	0	0	0	0	1	0
	0	1	0	0	0	0	0	0	1	0
	1	1	0	0	0	0	0	0	0	1
	ANY ODD NUMBER OF INPUTS = 1								1	0
	ANY EVEN NUMBER OF INPUTS = 1								0	1

FUNCTIONAL TRUTH TABLE*

B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	ODD	EVEN
0	0	0	0	0	0	0	0	0	1
0	1	1	0	0	1	1	1	1	0
1	0	0	1	1	1	0	1	0	1
1	0	1	1	1	0	1	0	1	0

*The Functional Truth Table is One Which Completely Exercises the Device.

CIRCUIT SCHEMATIC



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ELECTRICAL CHARACTERISTICS @ 25°C

Characteristic	Symbol	Pin Under Test	Test Limits Min	Test Limits Max	Unit	TEST VOLTAGE (Vdc)/CURRENT (mAdc) VALUES V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	V_{CC}	I_L
						-1.500	-0.850	-0.700	-5.2	Gnd	-2.5
Power Supply Drain Current	I_E	7	-	53	mAdc				3,4,5,6,7, 8,9,10,12	14	-
Input Current	*I_{in}	3,4,5,6, 8,9,10,12	-	100	µAdc			3,4,5,6, 8,9,10,12	7	14	
Input Leakage Current	*I_R	3,4,5,6, 8,9,10,12	-	1.0	µAdc				3,4,5,6,7, 8,9,10,12	14	
Logic "1" Output Voltage	**V_{OH}	1	-0.850	-0.700	Vdc	3,4,5,6, 8,9,10,12			7	14	1
		2				3,5,9	4,6,8,10,12				2
		1				4,10	3,5,6,8,9,12				1
		2				6,8,12	3,4,5,9,10				2
Logic "0" Output Voltage	V_{OL}	2	-1.800	-1.500	Vdc	3,4,5,6 8,9,10,12			7	14	
		1				3,5,9	4,6,8,10,12				-
		2				4,10	3,5,6,8,9,12				
		1				6,8,12	3,4,5,9,10				-

*Individually test each input using the pin connections shown.
**Logic "1" limits apply from no load (0 mAdc) to full load (-2.5 mAdc)

Switching Speed*** (fan-out = 15 pF)	Symbol	Pin Under Test	AC Parameters (typical)	Unit	Pulse In	Pulse Out	-4.0 Vdc V_{EE}	+1.2 Vdc V_{CC}
Propagation Delay	t_{12+2+}	2	13	ns	12	2	3, 4, 5, 6, 7, 8, 9, 10	14
	t_{12-2-}	2	14					
Rise Time	t_{2+}	2	4					
Fall Time	t_{2-}	2	6					
Propagation Delay	t_{12-1+}	1	13					
	t_{12+1-}	1	14					
Rise Time	t_{1+}	1	4					
Fall Time	t_{1-}	1	6					

***Switching speed measurements are made from the input which presents the longest delay path to the signal. Delays from all other inputs are shorter.

Pulse In: +0.450, 0 V, -0.350; t_r, t_f = 6.0 ns; f = 1 MHz (Typ); PW = Approx. 100 ns

APPLICATIONS INFORMATION

The MC1046 may be used as a parity checker-generator for EVEN or ODD parity simultaneously.

A highly versatile, can-count saving use of the MC1046 is in a Single-error Hamming Parity Code Detection and Correction circuit as shown here. A system word of 8-bits was used for simplicity in this example although any number of bits may be used.

In this 8-bit system, 4-bits of parity are generated and the 12 bit resulting word (8 message bits and 4 parity bits) is transmitted or otherwise processed. The Hamming Parity Detection circuit re-examines the input MESSAGE BITS exactly as the generator did. However, the parity bits generated at the receiver are compared with the transmitted parity bits via the high-speed MECL II MC1030 (Quad Exclusive "OR" Gate). The output Code (if the interconnections are correct) indicates, in a Binary Code, the bit which was in error. For example, if the output of the MC1030 were 8 = 0, 4 = 1, 2 = 0 and 1 = 1 (0101), the indication would be that the fifth bit was in error.

The system shown does not fully utilize the MC1046 by taking advantage of the 8 inputs and complimentary outputs. However, larger and more complex systems can more fully utilize its available input-output capability.