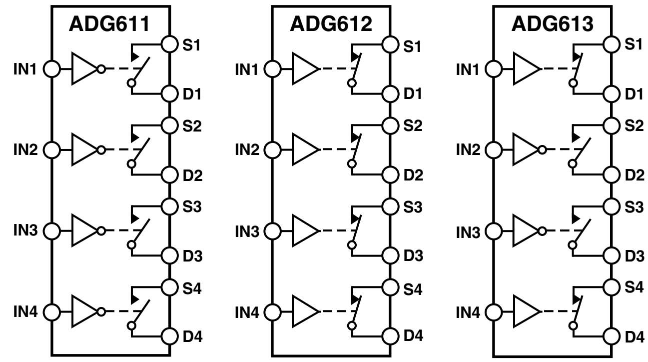
1 pC Charge Injection, 100 pA Leakage, CMOS ±5 V/+5 V/+3 V Quad SPST Switches

ADG611/ADG612/ADG613

FEATURES
1 pC Charge Injection
±2.7 V to ±5.5 V Dual Supply
+2.7 V to +5.5 V Single Supply
Automotive Temperature Range –40°C to +125°C
100 pA Max @ 25°C Leakage Currents
85 Ω On-Resistance
Rail-to-Rail Switching Operation
Fast Switching Times
16-Lead TSSOP Packages
Typical Power Consumption (<0.1 μW)
TTL/CMOS-Compatible Inputs

APPLICATIONS
Automatic Test Equipment
Data Acquisition Systems
Battery-Powered Systems
Communication Systems
Sample and Hold Systems
Audio Signal Routing
Relay Replacement
Avionics

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG611, ADG612, and ADG613 are monolithic CMOS devices containing four independently selectable switches. These switches offer ultralow charge injection of 1 pC over full input signal range and typical leakage currents of 10 pA at 25°C.

They are fully specified for ±5 V, +5 V, and +3 V supplies. They contain four independent single-pole/single-throw (SPST) switches. The ADG611 and ADG612 differ only in that the digital control logic is inverted. The ADG611 switches are turned on with a logic low on the appropriate control input, while a logic high is required to turn on the switches of the ADG612. The ADG613 contains two switches whose digital control logic is similar to the ADG611, while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON and has an input signal range that extends to the supplies. The ADG613 exhibits break-before-make switching action. The ADG611/ADG612/ADG613 are available in small 16-lead TSSOP packages.

PRODUCT HIGHLIGHTS

1. Ultralow Charge Injection (1 pC typically)
2. Dual ±2.7 V to ±5.5 V or Single +2.7 V to +5.5 V Operation.
3. Automotive Temperature Range, –40°C to +125°C
4. Small 16-lead TSSOP package.

REV. 0

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ADG611/ADG612/ADG613–SPECIFICATIONS

DUAL SUPPLY[1] (V_{DD} = +5 V ± 10%, V_{SS} = –5 V ± 10%, GND = 0 V, unless otherwise noted.)

Parameter	25°C	Y Version –40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On-Resistance (R_{ON})	85			Ω typ	V_S = ±3 V, I_S = –1 mA
	115	140	160	Ω max	Test Circuit 1
On-Resistance Match Between	2			Ω typ	
Channels (ΔR_{ON})	4	5.5	6.5	Ω max	V_S = ±3 V, I_S = –1 mA
On-Resistance Flatness ($R_{FLAT(ON)}$)	25			Ω typ	V_S = ±3 V, I_S = –1 mA
	40	55	60	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = –5.5 V
Source OFF Leakage I_S (OFF)	±0.01			nA typ	V_D = ±4.5 V, V_S = ∓4.5 V;
	±0.1	±0.25	±2	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01			nA typ	V_D = ±4.5 V, V_S = ∓4.5 V;
	±0.1	±0.25	±2	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01			nA typ	V_D = V_S = ±4.5 V, Test Circuit 3
	±0.1	±0.25	±6	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	µA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	45			ns typ	R_L = 300 Ω, C_L = 35 pF
	65	75	90	ns max	V_S = 3.0 V, Test Circuit 4
t_{OFF}	25			ns typ	R_L = 300 Ω, C_L = 35 pF
	40	45	50	ns max	V_S = 3.0 V, Test Circuit 4
Break-Before-Make Time Delay, t_D	15			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 3.0 V, Test Circuit 5
Charge Injection	–0.5			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, Test Circuit 6
Off Isolation	–65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Test Circuit 7
Channel-to-Channel Crosstalk	–90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Test Circuit 8
–3 dB Bandwidth	680			MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 9
C_S (OFF)	5			pF typ	f = 1 MHz
C_D (OFF)	5			pF typ	f = 1 MHz
C_D, C_S (ON)	5			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = –5.5 V
I_{DD}	0.001			µA typ	Digital Inputs = 0 V or 5.5 V
			1.0	µA max	
I_{SS}	0.001			µA typ	Digital Inputs = 0 V or 5.5 V
			1.0	µA max	

NOTES

[1]Temperature range is as follows. Y Version: –40°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY[1] (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.)

Parameter	Y Version 25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On-Resistance (R_{ON})	210			Ω typ	V_S = 3.5 V, I_S = –1 mA;
	290	350	380	Ω max	Test Circuit 1
On-Resistance Match Between	3			Ω typ	V_S = 3.5 V , I_S = –1 mA
Channels (ΔR_{ON})	10	12	13	Ω max	
LEAKAGE CURRENTS					V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V;
	±0.1	±0.25	±2	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V;
	±0.1	±0.25	±2	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01			nA typ	V_S = V_D = 1 V or 4.5 V, Test Circuit 3
	±0.1	±0.25	±6	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	µA max	
C_{IN}, Digital Input Capacitance[2]	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	70			ns typ	R_L = 300 Ω, C_L = 35 pF
	100	130	150	ns max	V_S = 3.0 V, Test Circuit 4
t_{OFF}	25			ns typ	R_L = 300 Ω, C_L = 35 pF
	40	45	50	ns max	V_S = 3.0 V, Test Circuit 4
Break-Before-Make Time Delay, t_D	25			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 3.0 V, Test Circuit 5
Charge Injection	1			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 6
Off Isolation	–62			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz Test Circuit 7
Channel-to-Channel Crosstalk	–90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz Test Circuit 8
–3 dB Bandwidth	680			MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 9
C_S (OFF)	5			pF typ	f = 1 MHz
C_D (OFF)	5			pF typ	f = 1 MHz
C_D, C_S (ON)	5			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 5.5 V
I_{DD}	0.001			µA typ	Digital Inputs = 0 V or 5.5 V
			1.0	µA max	

NOTES
[1]Temperature ranges are as follows. Y Version: –40°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

ADG611/ADG612/ADG613–SPECIFICATIONS

SINGLE SUPPLY[1] (V_{DD} = 3 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.)

Parameter	Y Version 25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On-Resistance (R_{ON})	380	420	460	Ω typ	V_S = 1.5 V, I_S = –1 mA; Test Circuit 1
LEAKAGE CURRENTS					V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.01			nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V;
	±0.1	±0.25	±2	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01			nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V;
	±0.1	±0.25	±2	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01			nA typ	V_S = V_D = 1 V or 3 V, Test Circuit 3
	±0.1	±0.25	±6	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	µA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	130			ns typ	R_L = 300 Ω, C_L = 35 pF
	185	230	260	ns max	V_S = 2 V, Test Circuit 4
t_{OFF}	40			ns typ	R_L = 300 Ω, C_L = 35 pF
	55	60	65	ns max	V_S = 2 V, Test Circuit 4
Break-Before-Make Time Delay, t_D	50			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 2 V, Test Circuit 5
Charge Injection	1.5			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 6
Off Isolation	–62			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz Test Circuit 7
Channel-to-Channel Crosstalk	–90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz Test Circuit 8
–3 dB Bandwidth	680			MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 9
C_S (OFF)	5			pF typ	f = 1 MHz
C_D (OFF)	5			pF typ	f = 1 MHz
C_D, C_S (ON)	5			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 3.3 V
I_{DD}	0.001			µA typ	Digital Inputs = 0 V or 3.3 V
			1.0	µA max	

NOTES
[1]Temperature ranges are as follows. Y Version: –40°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted)

V_{DD} to V_{SS} . . . . 13 V
V_{DD} to GND . . . . –0.3 V to +6.5 V
V_{SS} to GND . . . . +0.3 V to –6.5 V
Analog Inputs[2] . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
Digital Inputs[2] . . . . GND – 0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D . . . . 20 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D . . . . 10 mA
3 V operation 85°C to 125°C . . . . 7.5 mA
Operating Temperature Range
Automotive (Y Version) . . . . –40°C to +125°C
Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature . . . . 150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance . . . . 150.4°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . 215°C
Infrared (15 sec) . . . . 220°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG611YRU	–40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG612YRU	–40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG613YRU	–40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16

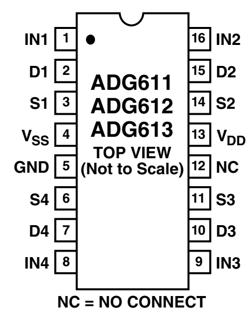
Table I. ADG611/ADG612 Truth Table

ADG611 In	ADG612 In	Switch Condition
0	1	ON
1	0	OFF

Table II. ADG613 Truth Table

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

PIN CONFIGURATIONS

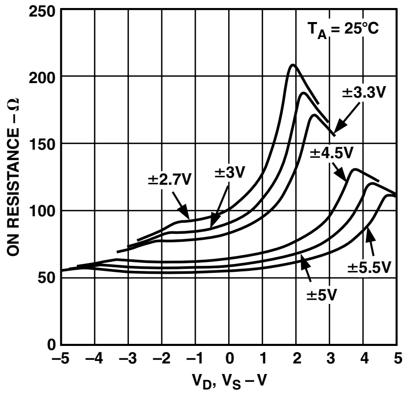


CAUTION

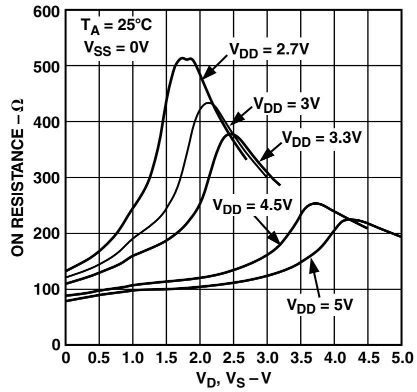
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG611/ADG612/ADG613 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

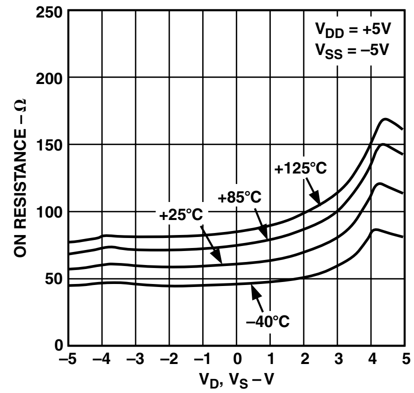
V_{DD}	Most Positive Power Supply Potential
V_{SS}	Most Negative Power Supply Potential
I_{DD}	Positive Supply Current
I_{SS}	Negative Supply Current
GND	Ground (0 V) Reference
S	Source Terminal. May be an input or output
D	Drain Terminal. May be an input or output
IN	Logic Control Input
V_D (V_S)	Analog Voltage on Terminals D, S
R_{ON}	Ohmic Resistance between D and S
ΔR_{ON}	On Resistance match between any two channels, i.e., $R_{ONMAX} - R_{ONMIN}$.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch "OFF"
I_D (OFF)	Drain Leakage Current with the Switch "OFF"
I_D, I_S (ON)	Channel Leakage Current with the Switch "ON"
V_{INL}	Maximum Input Voltage for Logic "0"
V_{INH}	Minimum Input Voltage for Logic "1"
I_{INL}(I_{INH})	Input Current of the Digital Input.
C_S (OFF)	"OFF" Switch Source Capacitance. Measured with reference to ground.
C_D (OFF)	"OFF" Switch Drain Capacitance. Measured with reference to ground.
C_D, C_S(ON)	"ON" Switch Capacitance. Measured with reference to ground.
C_{IN}	Digital Input Capacitance
t_{ON}	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
t_{OFF}	Delay between applying the digital control input and the output switching off.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
On Response	Frequency Response of the "ON" Switch
Insertion Loss	Loss Due to the ON Resistance of the Switch



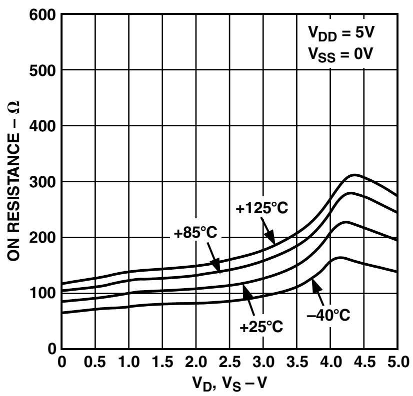
TPC 1. On Resistance vs. $V_D(V_S)$, Dual Supply



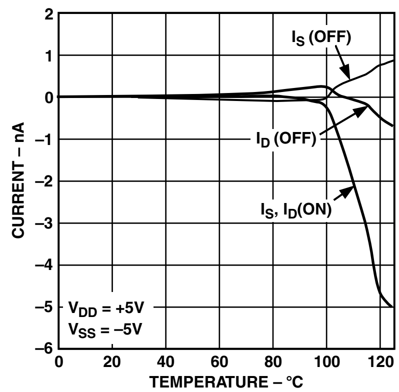
TPC 2. On Resistance vs. $V_D(V_S)$, Single Supply



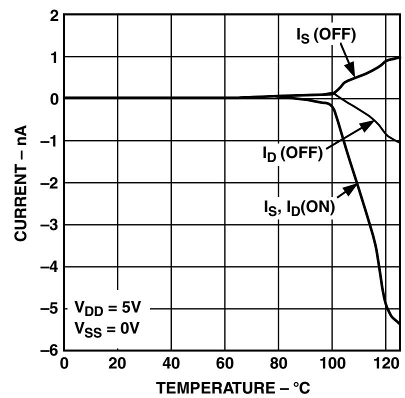
TPC 3. On Resistance vs. $V_D(V_S)$ for Different Temperatures, Dual Supply



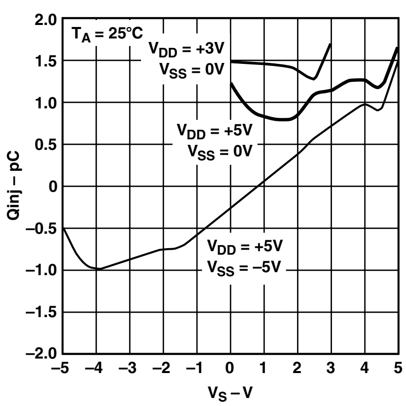
TPC 4. On Resistance vs. $V_D(V_S)$ for Different Temperatures, Single Supply



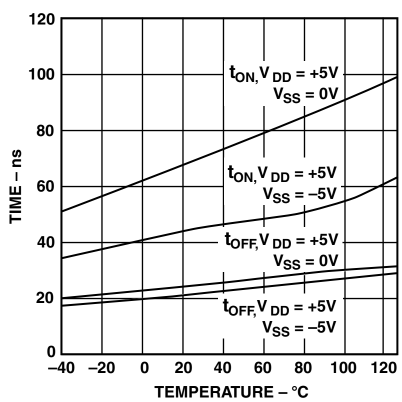
TPC 5. Leakage Currents vs. Temperature, Dual Supply



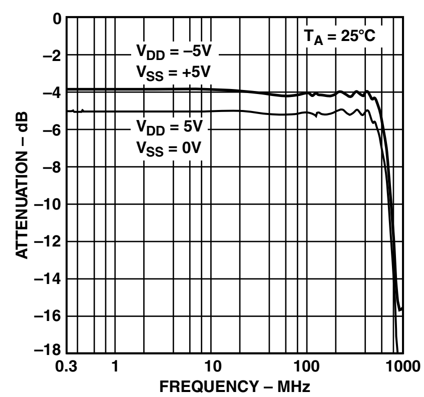
TPC 6. Leakage Currents vs. Temperature, Single Supply



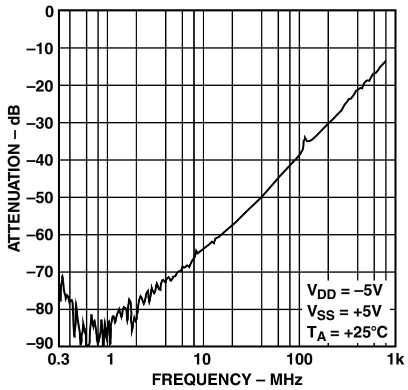
TPC 7. Charge Injection vs. Source Voltage



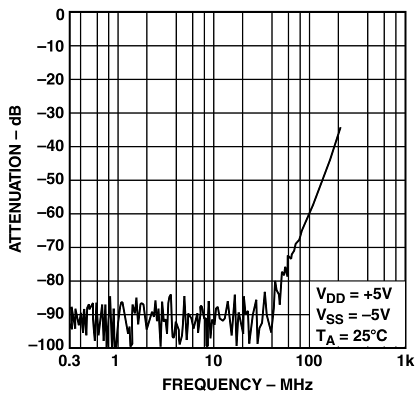
TPC 8. t_{ON}/t_{OFF} Times vs. Temperature



TPC 9. On Response vs. Frequency



TPC 10. Off Isolation vs. Frequency



TPC 11. Crosstalk vs. Frequency

APPLICATIONS

Figure 1 illustrates a photodetector circuit with programmable gain. With the resistor values shown in the circuits, and using different combinations of switches, gains in the range of 2 to 16 can be achieved.

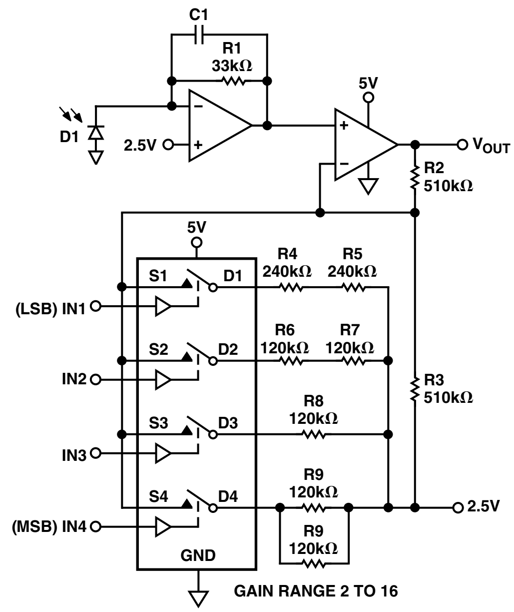
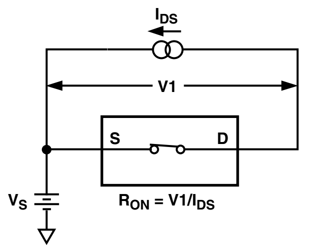
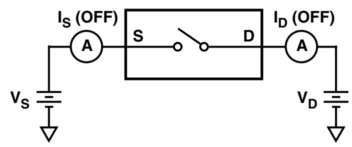


Figure 1. Photodetector Circuit with Programmable Gain

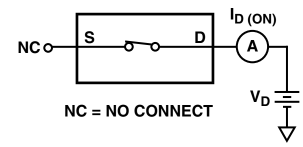
Test Circuits



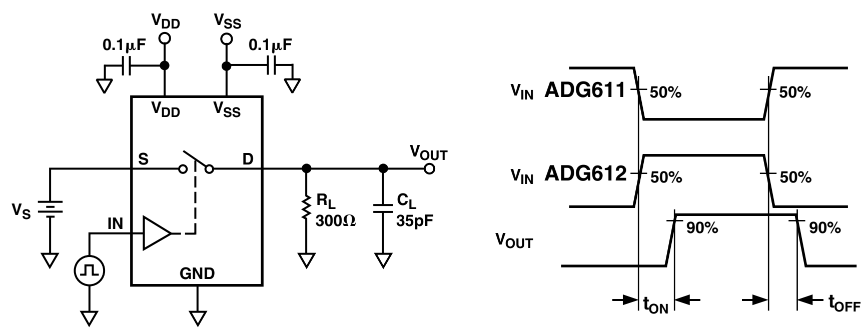
Test Circuit 1. On Resistance



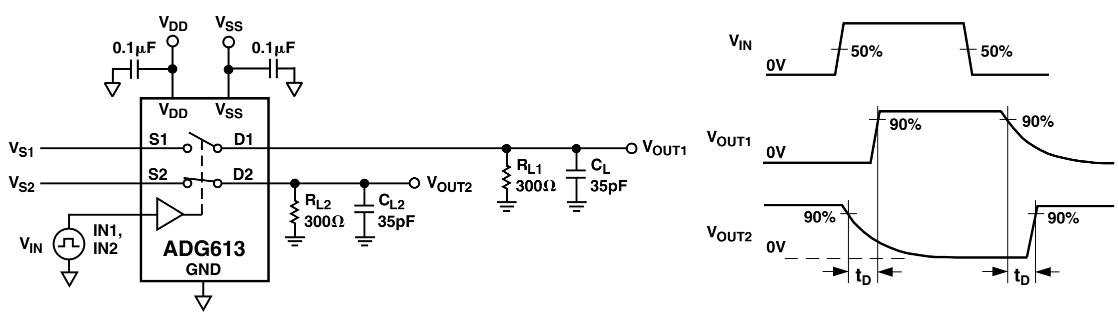
Test Circuit 2. Off Leakage



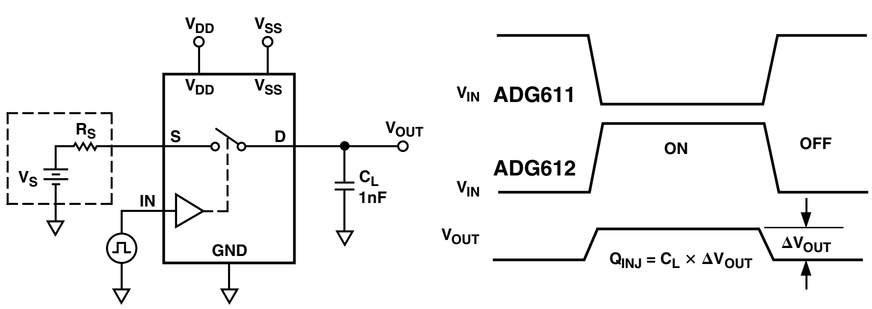
Test Circuit 3. On Leakage



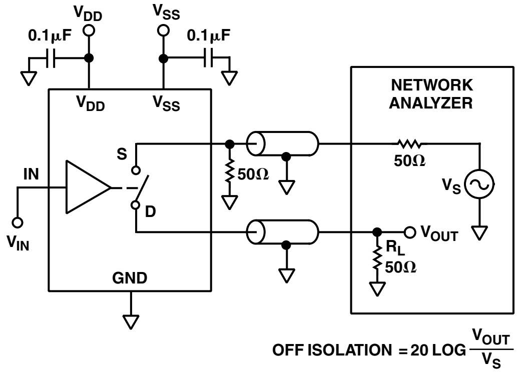
Test Circuit 4. Switching Times



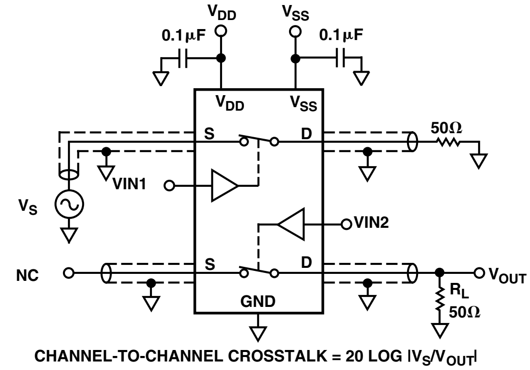
Test Circuit 5. Break-Before-Make Time Delay



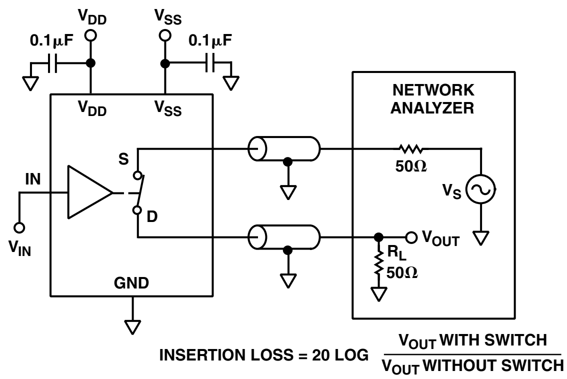
Test Circuit 6. Charge Injection



Test Circuit 7. Off Isolation



Test Circuit 8. Channel-to-Channel Crosstalk

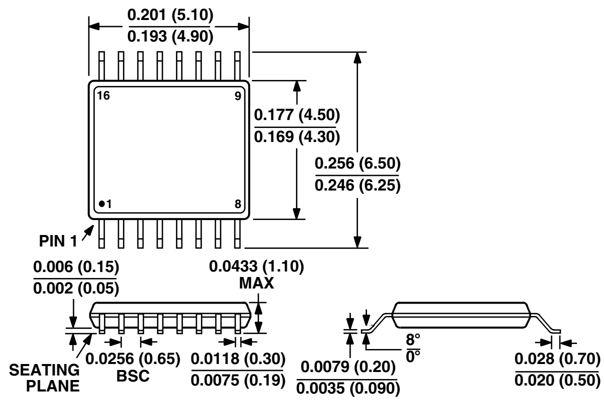


Test Circuit 9. Bandwidth

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead TSSOP (RU-16)



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