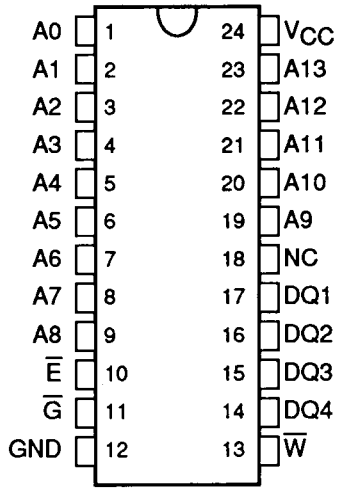
TMS6789
65,536-BIT HIGH-SPEED STATIC RANDOM-ACCESS MEMORY

MAY 1989 – REVISED JANUARY 1990

- **Organization . . . 16,384 x 4**
- **Single 5-V Power Supply (10% Tolerance)**
- **High Density 24-Pin Package**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**
  TMS6789-15 . . . 15 ns
  TMS6789-20 . . . 20 ns
  TMS6789-25 . . . 25 ns
  TMS6789-30 . . . 30 ns
- **Power Saving BiCMOS Technology**
- **3-State Output Buffers**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  — Active . . . 550 mW Worst Case
  — Standby . . . 55 mW Worst Case (CMOS Input Levels)

N and DJ Packages
Top View



description

The TMS6789 is a common I/O, 65,536-bit high-speed static random access memory organized as 16,384 words by 4 bits. The TMS6789 features maximum address access and a minimum cycle times of 15 ns, 20 ns, 25 ns, and 30 ns.

The TMS6789 is fabricated using BiCMOS technology. Maximum power dissipation is as low as 550 mW active. This reduces to a maximum of 55 mW (CMOS input levels) and 165 mW (TTL input levels) during standby operation.

PIN NOMENCLATURE	
A0-A13	Address Inputs
DQ1-DQ4	Data In - Data Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connect
V_{CC}	5-V Power Supply
$\overline{W}$	Write Enable

All inputs and outputs are compatible with Series 54/74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 54/74 TTL circuit without external resistors. The data ouputs are three-state for connecting multiple devices to a common bus.

The TMS6789 is offered in a 300-mil, 24 pin plastic dual-in-line package (N suffix) and a 24-pin plastic small outline J-lead package (DJ suffix). Both are characterized for operation from 0°C to 70°C.

operation

addresses (A0-A13)

The 14 addresses select one of the 16,384 4-bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL without external pull-up resistors.

chip enable/power down ($\overline{E}$)

The chip enable/power down terminal ($\overline{E}$) can be driven directly by standard TTL circuits, and affects the power down/deselect function of a chip. When $\overline{E}$ is high, the device is put into a reduced power standby mode. Data is retained during the standby mode.

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write enable ($\overline{W}$)

The read or write mode is selected through the write enable terminal ($\overline{W}$). A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{E}$ must be high when changing addresses to prevent inadvertently writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

output enable ($\overline{G}$)

The output enable terminal, which can be driven directly from standard TTL circuits, affects only the data out terminals. When output enable is at a logic high level, the output terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

data in/data out (DQ1-DQ4)

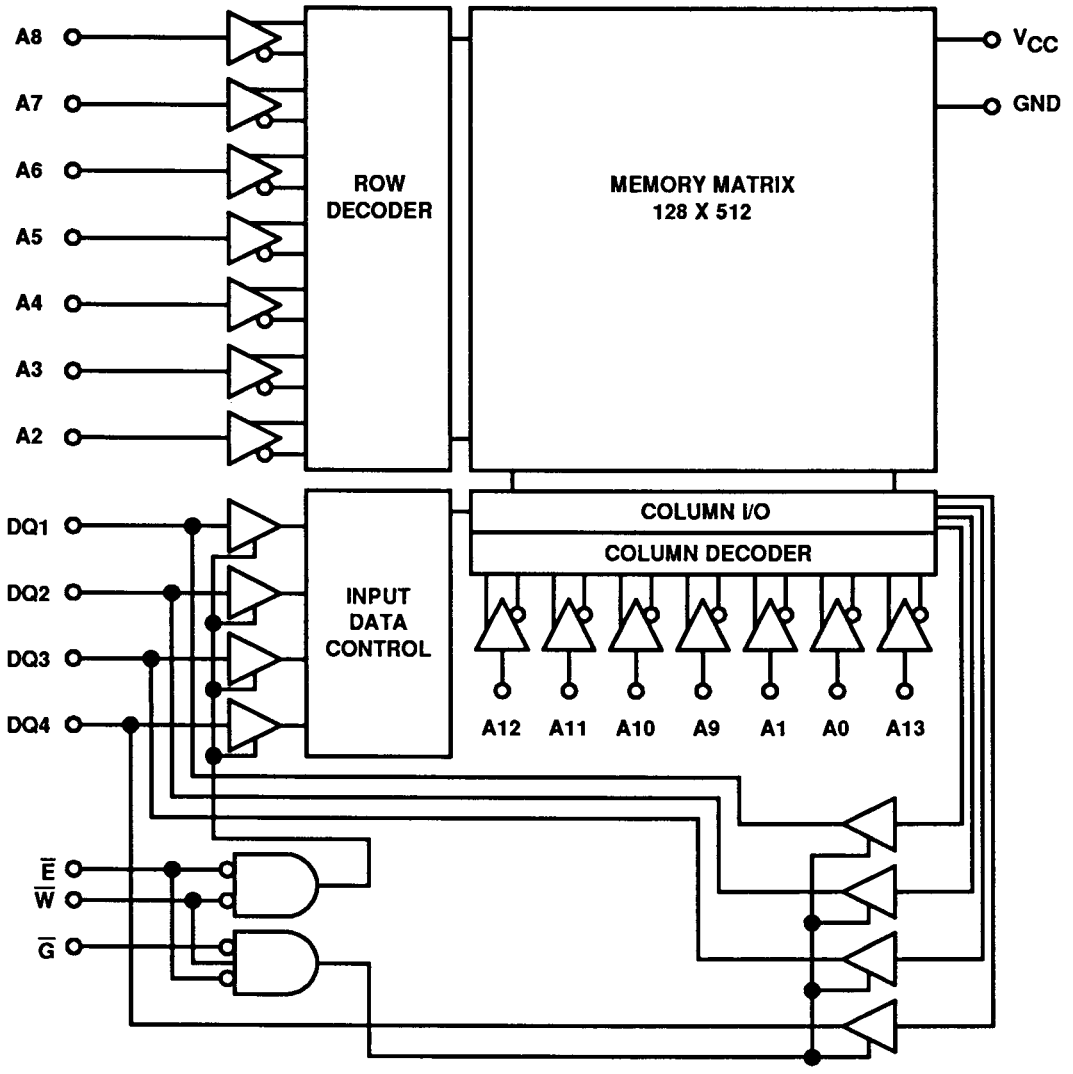
Data can be written into a selected device when write enable ($\overline{W}$) is low and chip enable ($\overline{E}$) is low. Data can be read when write enable ($\overline{W}$) is high as chip enable ($\overline{E}$) is low and output enable ($\overline{G}$) is low. The DQ terminals can be driven directly from standard TTL circuits. The three-state output buffers provide direct TTL compatibility.

function table

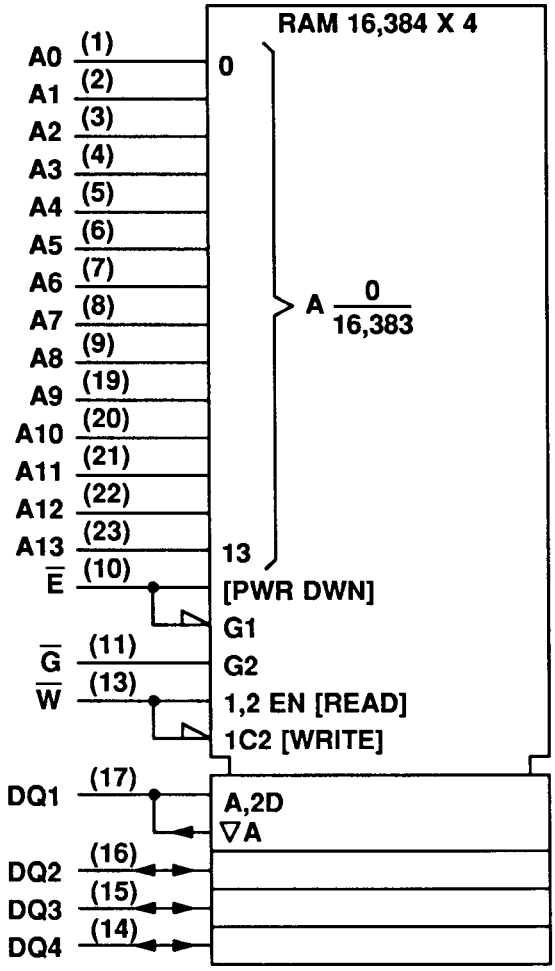
FUNCTION	MODE				
	Deselect	Read	Output Disable	Write (Write Cycles A, B, C, D)	Write (Write Cycles E, F)
$\overline{W}$	X	H	H	L	L
$\overline{E}$	H	L	L	L	L
$\overline{G}$	X	L	H	H	L
DQ1-DQ4	HI-Z	D_{OUT}	HI-Z	D_{IN}	D_{IN}

X = Don't Care

functional block diagram



logic symbol†



†Symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless other wise noted)†

Supply voltage range (see Note 1) . . . . . – 0.5 V to 7 V
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Temperature range powered down . . . . . – 10°C to 85°C
Storage temperature range . . . . . – 55°C to 125°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level Input voltage	2.2		6	V
V_{IL}	Low-level input voltage (see Note 2)	– 0.5		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The input voltage may go down to – 3 V for a maximum time interval of 10 ns.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = – 4 mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 8 mA			0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_{in} = GND to V_{CC}			2	µA
I_O	Output current (leakage)	$\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, $V_{i/o}$ = GND to V_{CC}			10	µA
I_{CC1}	Operating power supply current	$\overline{E}$ = V_{IL}, $I_{i/o}$ = 0 mA			100	mA
I_{CC2}	Average operating current	Minimum cycle, Duty 100%, $I_{i/o}$ = 0 mA			120	mA
$I_{CC(SB1)}$	Standby supply current (TTL levels)	$\overline{E}$ = V_{IH}			30	mA
$I_{CC(SB2)}$	Standby supply current (low-power CMOS levels)	$\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} – 0.2 V			10	mA

capacitance, T_A = 25°C, f = 1 MHz‡

PARAMETER		TEST CONDITION	TMS6789-15 TMS6789-20		TMS6789-25 TMS6789-30		UNIT
			MIN	MAX	MIN	MAX	
C_i	Input capacitance	V_{in} = 0 V		6		6	pF
$C_{i/o}$	Input/output capacitance	$V_{i/o}$ = 0 V		10		8	pF

‡Capacitance measurements are made on a sample basis only.

timing requirements over recommended supply voltage range and operating temperature range (read cycle) (see Note 3)

		ALT. SYMBOL	TMS6789-15		TMS6789-20		TMS6789-25		TMS6789-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	t_{RC}		15		20		25		30	ns

switching characteristics over full ranges of recommended operating conditions (read cycle) (see Note 3)

PARAMETER		ALT. SYMBOL	TMS6789-15		TMS6789-20		TMS6789-25		TMS6789-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	t_{AA}		15		20		25		30	ns
$t_{a(E)}$	Access time from $\overline{E}$	t_{ACS}		15		20		25		30	ns
$t_{a(G)}$	Access time from $\overline{G}$	t_{OE}	0	12	0	15	0	15	0	15	ns
$t_{en(E)}$	Output enable time from $\overline{E}$ (see Note 4)	t_{CLZ}	3		3		0		0		ns
$t_{en(G)}$	Output enable time from $\overline{G}$ (see Note 4)	t_{OLZ}	3		3		0		0		ns
$t_{dis(E)}$	Output disable time from $\overline{E}$ (see Note 4)	t_{CHZ}	0	6	0	8	0	10	0	12	ns
$t_{v(A)}$	Output data valid time after address change	t_{OH}	3		3		5		5		ns

NOTES: 3. Timing requirements and switching characteristics are defined under the following conditions:

Input pulse levels ..... GND to 3.0V
Input rise and fall time ..... 4 ns
Input timing reference level ..... 1.5 V ± 200 mV
Output timing reference level ..... 1.5 V ± 200 mV
Output load (including scope and jig) ..... see Figure 1

4. Transition is measured ± 200 mV from steady state voltage with specifed loading in Figure 1 Load B. This parameter is sampled and not 100% tested.

timing requirements over recommended supply voltage range and operating temperature range (write cycle) (see Note 3)

		ALT. SYMBOL	TMS6789-15		TMS6789-20		TMS6789-25		TMS6789-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time	t_{WC}	15		20		25		30		ns
$t_{su(A)}$	Address setup time	t_{AS}	0		0		0		0		ns
$t_{su(D)}$	Data setup time before write high	t_{DW}	9		12		15		20		ns
$t_{su(E)}$	Chip enable setup time	t_{CW}	10		15		20		25		ns
t_{AVWH}	Address valid time to write high	t_{AW}	10		15		20		25		ns
$t_{w(W)}$	Write pulse duration	t_{WP}	10		15		20		25		ns
$t_{rec(W)}$	Write recovery time	t_{WR}	3		3		0		0		ns
$t_{h(D)}$	Data hold time after write high	t_{DH}	0		0		5		5		ns
$t_{v(W)}$	Output data valid time after write high (see Note 4)	t_{OW}	0		0		0		0		ns

switching characteristics over full ranges of recommended operating conditions (write cycle) (see Note 3)

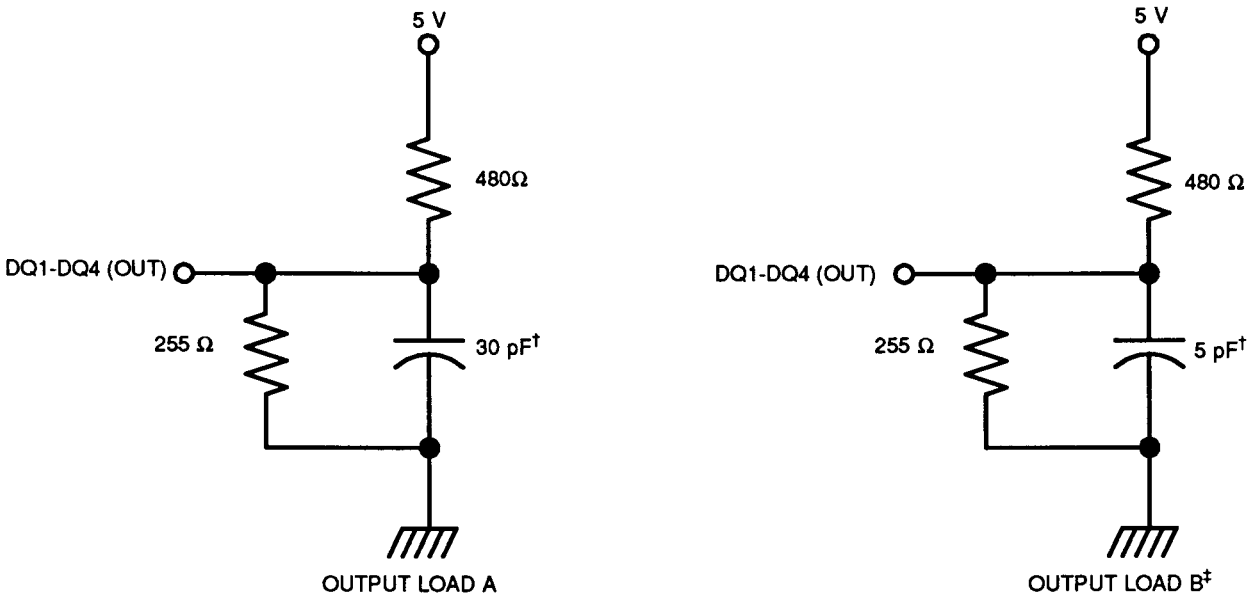
PARAMETER		ALT. SYMBOL	TMS6789-15		TMS6789-20		TMS6789-25		TMS6789-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{dis(G)}$	Output disable time from $\overline{G}$ (see Note 4)	t_{OHZ}	0	6	0	80	0	10	0	10	ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ (see Note 4)	t_{WHZ}	0	6	0	8	0	10	0	12	ns

NOTES: 3. Timing requirements and switching characteristics are defined under the following conditions:

Input pulse levels ..... GND to 3.0 V
Input rise and fall time ..... 4 ns
Input timing reference level ..... 1.5 V ± 200 mV
Output timing reference level ..... 1.5 V ± 200 mV
Output load (including scope and jig) ..... see Figure 1

4. Transition is measured ± 200 mV from steady state voltage with specifed loading in Figure 1 Load B. This parameter is sampled and not 100% tested.

PARAMETER MEASUREMENT INFORMATION

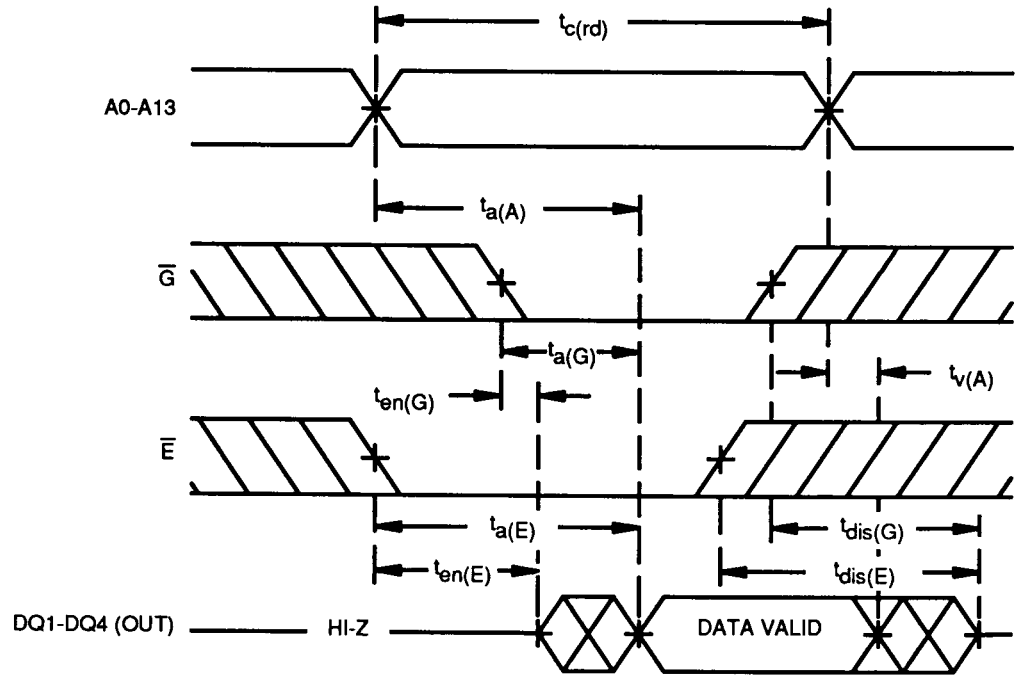


†This value includes scope and jig capacitance.

‡This output load applies for $t_{dis(E)}$, $t_{en(E)}$, $t_{dis(G)}$, $t_{en(G)}$, $t_{dis(W)}$, and $t_{v(W)}$.

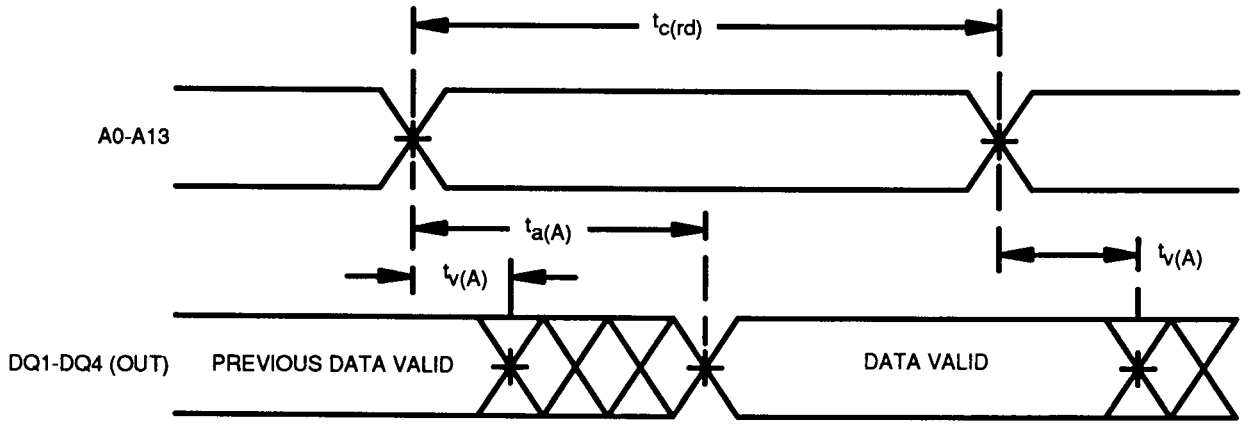
FIGURE 1. OUTPUT LOAD CIRCUIT

read cycle timing (type A)



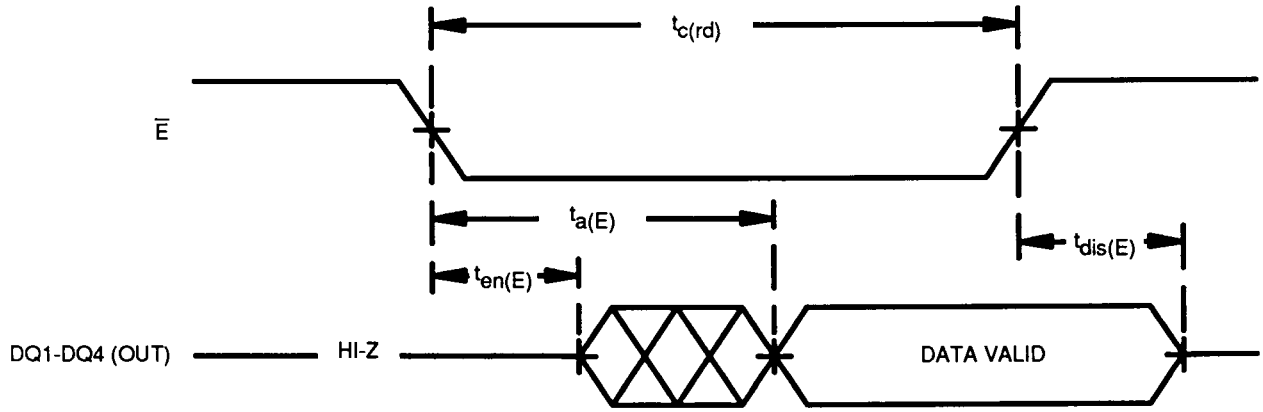
NOTE 5: $\overline{W}$ is high during the read cycle.

read cycle timing (type B)



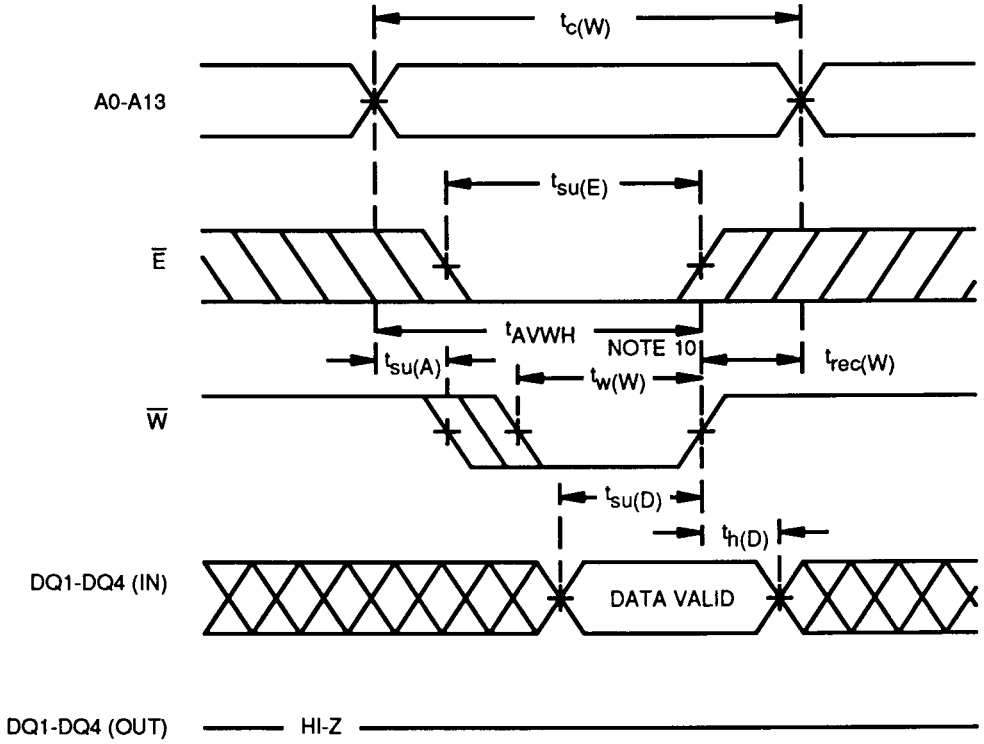
NOTES: 5. $\overline{W}$ is high during the read cycle.
6. $\overline{E}$ is low during the read cycle.
7. $\overline{G}$ is low during the read cycle.

read cycle timing (type C)



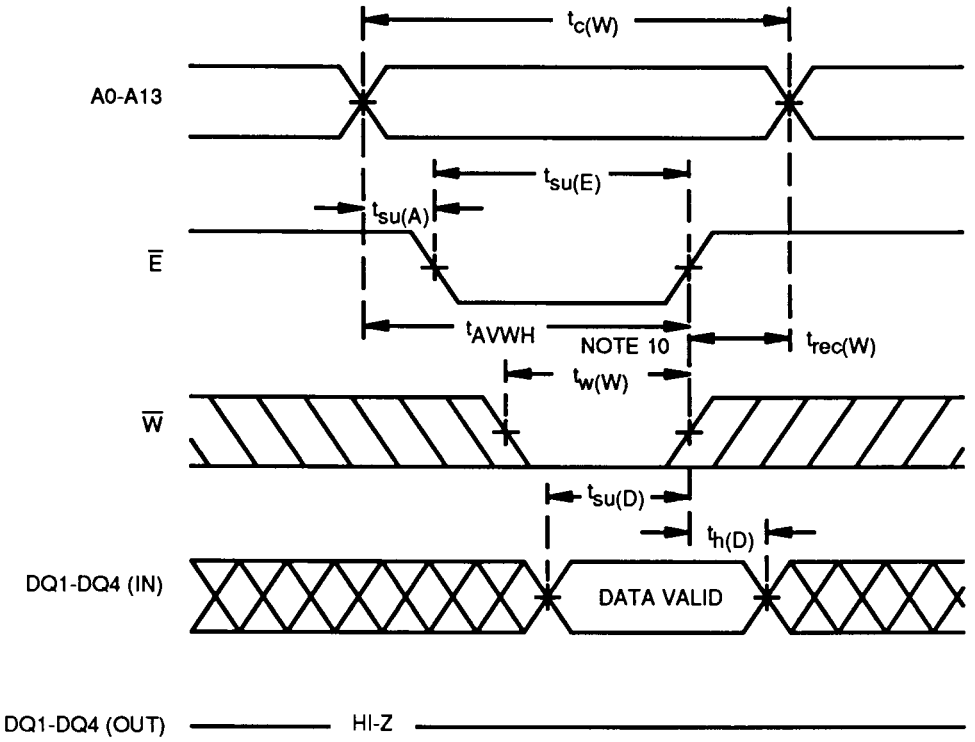
NOTES: 5. $\overline{W}$ is high during the read cycle..
7. $\overline{G}$ is low during the read cycle.
8. Address is valid prior to or at the same time $\overline{E}$ goes low.

write cycle timing ($\overline{W}$ controlled)



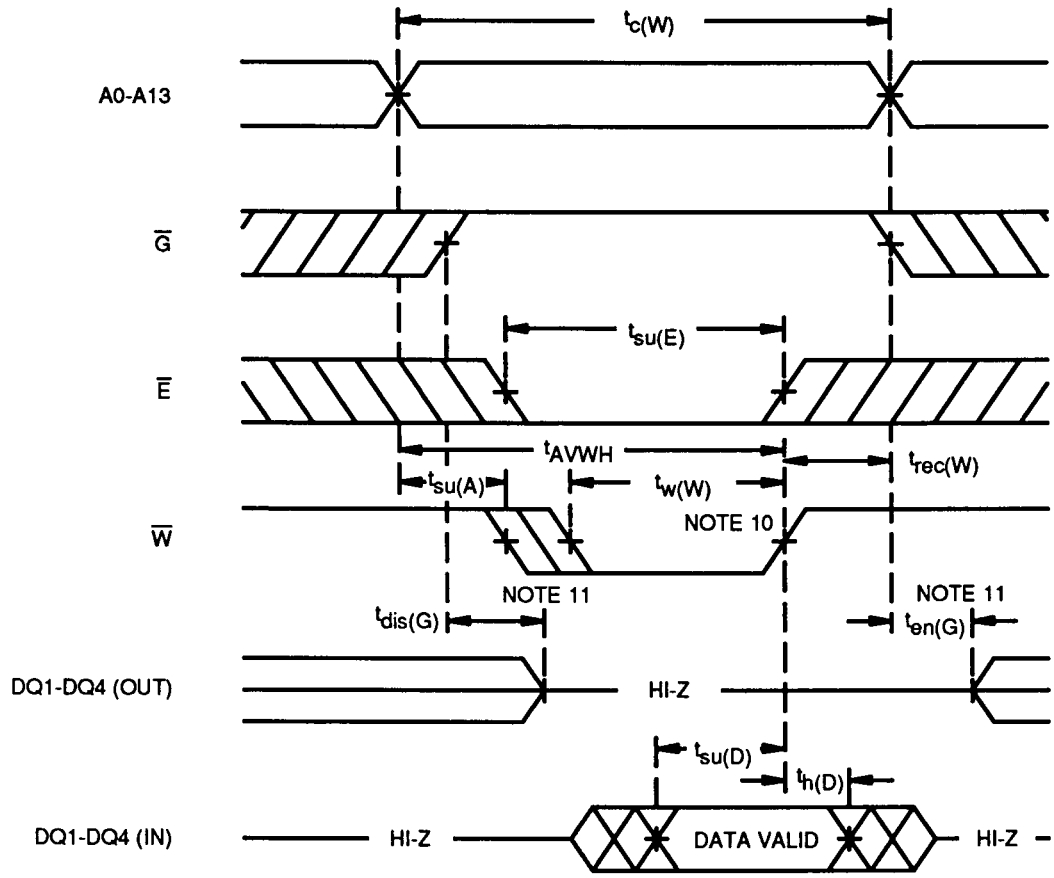
NOTES: 9. $\overline{G}$ is high during the write cycle.
10. A write occurs during the overlap of a low $\overline{E}$ and a low $\overline{W}$ ($t_{w(W)}$).

write cycle timing ($\overline{E}$ controlled)



NOTES: 9. $\overline{G}$ is high during the write cycle.
10. A write occurs during the overlap of a low $\overline{E}$ and a low $\overline{W}$ ($t_{w(W)}$).

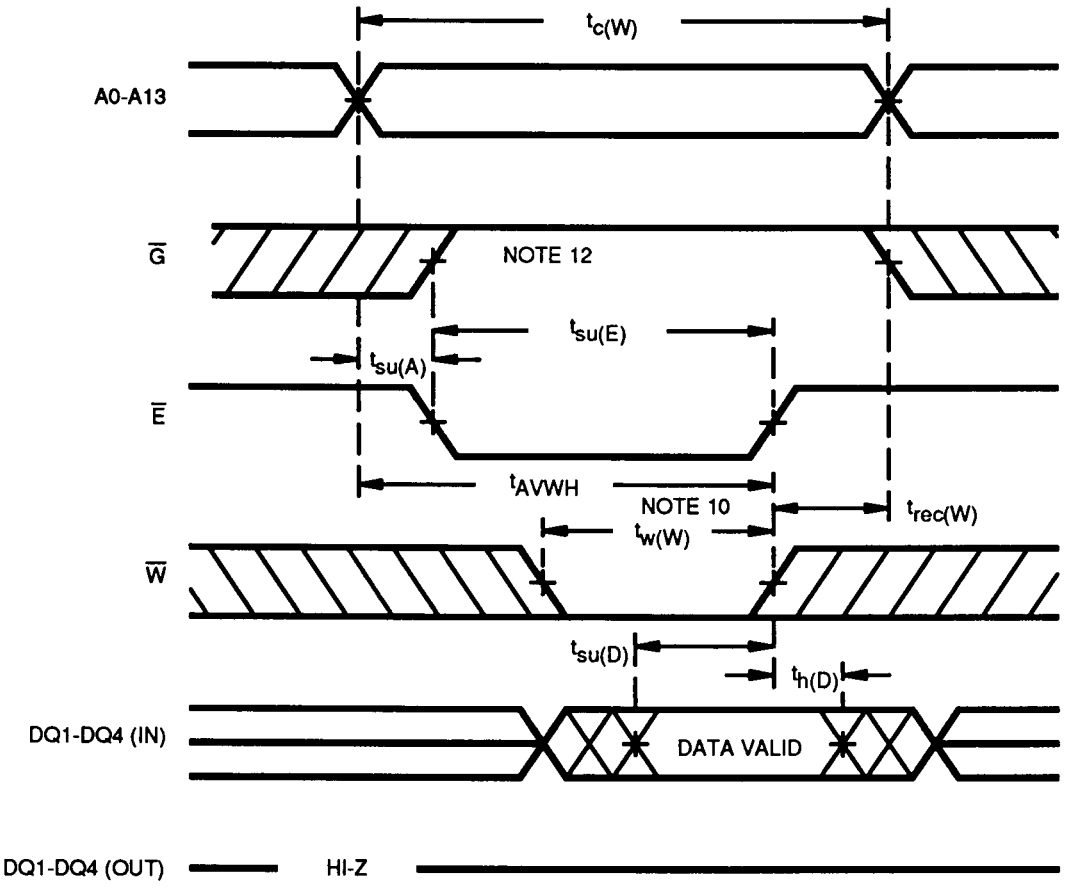
write cycle timing ($\overline{G}$ clocked, $\overline{W}$ controlled)



NOTES: 10. A write occurs during the overlap of a low $\overline{E}$ and a low $\overline{W}$ ($t_{w(W)}$).

11. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.

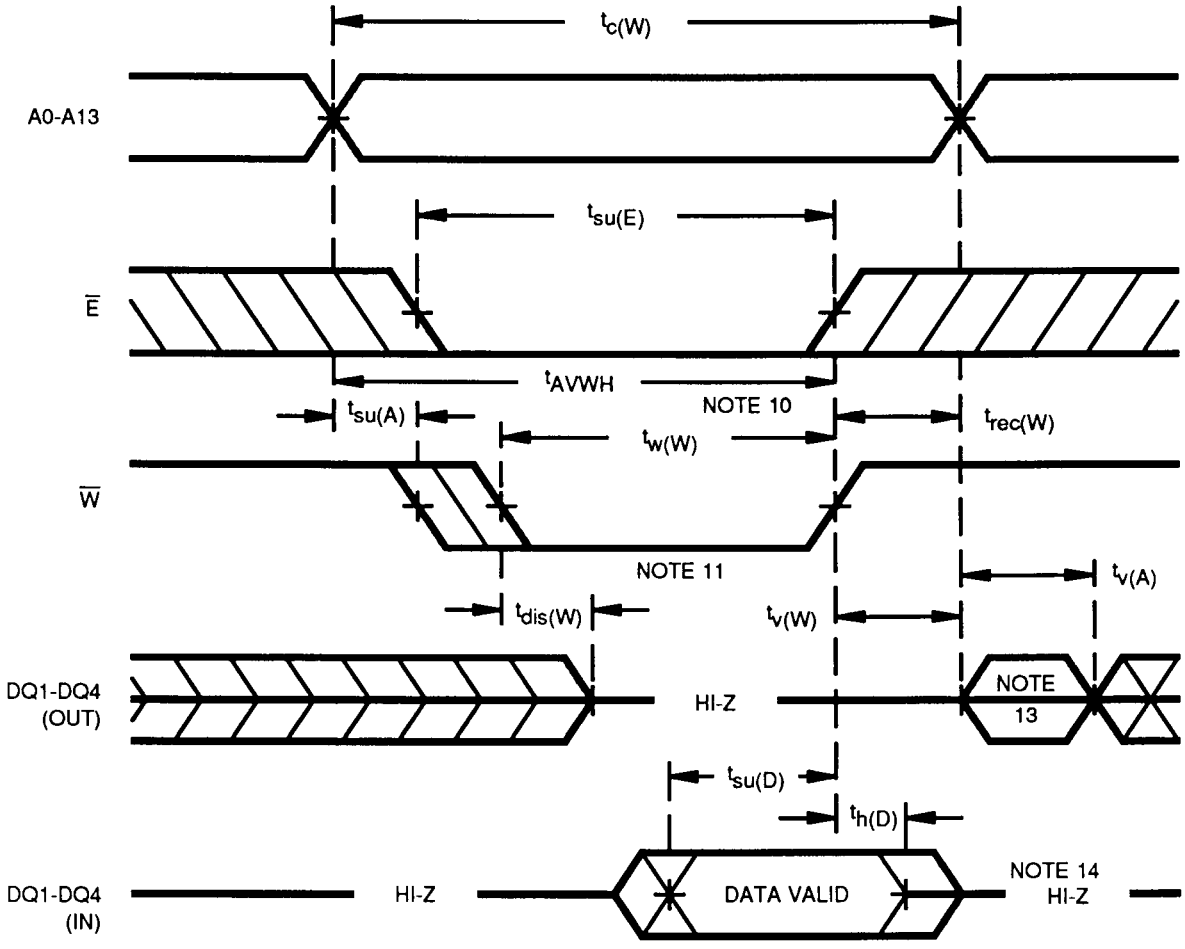
write cycle timing ($\overline{G}$ clocked, $\overline{E}$ controlled)



NOTES: 10. A write occurs during the overlap of a low $\overline{E}$ and a low $\overline{W}$ ($t_{w(W)}$).

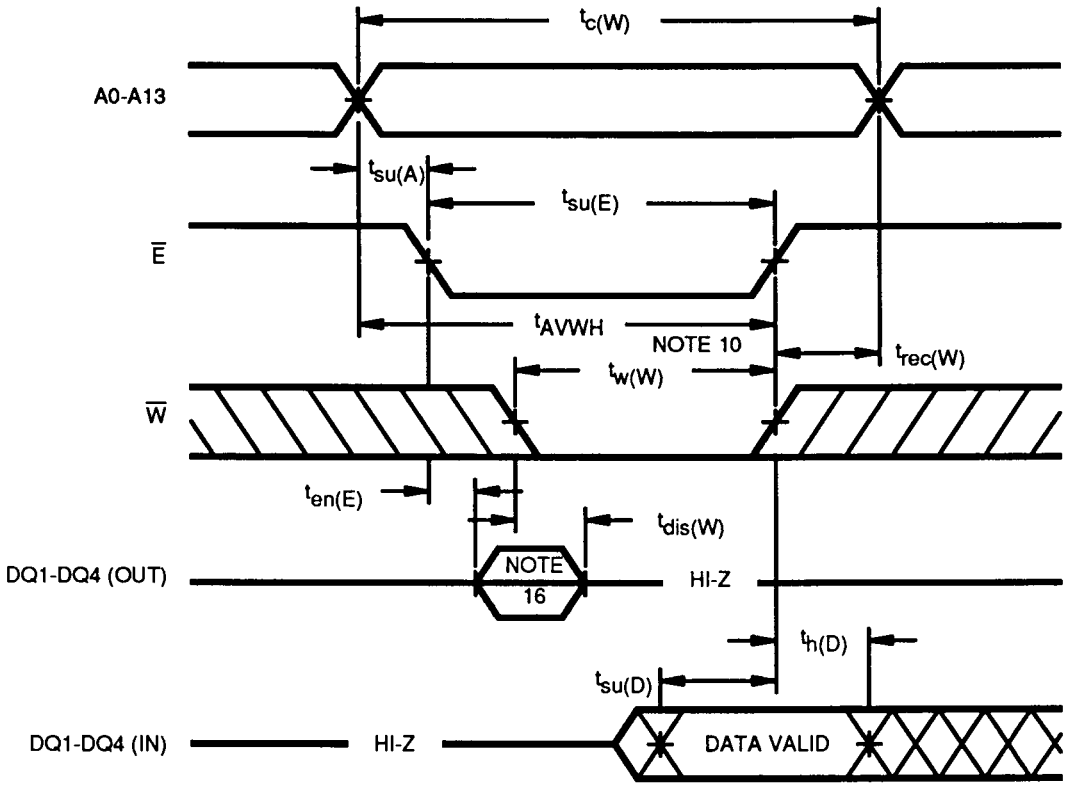
12. If the $\overline{E}$ low transition occurs simultaneously with the $\overline{W}$ low transition or after the $\overline{W}$ transition, output remains in a high-impedance state.

write cycle timing ($\overline{W}$ controlled)



NOTES: 10. A write occurs during the overlap of a low $\overline{E}$ and a low $\overline{W}$ ($t_{w(W)}$).
11. During this period, I/O pins are in the output state. The input signal out of phase must not be applied.
13. DQ1-DQ4 (OUT) is in the same phase as write data in this write cycle.
14. If $\overline{E}$ is low during this period, I/O pins are in the output state. Then the data input signals of the opposite phase to the outputs must not be applied.
15. $\overline{G}$ is low during the write cycle.

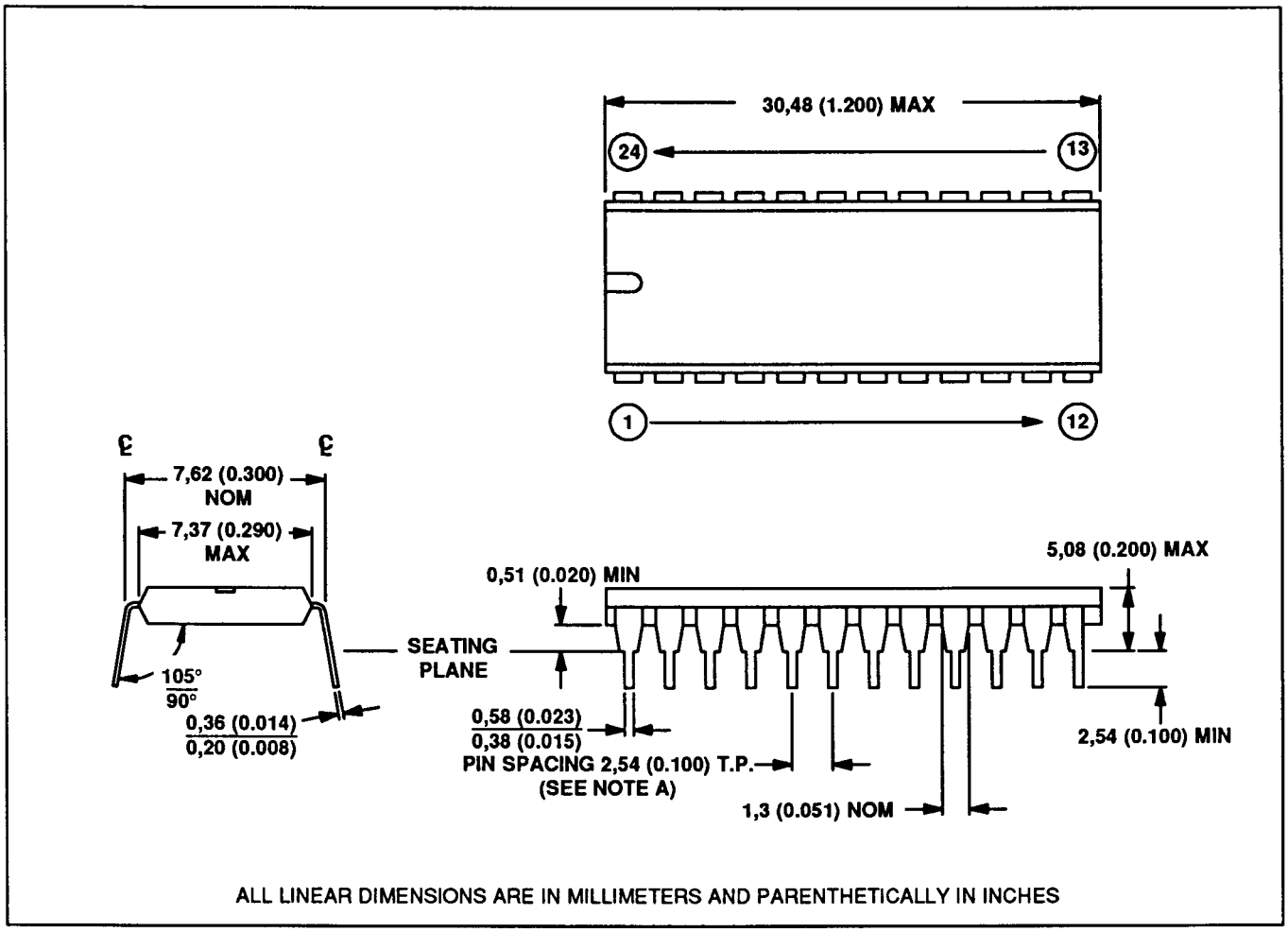
write cycle timing ($\overline{E}$ controlled)



NOTES: 10. A write occurs during the overlap of a low $\overline{E}$ and a low $\overline{W}$ ($t_{w(W)}$).
15. $\overline{G}$ is low during the write cycle.
16. If the $\overline{E}$ low transition occurs after $\overline{W}$ low transition, output remains in a high-impedance state.

MECHANICAL DATA

24-pin N plastic 300-mil package

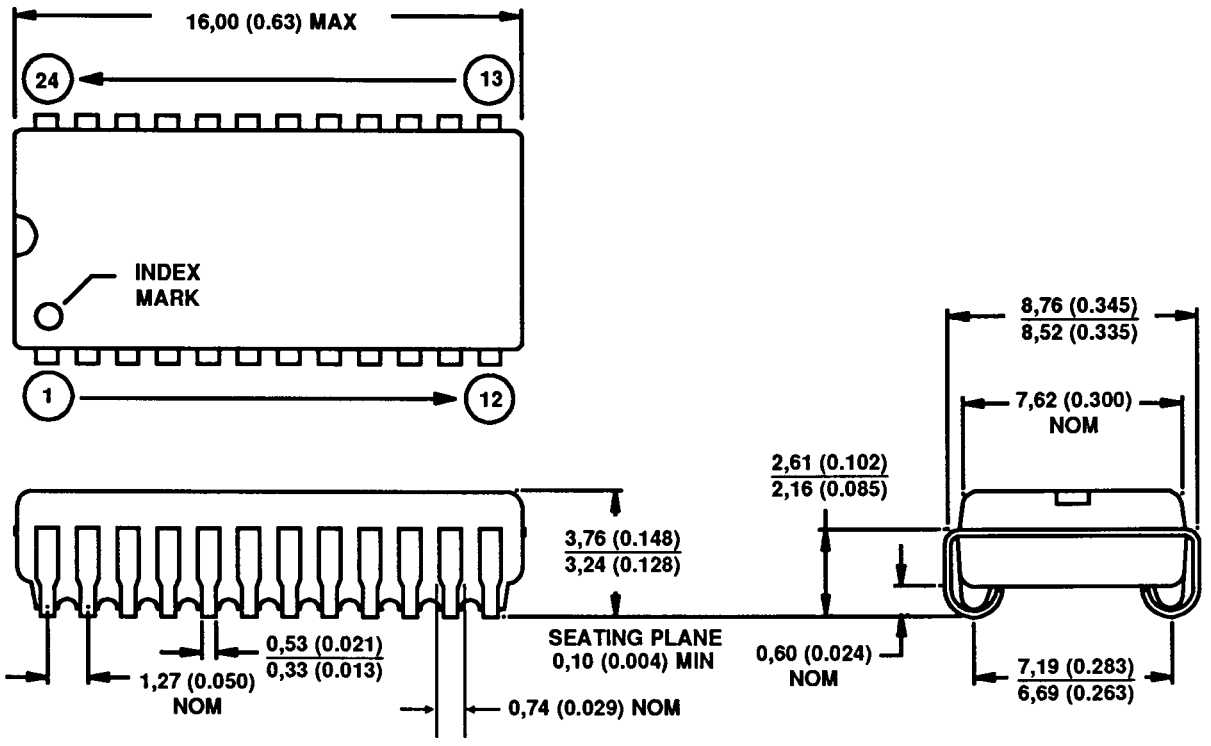


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

MECHANICAL DATA

24-pin small outline J-lead surface mount package (DJ Suffix)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES