

74VCXH245 Low Voltage Bidirectional Transceiver with Bushold

General Description

The VCXH245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The T/R input determines the direction of data flow. The OE input disables both the A and B Ports by placing them in a high impedance state. The VCXH245 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

The 74VCXH245 is designed for low voltage (1.2V to 3.6V) V_{CC} applications.

The 74VCXH245 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

Features

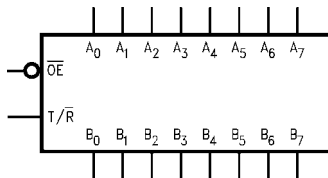
- 1.2V to 3.6V V_{CC} supply operation
- Bushold on data inputs eliminates the need for external pull-up/pull-down resistors
- t_{PD}
3.5 ns max for 3.0V to 3.6V V_{CC}
- Static Drive (I_{OH}/I_{OL})
 ± 24 mA @ 3.0V V_{CC}
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
Human body model > 2000V
Machine model > 200V

Ordering Code:

Order Number	Package Number	Package Description
74VCXH245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VCXH245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

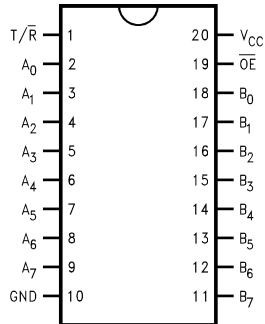


Pin Descriptions

Pin Names	Description
OE	Output Enable Input (Active LOW)
T/R	Transmit/Receive Input
A ₀ -A ₇	Side A Bushold Inputs or 3-STATE Outputs
B ₀ -B ₇	Side B Bushold Inputs or 3-STATE Outputs

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Connection Diagram

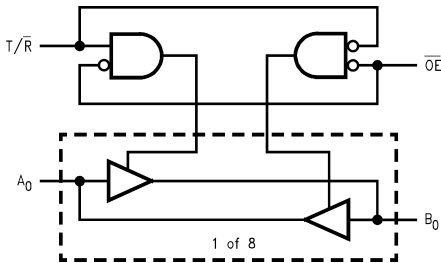


Truth Table

Inputs		Outputs
\overline{OE}	T/\overline{R}	
L	L	Bus B ₀ -B ₇ Data to Bus A ₀ -A ₇
L	H	Bus A ₀ -A ₇ Data to Bus B ₀ -B ₇
H	X	HIGH Z State on A ₀ -A ₇ , B ₀ -B ₇

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to +4.6V
DC Output Voltage (V_O)	
Outputs 3-STATE	-0.5V to +4.6V
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or Ground Current	± 100 mA
Storage Temperature (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 3)

Power Supply	
Operating	1.2V to 3.6V
Input Voltage	-0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0V to 3.6V
Output Current in I_{OH}/I_{OL}	
$V_{CC} = 3.0V$ to 3.6V	± 24 mA
$V_{CC} = 2.3V$ to 2.7V	± 18 mA
$V_{CC} = 1.65V$ to 2.3V	± 6 mA
$V_{CC} = 1.4V$ to 1.65V	± 2 mA
$V_{CC} = 1.2V$	± 100 μA
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Note 3: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6 2.3 - 2.7 1.65 - 2.3 1.4 - 1.6 1.2	2.0 1.6 $0.65 \times V_{CC}$ $0.65 \times V_{CC}$ $0.65 \times V_{CC}$		V
V_{IL}	LOW Level Input Voltage		2.7 - 3.6 2.3 - 2.7 1.65 - 2.3 1.4 - 1.6 1.2		0.8 0.7 $0.35 \times V_{CC}$ $0.35 \times V_{CC}$ $0.05 \times V_{CC}$	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -12$ mA $I_{OH} = -18$ mA $I_{OH} = -24$ mA	2.7 - 3.6 2.7 3.0 3.0	$V_{CC} - 0.2$ 2.2 2.4 2.2		V
		$I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA $I_{OH} = -12$ mA $I_{OH} = -18$ mA	2.3 - 2.7 2.3 2.3 2.3	$V_{CC} - 0.2$ 2.0 1.8 1.7		
		$I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA	1.65 - 2.3 1.65	$V_{CC} - 0.2$ 1.25		
		$I_{OH} = -100 \mu A$ $I_{OH} = -2$ mA	1.4 - 1.6 1.4	$V_{CC} - 0.2$ 1.05		
		$I_{OH} = -100 \mu A$	1.2	$V_{CC} - 0.2$		

DC Electrical Characteristics (Continued)							
Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units	
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.7 - 3.6		0.2	V	
		I _{OL} = 12 mA	2.7		0.4		
		I _{OL} = 18 mA	3.0		0.4		
		I _{OL} = 24 mA	3.0		0.55		
		I _{OL} = 100 μA	2.3 - 2.7		0.2		
		I _{OL} = 12 mA	2.3		0.4		
		I _{OL} = 18 mA	2.3		0.6		
		I _{OL} = 100 μA	1.65 - 2.3		0.2		
		I _{OL} = 6 mA	1.65		0.3		
I _I	Input Leakage Current	V _{IN} = V _{CC} or GND	1.2 - 3.6		±5.0	μA	
		I _{I(HOLD)}	Bushold Input Minimum Drive Hold Current	V _{IN} = 0.8V	3.0	75.0	μA
				V _{IN} = 2.0V	3.0	-75.0	
V _{IN} = 0.7V	2.3	45.0					
V _{IN} = 1.6V	2.3	-45.0					
V _{IN} = 0.57V	1.65	25.0					
V _{IN} = 1.07V	1.65	-25.0					
I _{I(OD)}	Bushold Input Over-Drive Current to Change State	(Note 4)	3.6	450	μA		
		(Note 5)	3.6	-450			
		(Note 4)	2.7	300			
		(Note 5)	2.7	-300			
		(Note 4)	1.95	200			
I _{OZ}	3-STATE Output Leakage	V _O = V _{CC} or GND	1.2 - 3.6		±10.0	μA	
		V _I = V _{IH} or V _{IL}					
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	1.2 - 3.6		20.0	μA	
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.7 - 3.6		750	μA	
<p>Note 4: An external driver must source at least the specified current to switch from LOW-to-HIGH.</p> <p>Note 5: An external driver must sink at least the specified current to switch from HIGH-to-LOW.</p>							

AC Electrical Characteristics (Note 6)							
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units	Figure Number
				Min	Max		
t _{PHL} , t _{PLH}	Propagation Delay A _n to B _n or B _n to A _n	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	3.5	ns	Figures 1, 2
			2.5 ± 0.2	0.8	4.2		
			1.8 ± 0.15	1.5	8.4		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	16.8		Figures 5, 6
			1.2		42.0		
t _{PZL} , t _{PZH}	Output Enable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	4.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	5.6		
			1.8 ± 0.15	1.5	9.8		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 5, 7, 8
			1.2		49.0		
t _{PLZ} , t _{PHZ}	Output Disable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	3.6	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	4.0		
			1.8 ± 0.15	1.5	7.2		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	14.4		Figures 5, 7, 8
			1.2		36.0		
t _{OSSL} , t _{OSLH}	Output to Output Skew (Note 7)	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1		1.5		
			1.2		1.5		

Note 6: For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8 2.5 3.3	0.3 0.7 1.0	V
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8 2.5 3.3	-0.3 -0.7 -1.0	V
V _{OHV}	Quiet Output Dynamic Valley V _{OH}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8 2.5 3.3	1.3 1.7 2.0	V

Capacitance

Symbol	Parameter	Conditions	T _A = +25°C	Units
			Typical	
C _{IN}	Input Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	6	pF
C _{I/O}	Input/Output Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	7	pF
C _{PD}	Power Dissipation Capacitance	V _I = 0V or V _{CC} , f = 10 MHz, V _{CC} = 1.8V, 2.5V or 3.3V	20	pF

AC Loading and Waveforms (V_{CC} 3.3V ± 0.3V to 1.8V ± 0.5V)

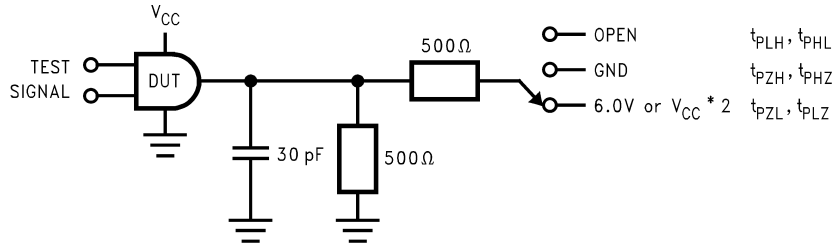


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5V \pm 0.2V$; $1.8V \pm 0.15V$
t_{PZH} , t_{PHZ}	GND

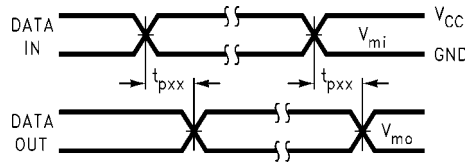


FIGURE 2. Waveform for Inverting and Non-inverting Functions

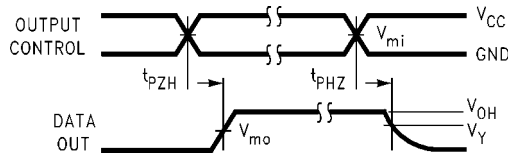


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

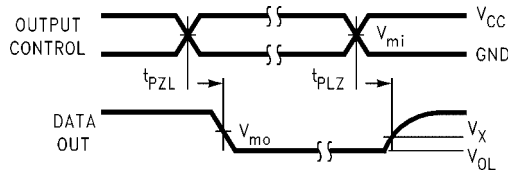


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

AC Loading and Waveforms ($V_{CC} 1.5V \pm 0.1V$ to $1.2V$)

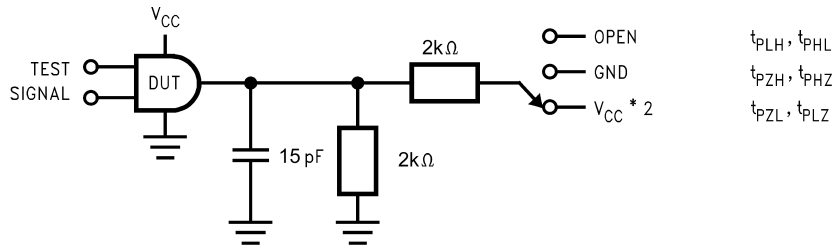


FIGURE 5. AC Test Circuit

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$V_{CC} \times 2$ at $V_{CC} = 1.5 \pm 0.1V$
t_{PZH}, t_{PHZ}	GND

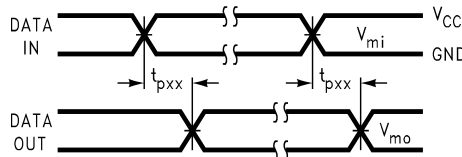


FIGURE 6. Waveform for Inverting and Non-Inverting Functions

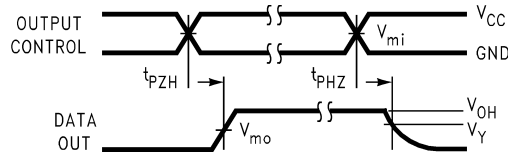


FIGURE 7. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

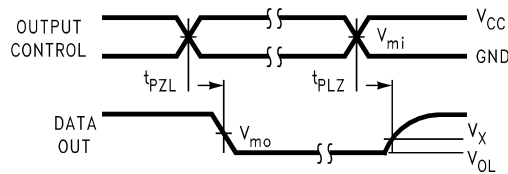
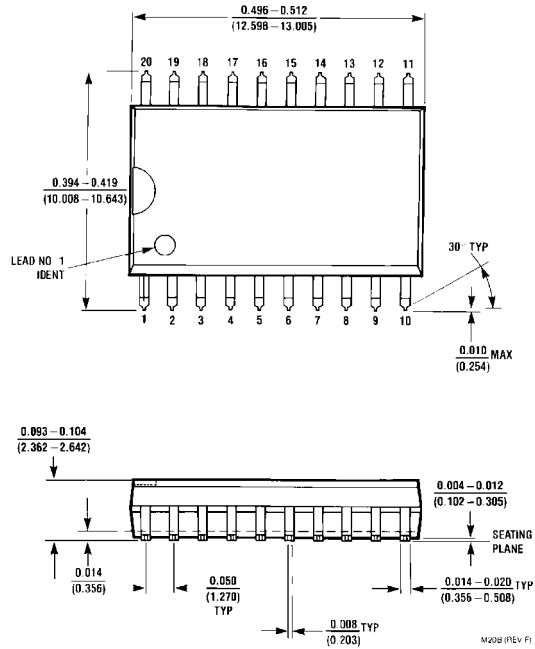


FIGURE 8. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

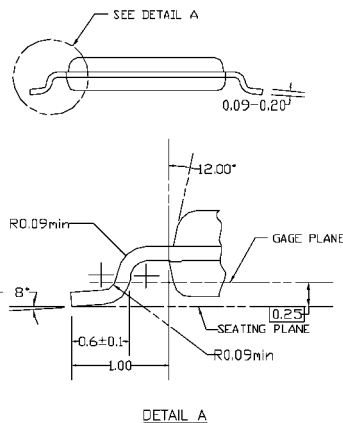
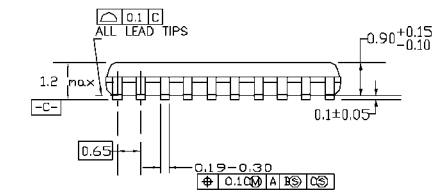
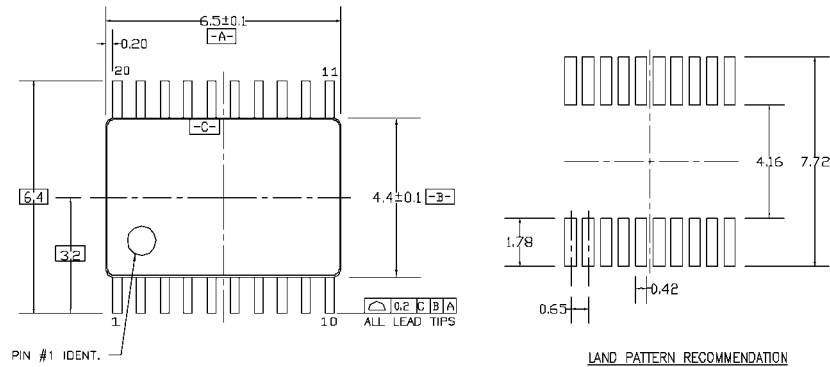
Symbol	V_{CC}
	$1.5V \pm 0.1V$
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$
V_X	$V_{OL} + 0.1V$
V_Y	$V_{OH} - 0.1V$

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit, JEDEC MS-013, 0.300" Wide Body
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

**20-Lead Thin Shrink Small Outline Package, JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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