August 2014

FAN21SV06 — TinyBuck™
6 A, 24V Single-Input Integrated Synchronous Buck Regulator with Synchronization Capability

Features

- Single-Supply Operation with 6 A Output Current
- Over 94% Efficiency
- Fully Synchronous Operation with Integrated Schottky Diode on Low-Side MOSFET Boosts Efficiency
- Single Supply Device for V_{IN} > 6.5 V – 24 V
- Programmable Frequency Operation (200-600 KHz)
- Externally Synchronizable Clock with Master/Slave Provisions
- Wide Input Range with Dual Supply: 3.0 V to 24 V
- Output Voltage Range: 0.8 V to 80%V_{IN}
- Power-Good Signal
- Accepts Ceramic Capacitors on Output
- External Compensation for Flexible Design
- Starts Up on Pre-Bias Outputs
- Integrated Bootstrap Diode
- Programmable Over-Current Protection
- Under-Voltage, Over-Voltage, and Thermal-Shutdown Protections
- 5 x 6 mm, 25-pin, 3-pad MLP

Applications

- Servers & Telecom
- Graphics Cards & Displays
- High-End Computing Systems
- Set-Top Boxes & Game Consoles
- Point-of-Load Regulation

Description

The FAN210SV06 TinyBuck™ is a highly efficient, small-footprint, programmable-frequency, 6 A integrated synchronous buck regulator.

FAN21SV06 contains both synchronous MOSFETs and a controller/driver with optimized interconnects in one package, which enables designers to solve high-current requirements in a small area with minimal external components, thereby saving cost. On-board internal 5 V regulator enables single-supply operation for input voltages >6.5 V.

The FAN21SV06 can be configured to drive multiple slave devices OR synchronize to an external system clock. In slave mode, FAN21SV06 may be set up to be free-running in the absence of a master clock signal.

External compensation, programmable switching frequency, and current-limit features allow for design optimization and flexibility. High-frequency operation allows for all ceramic solutions.

Fairchild's advanced BiCMOS power process combined with low-$R_{DS(ON)}$ internal MOSFETs and a thermally efficient MLP package provide the ability to dissipate high power in a small package. Integration helps to minimize critical inductances making layout simpler and more efficient compared to discrete solutions.

Output over-voltage, under-voltage, over-current and thermal-shutdown protections help protect the device from damage during fault conditions. FAN21SV06 prevents pre-biased output discharge during startup in point-of-load applications.

Related Resources

- *TinyCalc™ Calculator Design Tool* *AN-6033 — FAN21SV06 Design Guide*
- *AN-8022 — TinyCalc™ Calculator*

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN21SV06MPX	-10°C to 85°C	Molded Leadless Package (MLP) 5 x 6 mm	Tape and Reel
FAN21SV06EMPX	-40°C to 85°C		

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Typical Application Diagram

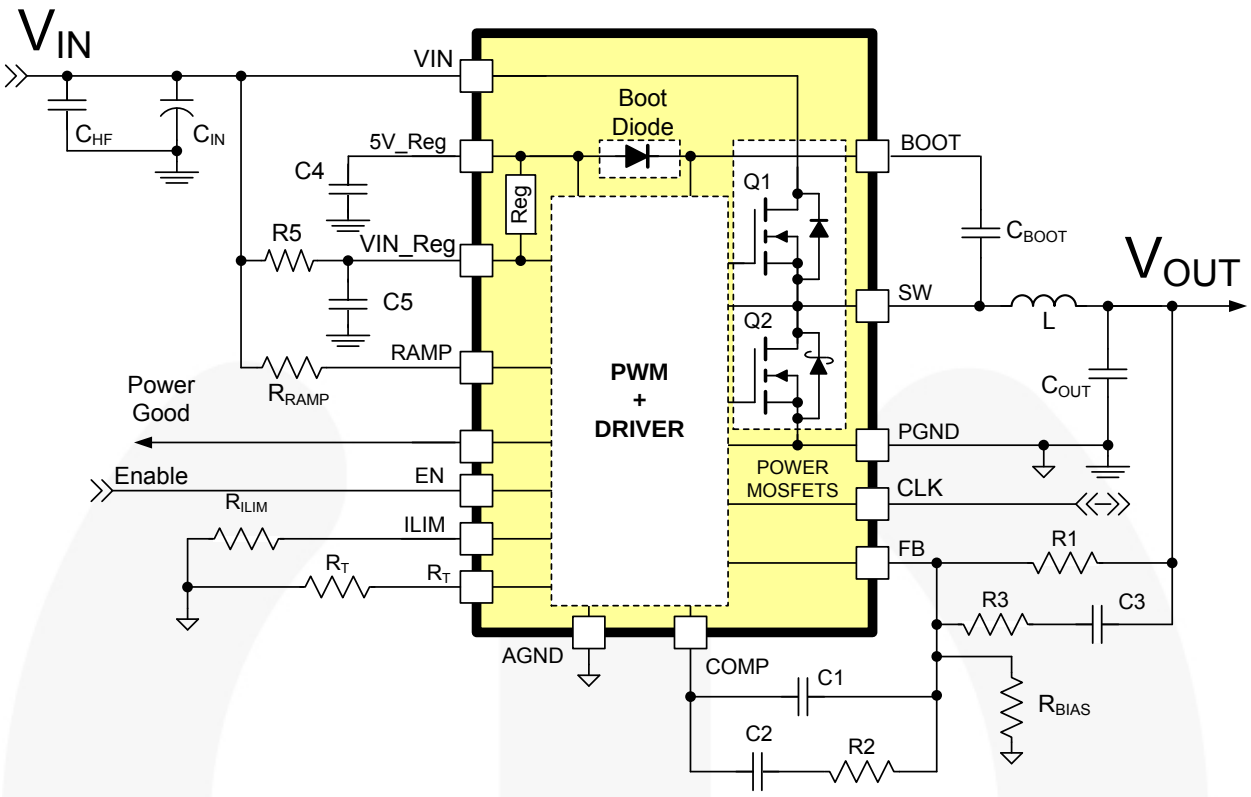

Figure 1. Typical Application, Master, V_{IN}=6.5 V to 24 V

Block Diagram

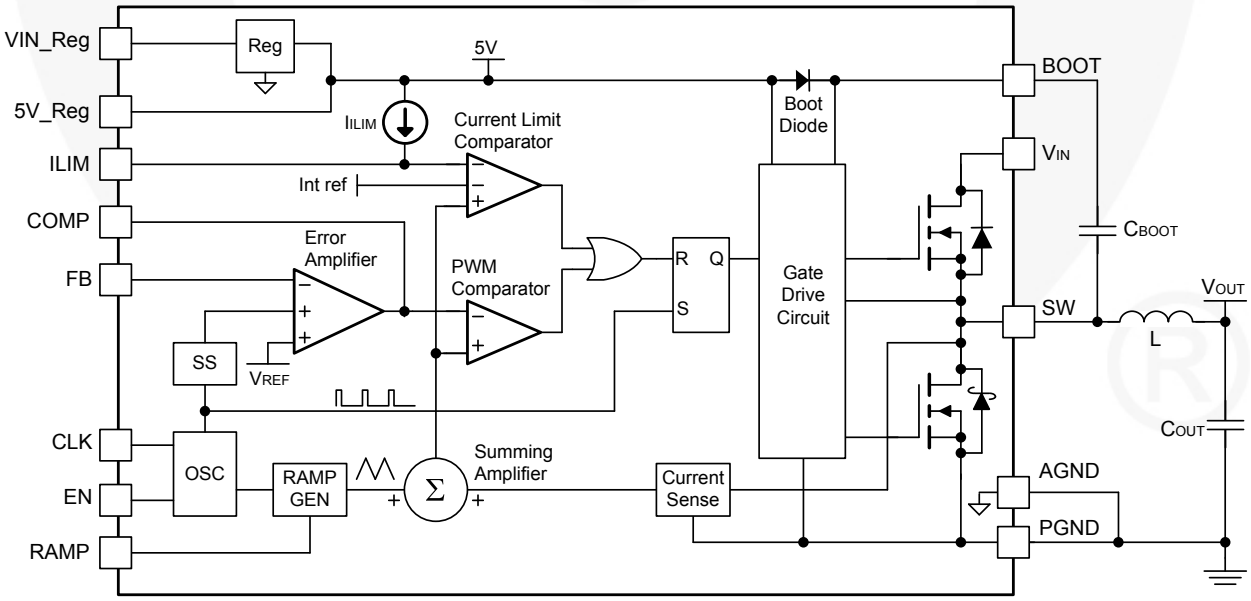

Figure 2. Block Diagram

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Pin Configuration

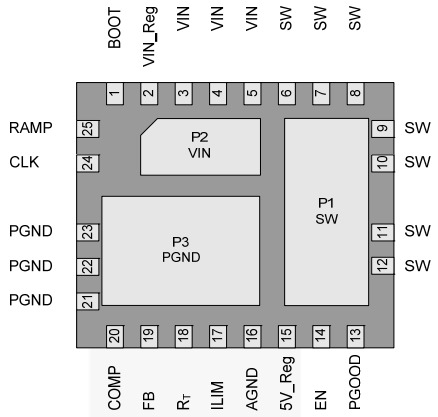

Figure 3. MLP 5 x 6 mm Pin Configuration (Bottom View)

Pad / Pin Definitions

Pad / Pin	Name	Description
P1, 6-12	SW	**Switching Node**. Junction of high-side and low-side MOSFETs.
P2, 3-5	VIN	**Power Input Voltage**. Supply voltage for the converter.
P3, 21-23	PGND	**Power Ground**. Power return and Q2 source.
1	BOOT	**High-Side Drive BOOT Voltage**. Connect through capacitor (C_{BOOT}) to SW. The IC has an internal synchronous bootstrap diode to recharge the capacitor on this pin to 5 V.
2	VIN_Reg	**Regulator Input Voltage.** Input voltage to the internal regulator. Connect to input voltage >6.5 V with 1 µF bypass capacitor at the pin.
13	PGOOD	**Power-Good**. An open-drain output that pulls LOW when the voltage on the FB pin is outside the limits specified in the electrical specs. PGOOD does not assert HIGH until the fault latch is enabled.
14	EN	**ENABLE**. Enables operation when pulled to logic HIGH or left open. Toggling EN resets the regulator after a latched-fault condition. This input has an internal pull-up. When a latched fault occurs, EN is discharged by a current sink.
15	5V_Reg	**5V Regulator Output**. Internal regulator output that provides power for the IC's logic and analog circuitry. This pin should be connected to AGND through a >2.2 µf X5R/X7R capacitor.
16	AGND	**Analog Ground**. The signal ground for the IC. All internal control voltages are referred to this pin. Tie this pin to the ground island/plane through the lowest impedance connection.
17	ILIM	**Current Limit**. A resistor (R_{ILIM}) from this pin to AGND can be used to program the current-limit trip threshold lower than the internal default setting.
18	R_T	**Oscillator Frequency and Master/Slave Set**. Connecting a resistor (R_T) to AGND sets the oscillator frequency and configures the CLK pin as an output (master). Tying this pin to 5 V_Reg through a resistor configures the CLK signal as an input (slave) and establishes the free-running oscillator frequency.
19	FB	**Output Voltage Feedback**. Connect through a resistor divider to the output voltage.
20	COMP	**Compensation**. Error amplifier output. Connect the external compensation network between this pin and FB.
24	CLK	**Clock**. Bi-directional signal pin, depending on master/slave configuration. When configured as a master, this pin represents the clock output that connects directly to the slave(s) for synchronizing with 180° phase shift.
25	RAMP	**Ramp Amplitude**. A resistor (R_{RAMP}) connected from this pin to VIN sets the internal ramp amplitude and also provides voltage feedforward functionality.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Conditions	Min.	Max.	Units
VIN, VIN_Reg to AGND	AGND=PGND		28	V
5V_Reg to AGND	AGND=PGND		6	V
BOOT to PGND			35	V
BOOT to SW		-0.5	6.0	V
SW to PGND	Continuous	-0.5	24.0	V
	Transient (t < 20 ns, f ≤ 600 KHz)	-5	30	V
All other pins		-0.3	6.0	V
ESD	Human Body Model, JESD22-A114	1.5		kV
	Charged Device Model, JESD22-C101	2.5		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
f_{SW}	Switching Frequency		200	500	600	KHz
V_{IN}, VIN_Reg	Supply Voltage for Power and Bias	VIN to PGND	3.0		24.0	V
		VIN_Reg to AGND	6.5		24.0	V
T_A	Ambient Temperature	FAN21SV06MX	-10		+85	°C
		FAN21SV06EMX	-40		+85	°C
T_J	Junction Temperature				+125	°C

Thermal Information

Symbol	Parameter		Min.	Typ.	Max.	Units
T_{STG}	Storage Temperature		-65		+150	°C
T_L	Lead Soldering Temperature, 30sec				+300	°C
θ_{JC}	Thermal Resistance: Junction-to-Case	P1 (Q2)		4		°C/W
		P2 (Q1)		7		°C/W
		P3		4		°C/W
$\theta_{J\text{-}PCB}$	Thermal Resistance: Junction-to-Mounting Surface[1]			35[1]		°C/W
P_D	Total Power Dissipation in the package, T_A=25°C[1]				2.8	W

Note:

1. Typical thermal resistance when mounted on a four-layer, two-ounce PCB, as shown in Figure 37. Actual results are dependent upon mounting method and surface related to the design.

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Electrical Characteristics

Recommended operating conditions, using the circuit in Figure 1, with V_{IN}, V_{IN_Reg}=12 V, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies					
Operating Current (VIN+VIN_Reg)	V_{IN}=12 V, 5 V_Reg open, CLK open, f_{SW}=500 KHz, No Load		22	30	mA
VIN_Reg Operating Current	EN=High, 5 V_Reg open, CLK open, f_{SW}=500 KHz		11		mA
VIN_Reg Quiescent Current	EN=High, FB=0.9 V		4	5	mA
VIN_Reg Standby Current	EN=0, V_{IN}=12 V			1	mA
5V_Reg Output Voltage	Internal V_{CC} Regulator, No Load (6.5 V <VIN_Reg<24 V)	4.7	5.0	5.3	V
5V_Reg Max Current Load	VIN_Reg=12 V)			5	mA
VIN_Reg UVLO Threshold	Rising V_{IN}, V_{IN}=VIN_Reg		5.6	6.3	V
	Falling V_{IN}, V_{IN}=VIN_Reg			5	V
Reference					
Reference Voltage measured at FB *(See Figure 4 for Temperature Coefficient)*	FAN21SV06M, 25°C	794	800	806	mV
	FAN21SV06EM, 25°C	795	800	805	mV
Oscillator					
Frequency	R_T=50 kΩ to GND (Master Mode)	255	300	345	KHz
	R_T=24 kΩ to GND (Master Mode)	540	600	660	KHz
Frequency in Slave Mode compared to Master Mode	R_T=24 kΩ to 50kΩ to 5 V_Reg (Slave Mode)	-15		+15	%
Minimum On-Time [2]			40	65	ns
Duty Cycle	V_{IN}=6.5 V, f_{SW}=600 KHz		80	85	%
Ramp Amplitude, Peak–to-Peak[2]	16 V_{IN}, 1.8 V_{OUT}, R_T=30 kΩ, R_{RAMP}=200 kΩ		0.5		V
Minimum Off-Time [2]			100	150	ns
Synchronization					
CLK Output Pulse Width	Master (R_T to GND)	70	85	100	ns
CLK Output Sink Current	Master, V_{CLK}=0.4 V	0.25		0.35	mA
CLK Output Source Current	Master, V_{CLK}=2 V	-2.5		-2.0	mA
CLK Input Pulse Width	Slave: $V_{CLK} \geq$ 2 V	50			ns
CLK Input Source Current	Slave: V_{CLK}=1 V	-230	-200	-170	µA
CLK Input Threshold, Rising	Slave	1.73	1.83	1.93	V
Soft-Start					
V_{OUT} to Regulation ($T_{0.8}$)	Frequency=500 KHz		2.5		ms
Fault Enable/SSOK ($T_{1.0}$)			3.1		ms
Error Amplifier					
DC Gain [2]	VIN_Reg > 6.5 V	80	85		dB
Gain Bandwidth Product[2]		12	15		MHz
Output Voltage Swing (V_{COMP})		0.4		4.0	V
Output Current, Sourcing	5V_Reg=5 V, V_{COMP}=2.2 V	1.5	2.2	2.5	mA
Output Current, Sinking	5V_Reg=5 V, V_{COMP}=1.2 V	0.8	1.2	1.5	mA
FB Bias Current	V_{FB}=0.8 V, 25°C	-850	-650	-450	nA

Note:

2. Specifications guaranteed by design and characterization; not production tested.

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Electrical Characteristics (Continued)

Recommended operating conditions using the circuit in Figure 1 with V_{IN}, VIN_Reg=12 V, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
Control Functions					
EN Threshold, Rising			1.35	2.00	V
EN Hysteresis			250		mV
EN Pull-Up Current	VIN_Reg >6.5 V	-8	-6	-4	µA
EN Discharge Current	Auto-Restart Mode, VIN_Reg>6.5 V		1		µA
FB OK Drive Resistance			800	1000	KΩ
PGOOD LOW Threshold	FB < V_{REF}, 2 Consecutive Clock Cycles(3)	-14.5	-11.0	-8.0	%V_{REF}
	FB > V_{REF}, 2 Consecutive Clock Cycles(3)	+6.5	+10.0	+13.5	%V_{REF}
PGOOD Low Voltage	I_{OUT} ≤ 2 mA			0.4	V
PGOOD Leakage Current	V_{PGOOD}=5 V		0.2	1.0	µA
Protection and Shutdown					
Current Limit	R_{ILIM} Open, fsw=500 KHz,, V_{OUT}=1.8 V, Rramp=200 kΩ, 16 Consecutive Clock Cycles(3)	7	9	11	A
I_{LIM} Current	VIN_Reg > 6.5 V, 25°C	-11	-10	-9	µA
Over-Temperature Shutdown	Internal Temperature		155		°C
Over-Temperature Hysteresis			30		°C
Over-Voltage Threshold	2 Consecutive Clock Cycles(3)	110	115	120	%V_{OUT}
Under-Voltage Shutdown	16 Consecutive Clock Cycles(3)	68	73	78	%V_{OUT}
Fault-Discharge Threshold	Measured at FB pin		250		mV
Fault-Discharge Hysteresis	Measured at FB pin (V_{FB} ~50 mV)		250		mV

Note:

3. Delay times are not tested in production. Guaranteed by design.

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Typical Characteristics

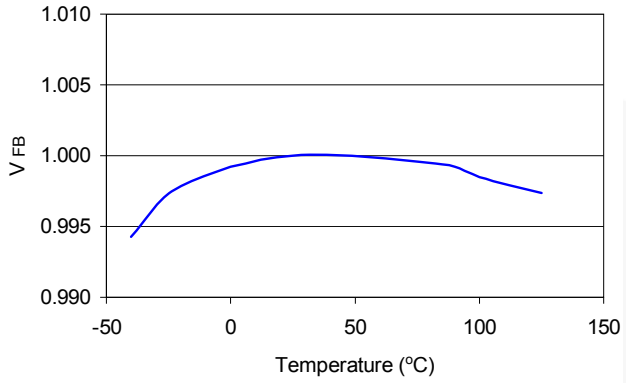

Figure 4. Reference Voltage (V_{FB}) vs. Temperature, Normalized

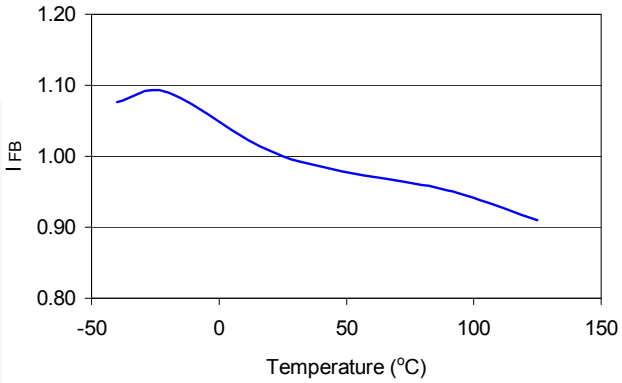

Figure 5. Reference Bias Current (I_{FB}) vs. Temperature, Normalized

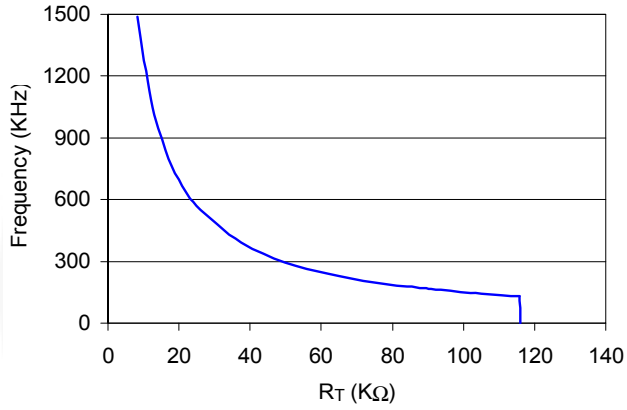

Figure 6. Frequency vs. R_T (Master)

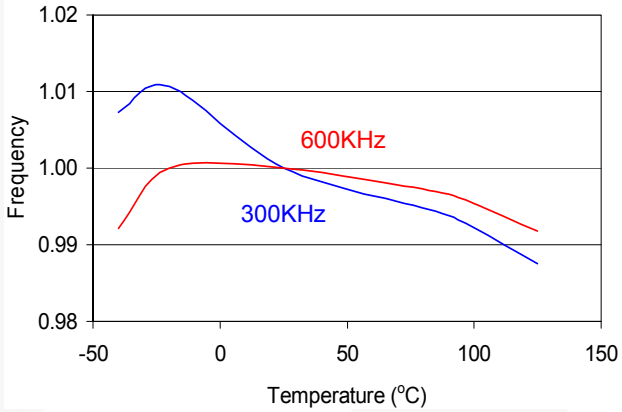

Figure 7. Frequency vs. Temperature, Normalized

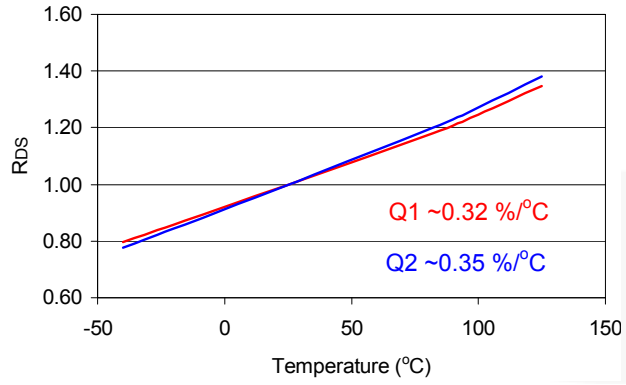

Figure 8. R_{DS} vs. Temperature, Normalized (5 V_Reg=V_{GS}=5 V)

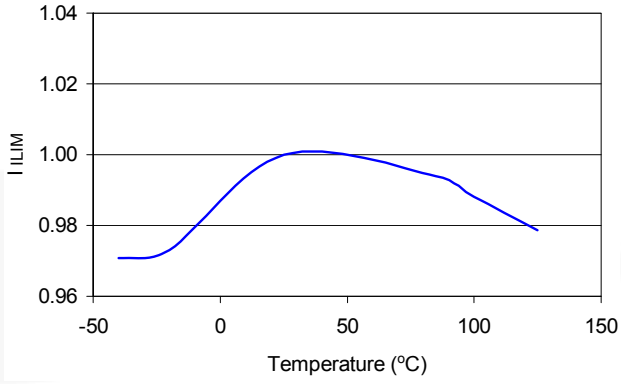

Figure 9. ILIM Current (I_{ILIM}) vs. Temperature, Normalized

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Application Circuit

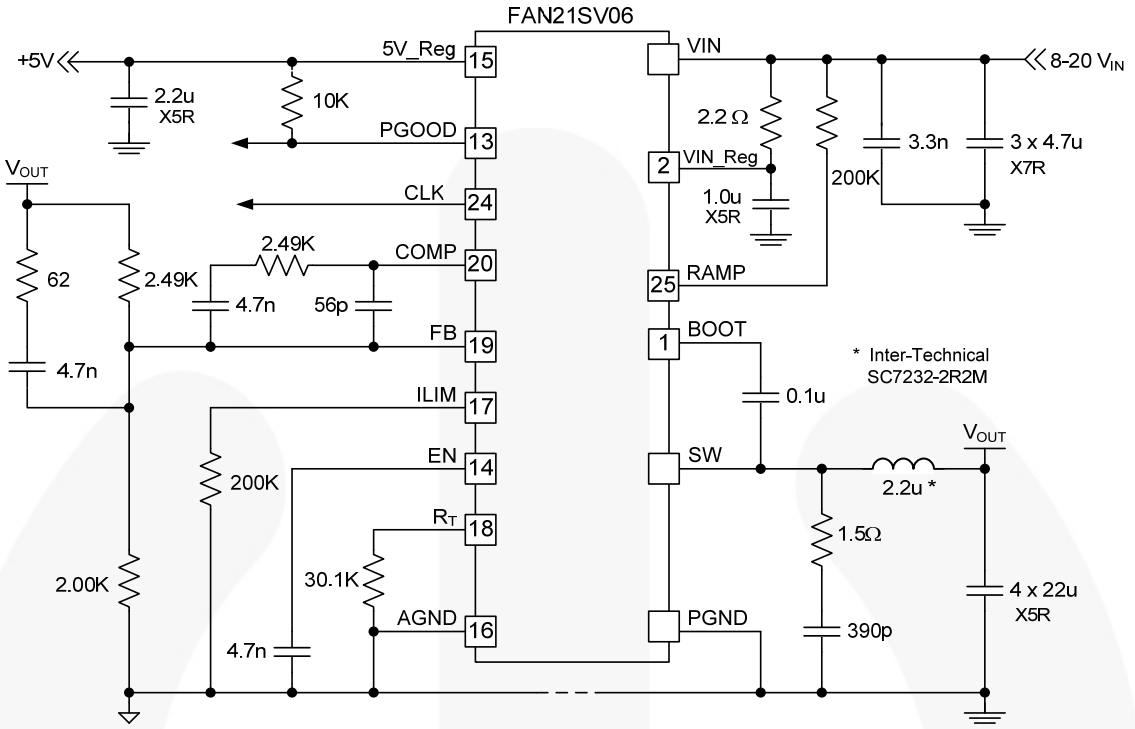

Figure 10. Single-Supply Application Circuit: 1.8 V_{OUT}, 500 KHz, Master

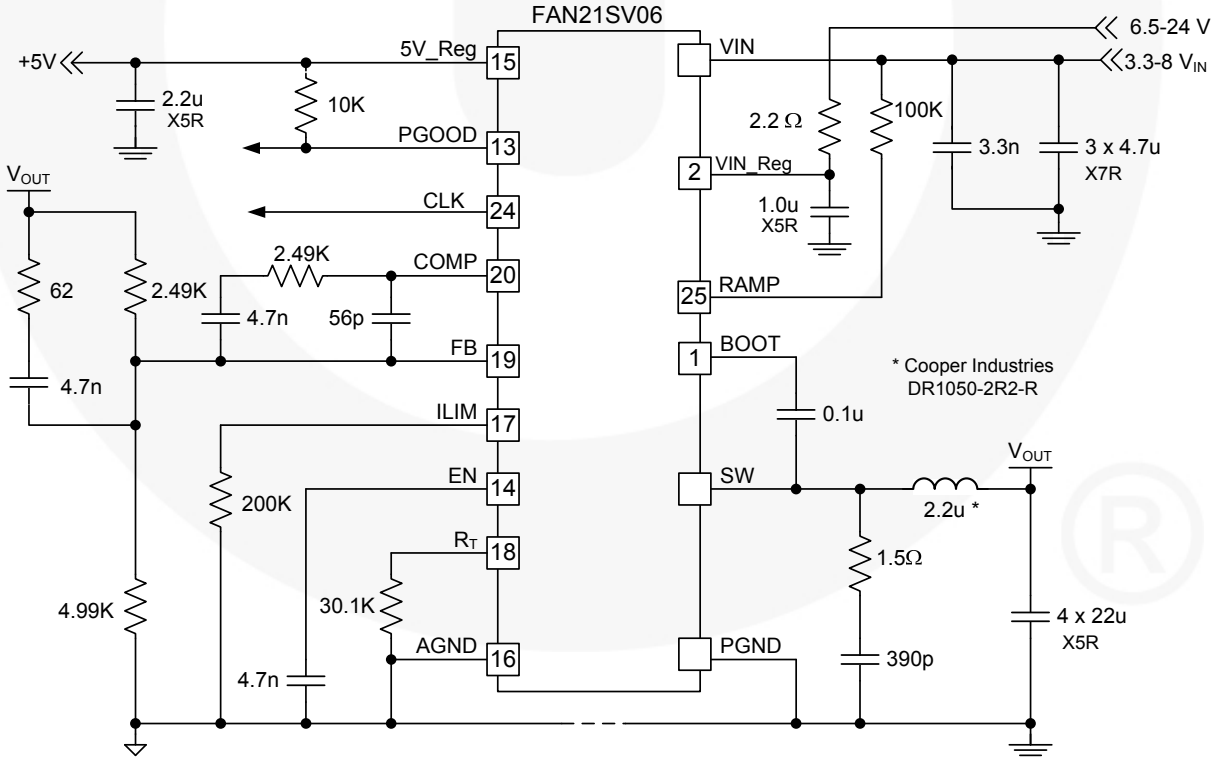

Figure 11. Dual-Supply Application Circuit: 1.2 V_{OUT}, 600 KHz, Master 3.3 V – 8 V Input

Typical Performance Characteristics

Typical operating characteristics using the circuit shown in Figure 10, unless otherwise specified.

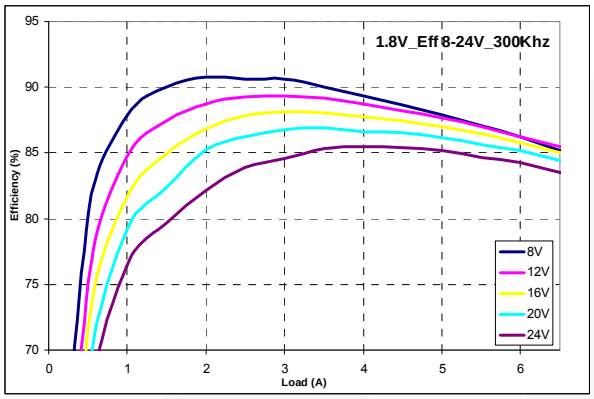

Figure 12. 1.8 V_{OUT} Efficiency Over V_{IN} vs. Load

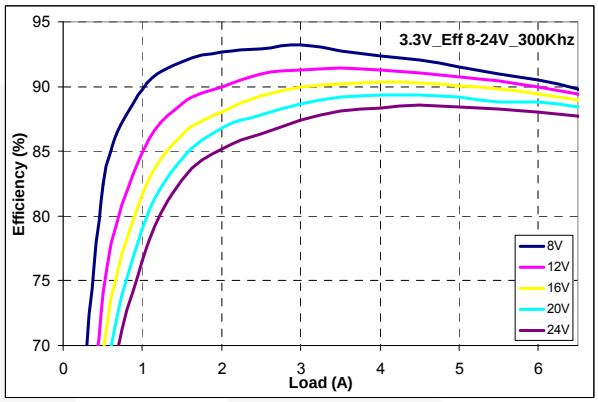

Figure 13. 3.3 V_{OUT} Efficiency vs. Load (Circuit Value Changes)

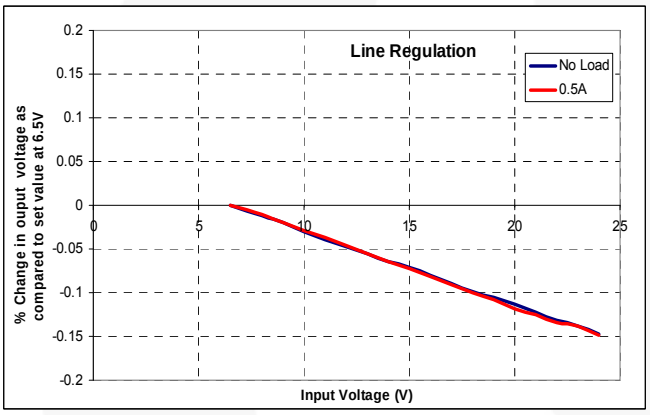

Figure 14. 1.8 V_{OUT} Line Regulation

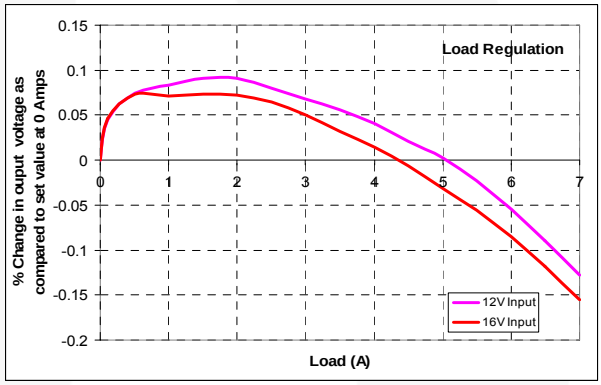

Figure 15. 1.8 V_{OUT} Load Regulation

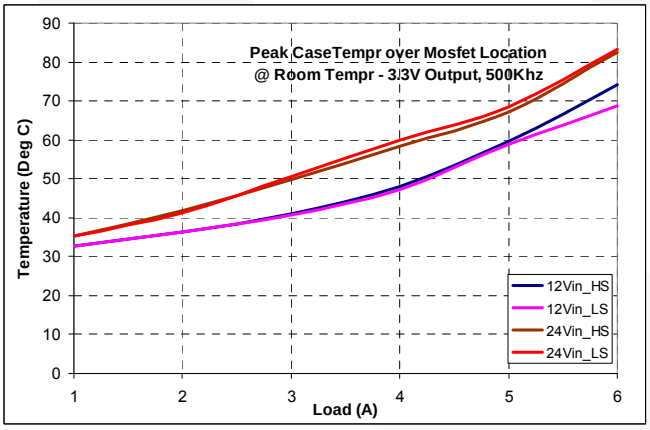

Figure 16. Peak Case Temp over MOSFET Locations 3.3 V Output, 12 V and 24 V Input (500 KHz)

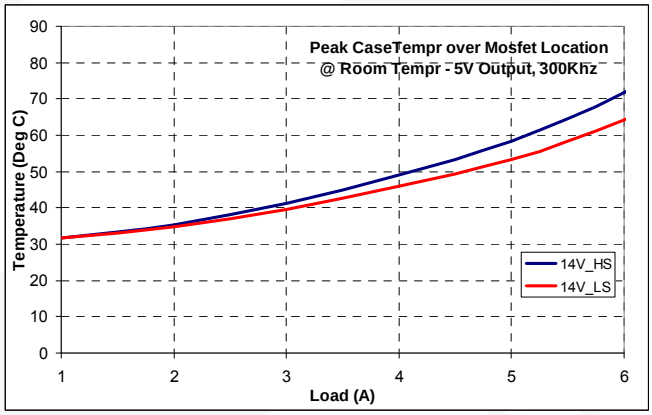

Figure 17. Peak Case Temp. Over MOSFET Locations 5 V Output (300 KHz)

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Typical Performance Characteristics (Continued)

Typical operating characteristics using the circuit shown in Figure 10. V_{IN}=12 V, unless otherwise specified.

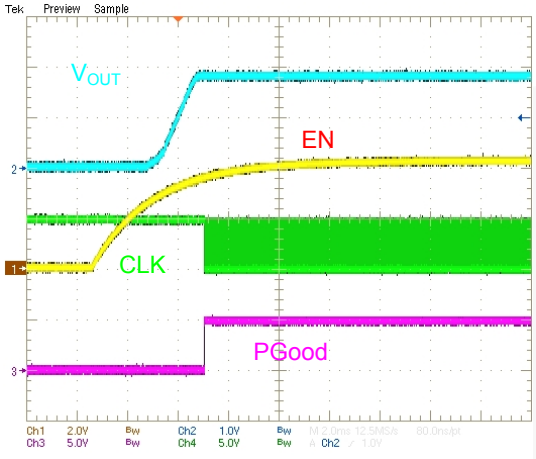

Figure 18. CLK and V_{OUT} at Startup

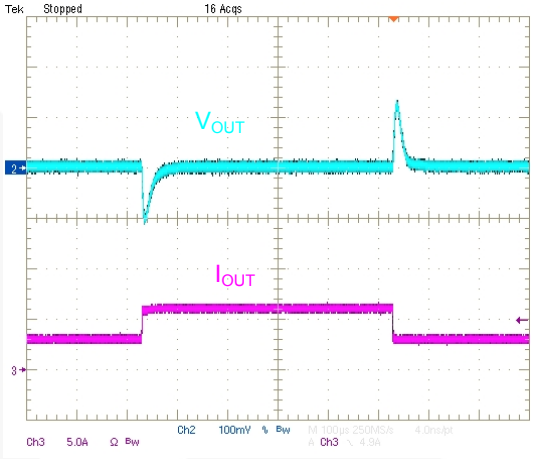

Figure 19. Transient Response, 3-6 A Load

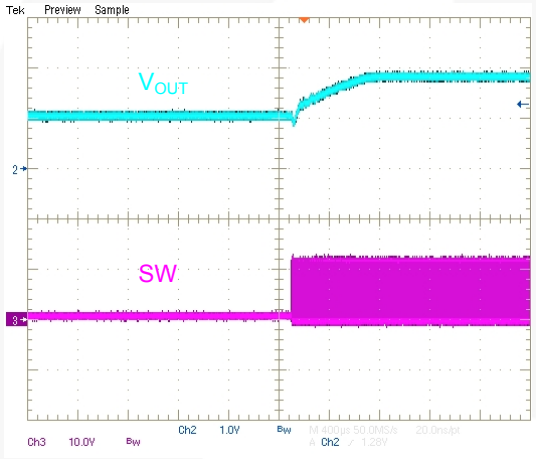

Figure 20. Startup on Pre-Bias

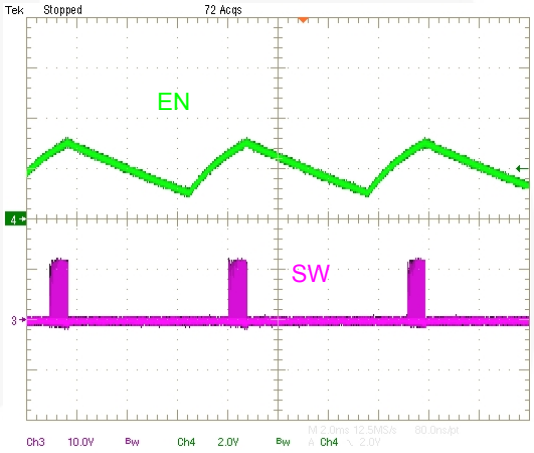

Figure 21. Restart on Fault

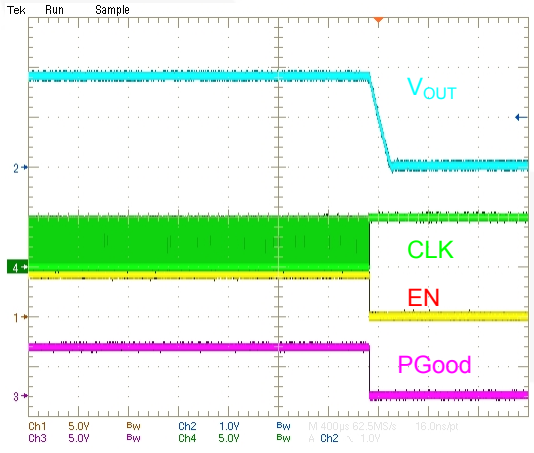

Figure 22. Shutdown, 1 A Load

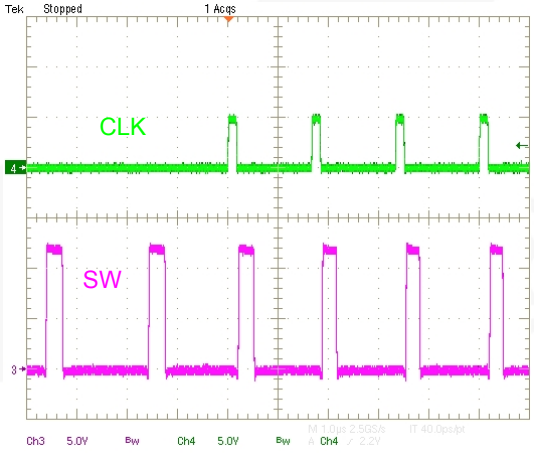

Figure 23. Slave (500 KHz Free-Run to 600 KHz Synchronization)

Typical Performance Characteristics (Continued)

Typical operating characteristics using the circuit shown in Figure 10, unless otherwise specified.

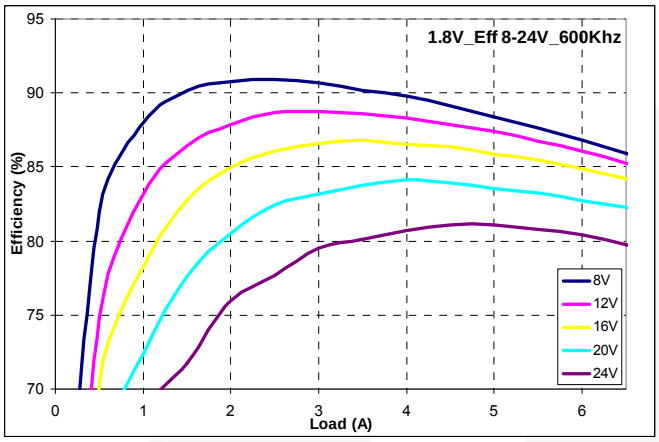

Figure 24. 1.8 V_{OUT} Efficiency 600 KHz

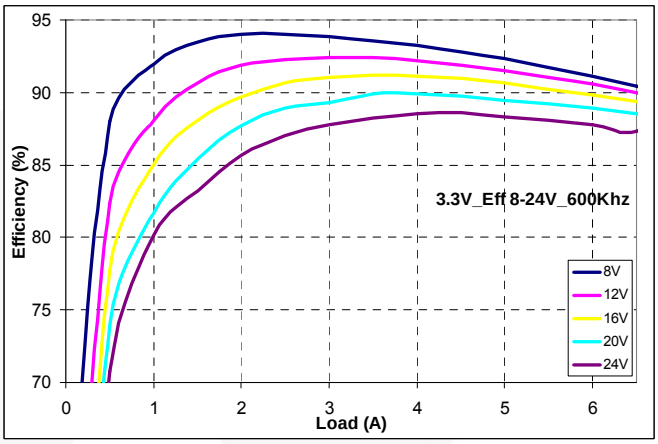

Figure 25. 3.3 V_{OUT} Efficiency 600 KHz

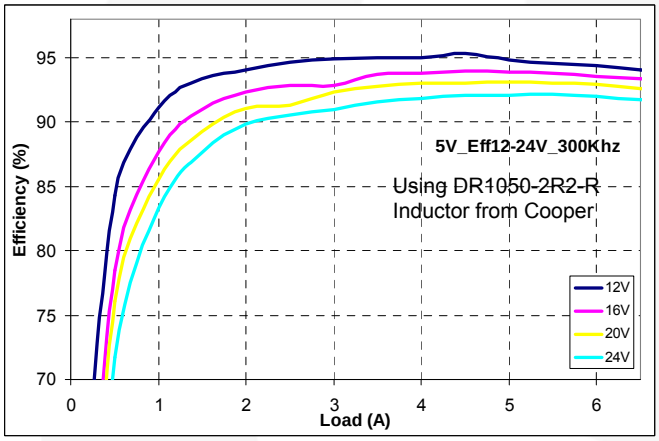

Figure 26. 5 V_{OUT} Efficiency 300 KHz (Circuit Values Change)

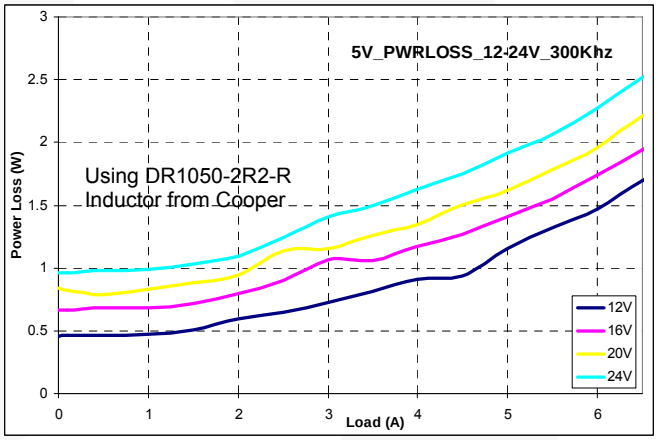

Figure 27. Device Power Loss (5 V_{OUT}, 300 KHz) (Circuit Values Change)

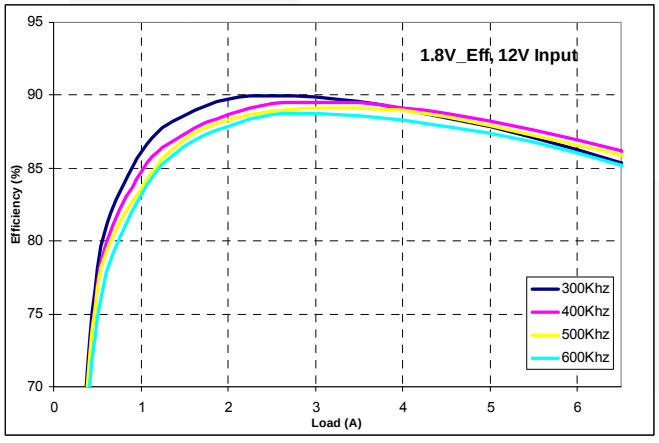

Figure 28. 1.8 V_{OUT} Efficiency Over f_{SW} (Circuit Values Change)

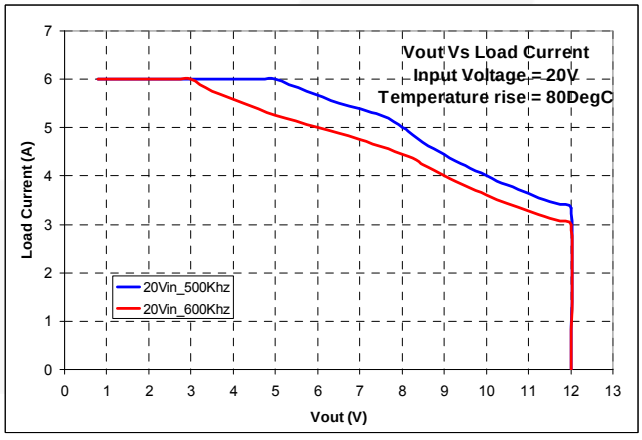

Figure 29. Typical Output Operating Area Based on Thermal Limitations (Circuit Values Change)

Circuit Operation

PWM Generation

Refer to Figure 2 for the PWM control mechanism. FAN21SV06 uses the summing-mode method of control to generate the PWM pulses. An amplified current-sense signal is summed with an internally generated ramp and the combined signal is compared with the output of the error amplifier to generate the pulse width to drive the high-side MOSFET. Sensed current from the previous cycle is used to modulate the output of the summing block. The output of the summing block is also compared against a voltage threshold set by the R_{LIM} resistor to limit the inductor current on a cycle-by-cycle basis. The controller facilitates external compensation for enhanced flexibility.

Initialization

Once VIN_Reg voltage exceeds the UVLO threshold and EN is high, the IC checks for an open or shorted FB pin before releasing the internal soft-start ramp (SS).

If R1 is open (Figure 1), error amplifier output (COMP) is forced LOW and no pulses are generated. After the SS ramp times out (T1.0), an under-voltage fault occurs.

If the parallel combination of R1 and R_{BIAS} is ≤ 1 kΩ, the internal SS ramp is not released and the regulator does not start.

Internal Regulator

FAN21SV06 facilitates single-supply operation for input voltages >6.5 V. At startup, the output of the internal regulator tracks the input voltage and comes into regulation (5 V) when VIN_Reg exceeds the UVLO threshold. The EN pin is released at the same time. The output voltage of the internal regulator (5 V_Reg) is set to 5 V. The internal regulator supplies power to all the control circuits including the drivers.

For applications with V_{IN}<6.5 V, FAN21SV06 can be used if VIN_Reg is provided with a separate low-power source >6.5 V. VIN_Reg supply should come up after VIN during dual-supply operation. The VIN_Reg pin should always be decoupled with at least 1 µF ceramic capacitor (see Figure 11).

Since V_{CC} is used to drive the internal MOSFET gates, high peak currents are present on the 5V_Reg pin. Connect a ≥2.2 µf X5R or X7R decoupling capacitor between the 5 V_Reg pin and PGND.

In addition to supplying power for the control circuits internally, 5 V_Reg output can be used as a reference voltage for other applications requiring low noise reference voltage. 5 V_Reg is capable of sourcing up to 5 mA of output current.

When EN is pulled LOW externally, 5 V_Reg output is still present but the IC is in standby mode with no switching.

Soft-Start

FAN21SV06 uses an internal digital soft-start circuit to slowly ramp up the output voltage and limit inrush current during startup. When 5 V_Reg is in regulation and EN is high, the circuit releases SS and enables the PWM regulator. Soft-start time is a function of switching frequency (number of clock cycles).

Once internal SS ramp has charged to 0.8 V (T0.8), the output voltage is in regulation. Until SS ramp reaches 1.0 V (T1.0), only over-current-protection circuit is active during soft-start and all other output protections are inhibited.

In dual-supply operation mode, it is necessary to apply VIN before VIN_Reg reaches its UVLO threshold to avoid skipping the soft-start cycle.

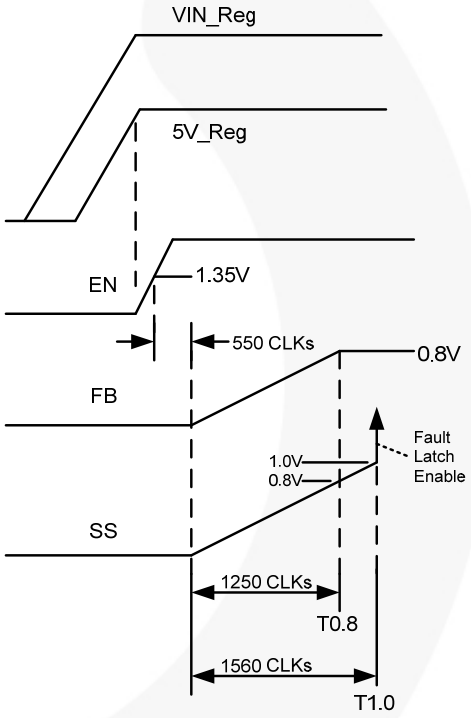

Figure 30. Typical Soft-Start Timing Diagram

VIN_Reg UVLO or toggling the EN pin discharges the SS and resets the IC.

Startup on Pre-Bias

The regulator does not allow the low-side MOSFET to operate in full synchronous mode until SS reaches 95% of V_{REF} (~0.76 V). This enables the regulator to startup on a pre-biased output and ensures that output is not discharged during the soft-start cycle.

Protections

The converter output is monitored and protected against extreme overload, short-circuit, over-voltage, and under-voltage conditions.

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Under-Voltage Protection

If FB remains below the under-voltage threshold for 16 consecutive clock cycles, the fault latch is set and the converter shuts down. This fault is prevented from setting the fault latch during soft-start.

Over-Voltage Protection

If FB exceeds 115% • V_{REF} for two consecutive clock cycles, the fault latch is set and shutdown occurs.

A shorted high-side MOSFET condition is detected when SW voltage exceeds ~0.7 V while the low-side MOSFET is fully enhanced. The fault latch is set immediately upon detection.

These two fault conditions are allowed to set the fault latch at any time, including during soft-start.

Over-Temperature Protection

The chip incorporates an over-temperature-protection circuit that sets the fault latch when a die temperature of about 155°C is reached. The IC is allowed to restart when the die temperature falls below 125°C.

EN / Auto-Restart

After a fault, EN pin is discharged with 1 µA current pull down to a 1.1 V threshold before the internal 800 kΩ pull up is restored. A new soft-start cycle begins when EN charges above 1.35 V.

Depending on the external circuit, the FAN21SV06 can be configured to remain latched off or automatically restart after a fault, as listed in Table 1.

Table 1. Fault / Restart Configurations

EN pin	Controller / Restart State
Pull to GND	Standby
Connected to 5 V_Reg	No restart – latched OFF
Open	Immediate restart after fault
Cap to GND	New soft-start cycle after: EN is HIGH (Auto Restart Mode)

With EN left open, restart is immediate.

If auto-restart is not desired, tie the EN pin high with a logic gate to keep the 1 µA current sink from discharging EN to 1.1 V. Figure 31 shows one method to pull up EN to V_{CC} for a latch configuration.

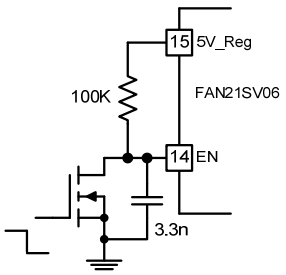

Figure 31. Enable Control with Latch Option

Power Good (PGOOD) Signal

PGOOD is an open-drain output that asserts LOW when V_{OUT} is out of regulation, as measured at the FB pin. The thresholds are specified in the Electrical Specifications section. PGOOD does not assert HIGH until soft start is complete (T1.0).

Application Information

Setting the Output Voltage

The output voltage of the regulator can be set from 0.8 V to ~80% of V_{IN} by an external resistor divider (R1 and R_{BIAS} in Figure 1). For output voltages >3.3 V, output current rating may need to be de-rated depending on the ambient temperature, power dissipated in the package and the PCB layout. (Refer to Thermal Information table and Figure 29.)

The internal reference is set to 0.8 V with 650 nA sourced from the FB pin to ensure that the regulator does not start if the pin is left open.

The external resistor divider is calculated using:

$$\frac{0.8V}{R_{BIAS}} = \frac{V_{OUT} - 0.8V}{R1} + 650nA \quad (1)$$

Connect R_{BIAS} between FB and AGND.

Setting the Clock Frequency

Oscillator frequency is determined by a resistor, R_T, that is connected between the (R_T)pin and AGND (Master Mode) or 5 V_Reg (Slave Mode):

$$f_{(KHz)} = \frac{10^6}{(65 \bullet R_T) + 135} \quad (2)$$

where R_T is expressed in kΩ.

$$R_{T(K\Omega)} = \frac{(10^6 / f) - 135}{65} \quad (3)$$

where frequency (f) is expressed in KHz. In slave mode, the switching frequency is about 10% slower for the same R_T.

The regulator does not start if R_T is open in Master mode.

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Calculating the Inductor Value

Typically the inductor value is chosen based on ripple current (ΔI_L) which is chosen between 10 to 35% of the maximum DC load. Regulator designs that require fast transient response use a higher ripple-current setting while regulator designs that require higher efficiency keep ripple current on the low side and operate at a lower switching frequency.

$$\Delta IL = \frac{V_{OUT} \bullet (1-D)}{L \bullet f} \quad (4)$$

where f is the oscillator frequency, and

$$L = \frac{V_{OUT} \bullet (1-D)}{\Delta IL \bullet f} \quad (5)$$

Setting the Ramp-Resistor Value

As a starting point, set the internal ramp amplitude (ΔV_{RAMP}) to 0.5 V. R_{RAMP} is approximately:

$$R_{RAMP(K\Omega)} = \frac{(V_{IN} - 1.8) \bullet V_{OUT}}{18x10^{-6} \bullet V_{IN} \bullet f} - 2 \quad (6)$$

where frequency (f) is expressed in KHz.

Refer to AN-6033 — FAN21SV06 Design Guide to determine the optimal R_{RAMP} value.

Setting the Current Limit

The current limit system involves two comparators. The MAX I_{LIMIT} comparator is used with a V_{ILIM} fixed-voltage reference and represents the maximum current limit allowable. This reference voltage is temperature compensated to reflect the R_{DSON} variation of the low-side MOSFET. The ADJUST I_{LIMIT} comparator is used where the current limit needs to be set lower than the V_{ILIM} fixed reference. The 10 µA current source does not track the R_{DSON} changes over temperature, so change is added into the equations for calculating the ADJUST I_{LIMIT} comparator reference voltage, as is shown below. Figure 32 shows a simplified schematic of the over-current system.

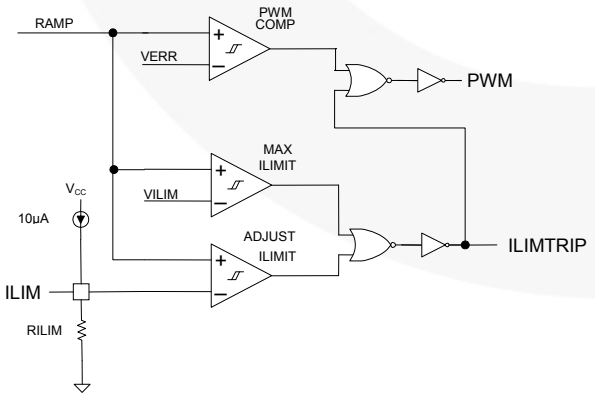

Figure 32. Current-Limit System Schematic

Since the I_{LIM} voltage is set by a 10 µA current source into the R_{ILIM} resistor, the basic equation for setting the reference voltage is:

$$V_{RILIM} = 10\mu A * R_{ILIM} \quad (7)$$

To calculate R_{ILIM}:

$$R_{ILIM} = V_{RILIM} / 10\mu A \quad (8)$$

The voltage V_{RILIM} is made up of two components, V_{BOT} (which relates to the current through the low-side MOSFET) and V_{RMPEAK} (which relates to the peak current through the inductor). Combining those two voltage terms results in:

$$R_{ILIM} = (V_{BOT} + V_{RMPEAK}) / 10\mu A \quad (9)$$

$$R_{ILIM} = \{0.96 + (I_{LOAD} * R_{DSON} * K_T * 8)\} + \{D*(V_{IN} - 1.8)/(f_{SW}*0.03*10\text{^-}3*R_{RAMP})\}/10\mu A \quad (10)$$

where:

$V_{BOT} = 0.96 + (I_{LOAD} * R_{DSON} * K_T * 8)$;

$V_{RMPEAK} = D*(V_{IN} - 1.8)/(f_{SW}*0.03*10\text{^-}3*R_{RAMP})$;

I_{LOAD} = the desired maximum load current;

R_{DSON} = the nominal R_{DSON} of the low-side MOSFET;

K_T = the normalized temperature coefficient for the low-side MOSFET (on datasheet graph);

$D = V_{OUT}/V_{IN}$ duty cycle;

f_{SW} = Clock frequency in kHz; and

R_{RAMP} = chosen ramp resistor value in kΩ.

After 16 consecutive, pulse-by-pulse, current-limit cycles, the fault latch is set and the regulator shuts down. Cycling V_{CC} or EN restores operation after a normal soft-start cycle *(refer to the Auto-Restart section)*.

The over-current protection fault latch is active during the soft-start cycle. Use 1% resistor for R_{ILIM}.

Loop Compensation

The control loop is compensated using a feedback network around the error amplifier. Figure 33 shows a complete Type-3 compensation network. Type-2 compensation eliminates R3 and C3.

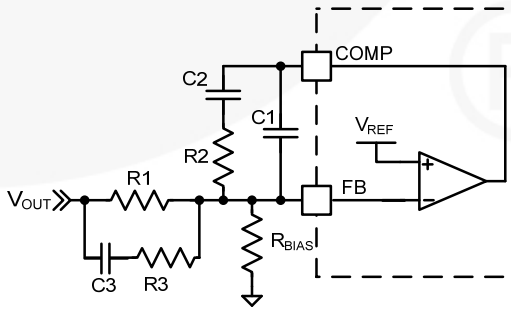

Figure 33. Compensation Network

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Since the FAN21SV06 employs summing current-mode architecture, Type-2 compensation can be used for many applications. For applications that require wide loop bandwidth and/or use very low-ESR output capacitors, Type-3 compensation may be required.

R_{RAMP} provides feedforward compensation for changes in V_{IN}. With a fixed R_{RAMP} value, the modulator gain increases as V_{IN} is reduced, which could make it difficult to compensate the loop. For low-input-voltage-range designs (3 V to 8 V), R_{RAMP} and the compensation component values are going to be different as compared to designs with V_{IN} between 8 V and 24 V.

Master/Slave Configuration

When first enabled, the IC determines if it is configured as a master or slave for synchronization, depending on how R_T is connected.

Table 2. Master / Slave Configuration

R_T to:	Master / Slave	CLK Pin
GND	Master	Output
5V_Reg	Slave, free-running	Input

Slaves free-run in the absence of an external clock signal input when R_T is connected to 5 V_Reg, allowing regulation to be maintained. It is not recommended to leave R_T open when running in slave mode to avoid noise pick up on the clock pin.

Slave free-running frequency should be set at least 25% lower than the incoming synchronizing pulse frequency. Maximum synchronizing clock frequency is recommended to be below 600 KHz.

Synchronization

The synchronization method employed by the FAN21SV06 also provides the following features for maximum flexibility.

- Synchronization to an external system clock
- Multiple FAN21SV06s can be synchronized to a single master or system clock
- Independently programmable phase adjustment for one or multiple slaves
- Free-running capability in the absence of system clock or, if the master is disabled/faulted, the slaves can continue to regulate at a lower frequency

The FAN21SV06 master outputs an 85 ns-wide clock (CLK) signal, delayed 180° from its leading PWM edge. This feature allows out-of-phase operation for the slaves, thereby reducing the input capacitance requirements when more than one converter is operating on the same input supply. The leading SW-node edge is delayed ~40 ns from the rising PWM signal.

On a slave, synchronization is rising-edge triggered. The CLK input pin has a 1.8 V threshold and a 200 µA current source pull-up.

In Master mode, the clock signals go out after power-good signal asserts high. Likewise, in Slave mode synchronization to an external clock signal occurs after the power-good signal goes high. Until then, the converter operates in free-run mode.

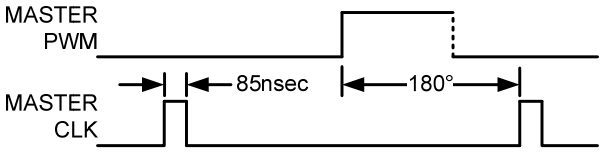


Figure 34. Synchronization Timing Diagram

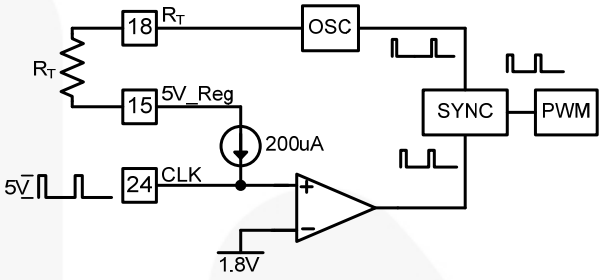


Figure 35. Slave-CLK-Input Block Diagram

One or more slaves can be connected directly to a master or system clock to achieve a 180° phase shift.

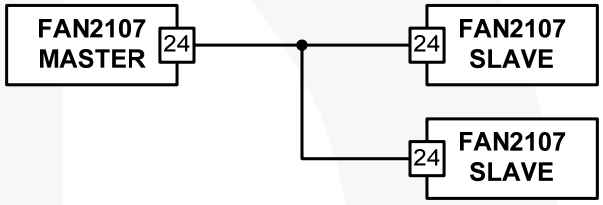


Figure 36. Slaves with 180° Phase Shift

Since the synchronizing circuit utilizes a narrow reset pulse, the actual phase delay is slightly more than 180°.

The FAN21SV06 is not intended for use in single-output, multi-phase regulator applications.

PCB Layout

Good PCB layout and careful attention to temperature rise is essential for reliable operation of the regulator. Four-layer PCB with 2-ounce copper on the top and bottom side and thermal vias connecting the layers is recommended. Keep power traces wide and short to minimize losses and ringing. Do not connect AGND to PGND below the IC. Connect AGND pin to PGND at the output OR to the PGND plane.

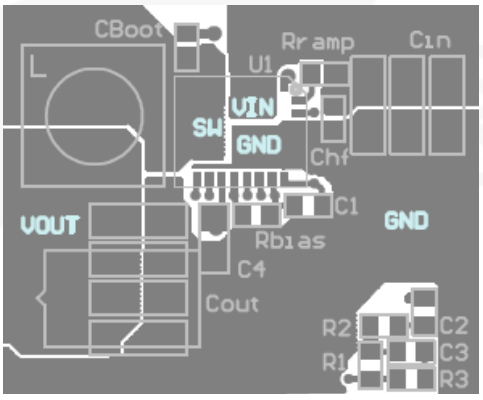
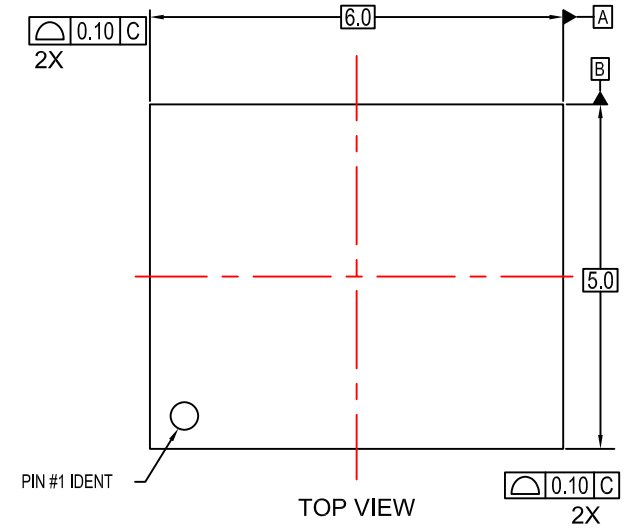
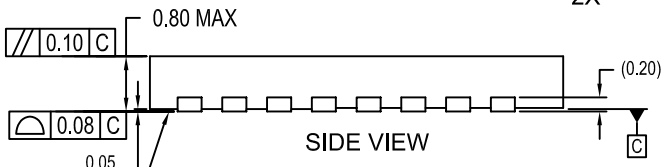


Figure 37. Recommended PCB Layout

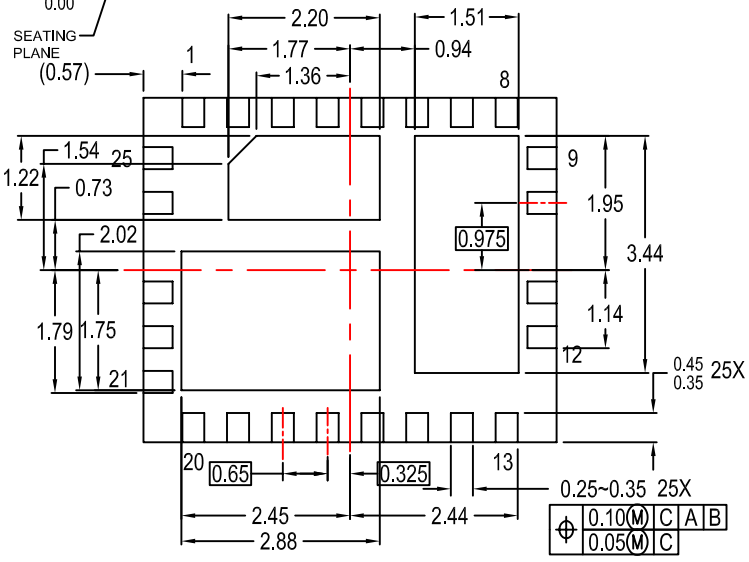
REVISIONS			
LTR	DESCRIPTION	DATE	BY/SITE
1	RELEASE TO DOCUMENT CONTROL	12-Jul-2007	J Chan/FSPM
2	ADDED DIMENSIONS TO BOTTOM VIEW AND LANDPATTERN RECOMMENDATION	7-SEPT-2007	H.ALLEN/FSME
3	CHAMFERED LANDPATTERN PAD 1	17-JUN-2009	H.ALLEN/FSME



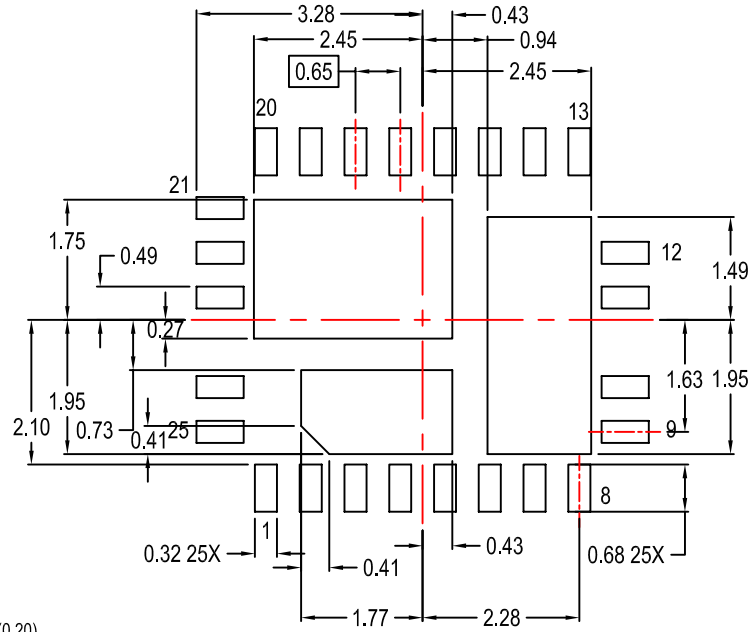
TOP VIEW



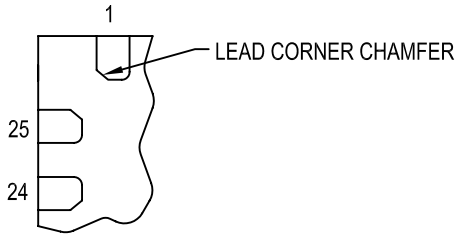
SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN
ALL VALUES TYPICAL EXCEPT WHERE NOTED



OPTIONAL LEAD DESIGN
(LEADS# 1, 24 & 25 ONLY)
SCALE: 1.5X

NOTES: UNLESS OTHERWISE SPECIFIED

A) DIMENSIONS ARE IN MILLIMETERS.

B) DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.

D) DESIGN BASED ON JEDEC MO-220 VARIATION WJHC

E) TERMINALS ARE SYMMETRICAL AROUND THE X & Y AXIS EXCEPT WHERE DEPOPULATED.

F) DRAWING FILENAME: MKT-MLP25AREV3

APPROVALS	DATE
DRAWN H.ALLEN	7-SEPT-07
DFTG. CHK. S.MARTIN	7-SEPT-07
ENGR. CHK.	

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