



3.3 Volt CMOS Bus Interface 8-Bit Latches

QS74FCT3373
QS74FCT32373

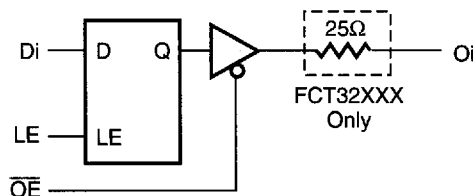
FEATURES/BENEFITS

- Pin and function compatible to the 74F373 74LVT373 and 74FCT373T
- Available in SOIC and QSOP
- Undershoot clamp diodes on all inputs
- Ground bounce controlled outputs
- Low power QCMOS: 0.03 μ W typ static
- JEDEC spec compatible
- $I_{OL} = 24$ mA Com.
- TTL-compatible input and output levels
- Extended temperature -40°C to $+85^{\circ}\text{C}$
- 2.7V to 3.6V Supply Voltage
- 5V compatible input pins

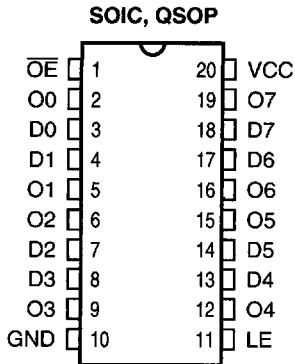
DESCRIPTION

The QSFCT3373 is an 8-bit high-speed CMOS TTL-compatible buffered latch with three-state outputs that are ideal for driving high-capacitance loads such as memory and address buses. All inputs have clamp diodes for undershoot noise suppression and all outputs have ground bounce suppression (see QSI Application Note AN-001). Input pins can be driven by 3.3V or 5V components allowing voltage transition in mixed supply systems. Ultra-low power QCMOS technology makes this product ideal for portable computing systems or communications devices.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (All Pins Top View)



PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
O _i	O	Data Outputs
LE	I	Latch Enable
\overline{OE}	I	Output Enable

FUNCTION TABLE

\overline{OE}	Inputs LE	Di	Internal Q Value	Outputs O _i	Function
H	X	X	X	Hi-Z	Disable Outputs
L	X	X	H	H	Enable Outputs
L	X	X	L	L	
X	H	L	L	X	Pass Input Data
X	H	H	H	X	
X	L	X	Q	X	Hold Prior Data

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage to Ground	-0.5V to +4.6V
DC Output Voltage V_{OUT}	-0.5V to $V_{CC} + 0.5V^{(2)}$
DC Input Voltage V_{IN}	-0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Input Diode Current with $V_{IN} < 0$	± 20 mA
DC Output Diode Current with $V_{OUT} < 0$	± 50 mA
DC Output Current Max. Sink Current/Pin	± 60 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	-65° to +150°C

Note:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.
2. Not to exceed 4.6V

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1$ MHz, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	Unit
1,3,4,7,8,11,13,14,17,18	4	4	pF
2,5,6,9,12,15,16,19	6	6	pF

Note: Capacitance is characterized but not tested.

RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Min	Max	Unit
V_{CC}	Supply Voltage	2.7	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_{OUT}	Output Voltage	0	V_{CC}	V
T_A	Ambient Operating Temperature	-40	+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate ⁽¹⁾	0	8	ns/V

Notes:

1. As measured between 0.8V and 2V.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Recommended operating conditions apply unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V _{IH}	Input HIGH Voltage	Input Pins	2.0	—	5.5	V
		I/O Pins	2.0	—	V _{CC} +0.5	V
V _{IL}	Input LOW Voltage	Input Pins	-0.5	—	0.8	V
ΔV _T	Input Hysteresis	V _{TLH} - V _{THL} for All Inputs	—	0.2	—	V
I _{IH} I _{IL}	Input Current Input HIGH or LOW	V _{CC} = Max., 0 ≤ V _{IN} < V _{CC}	—	—	1	μA
I _{oz}	Off-State Output Current (Hi-Z)	V _{CC} = Max., 0 ≤ V _{IN} ≤ V _{CC}	—	—	5	μA
I _{os}	Short Circuit Current	V _{CC} = Max., V _{OUT} = GND ^(2,3)	-60	—	-225	mA
V _{IC}	Input Clamp Voltage	V _{CC} = Min., I _{IN} = -18 mA ⁽³⁾	—	-0.7	—	V
V _{OH}	Output HIGH Voltage	V _I = V _{IH} or V _{IL} , V _{CC} = Min, I _{OH} = -100 μA	V _{CC} -0.2	—	—	V
		V _I = V _{IH} or V _{IL} , V _{CC} = 3V, I _{OH} = -8 mA	2.4	—	—	V
V _{OL}	Output LOW Voltage (FCT3XXX)	V _I = V _{IH} or V _{IL} , V _{CC} = Min, I _{OL} = 100 μA	—	—	0.2	V
		V _I = V _{IH} or V _{IL} , V _{CC} = 3V, I _{OL} = 16 mA	—	—	0.4	V
		V _I = V _{IH} or V _{IL} , V _{CC} = 3V, I _{OL} = 24 mA	—	—	0.5	V
V _{OL}	Output LOW Voltage (FCT32XXX-25Ω)	V _I = V _{IH} or V _{IL} , V _{CC} = 3V, I _{OL} = 8 mA	—	—	0.5	V
R _{OUT}	Output Resistance ⁽⁴⁾ (FCT32XXX-25Ω)	V _{CC} = 3V, I _{OL} = 8 mA	—	40	—	Ω

Notes:

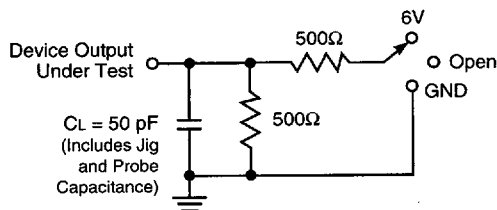
1. Typical values indicate V_{CC} = 3.3V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.
4. R_{OUT} represents total output impedance and includes added series termination resistance.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Typ	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max., freq = 0 0V ≤ V _{IN} ≤ 0.2V or V _{cc} -0.2V ≤ V _{IN} ≤ V _{cc}	—	0.01	20	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max., freq = 0, V _{IN} = V _{cc} - 0.6V	—	1.0	20	μA
Q _{CCD}	Supply Current per Input per MHz	V _{cc} = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V _{cc} ^(2,3)	—	40	85	μA/ MHz

Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
- For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
- I_c can be computed using the above parameters as explained in the Technical Overview section.



Test	Switch
t _{PHL} /t _{PLH}	Open
t _{PZL} /t _{PLZ}	6V
t _{PZH} /t _{PHZ}	GND

Load Circuit for Outputs

Notes

- Input pulse characteristics: 0V to 2.7V, t_r = t_f = 2.5 ns (10% to 90%), transition measured at 1.5V, pulse generator Z_{OUT} = 50Ω.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Recommended operating conditions apply unless otherwise specified.

Symbol	Description ⁽¹⁾	3373, 32373 (V _{CC} = 3.3V ± 0.3V)		3373A, 32373A (V _{CC} = 3.3V ± 0.3V)		Unit
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay Data to O _i , FCT3373	1.5	8	1.5	5.2	ns
t _{PLH} t _{PHL}	Propagation Delay Data to O _i , FCT32373	1.5	8	1.5	5.2	ns
t _{PLH} t _{PHL}	Propagation Delay Data LE to O _i , FCT3373	2	13	2	8.5	ns
t _{PLH} t _{PHL}	Propagation Delay Data LE to O _i , FCT32373	2	13	2	8.5	ns
t _{PZH} t _{PZL}	Output Enable \overline{OE} , to Y _i , FCT3373	1.5	11	1.5	6.5	ns
t _{PZH} t _{PZL}	Output Enable \overline{OE} , to Y _i , FCT32373	1.5	11	1.5	6.5	ns
t _{PLZ} t _{PHZ}	Disable Time ⁽²⁾	1.5	7	1.5	5.5	ns
t _s	Data Setup Time	2	—	2	—	ns
t _h	Data Hold Time D _i to LE HIGH-to-LOW	1.5	—	1.5	—	ns
t _w	LE Pulse Width ⁽²⁾ HIGH or LOW	6	—	5	—	ns

Notes:

1. Minimums guaranteed but not tested for all parameters except t_s and t_h.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.