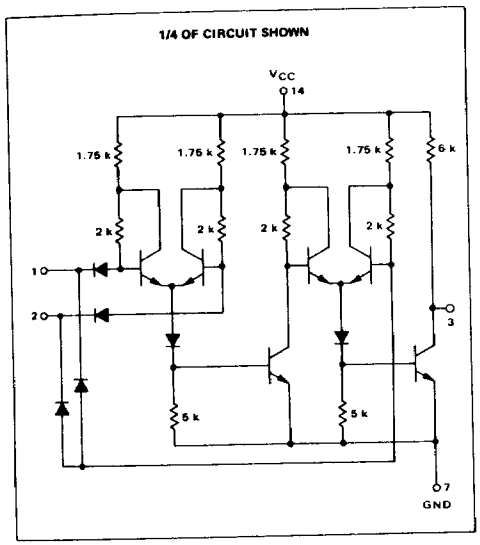
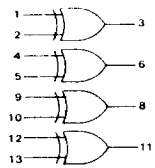
QUAD 2-INPUT
EXCLUSIVE "OR" GATE

MC1912F • MC1812F,P

This device consists of four 2-input gates, each performing the logical EXCLUSIVE OR function. Added logic flexibility provided by this device helps to optimize system designs.





Positive Logic: $3 = 1 \bullet \overline{2} + \overline{1} \bullet 2$

Input Loading Factor = 2

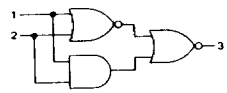
Output Loading Factor = 8

Total Power Dissipation:

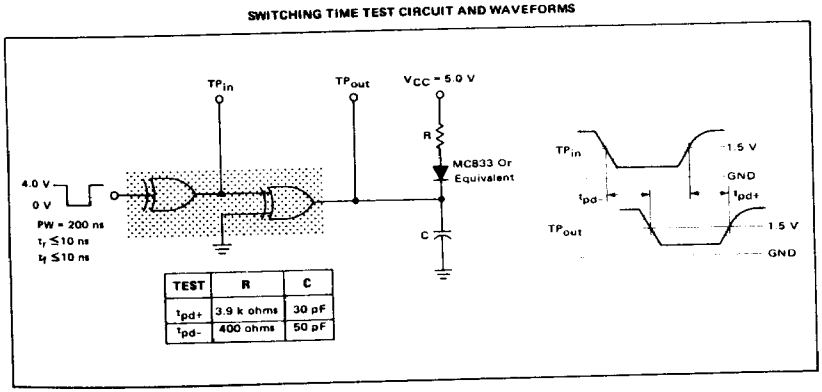
	MC1912/MC1812
Both Inputs High	115 mW
Both Inputs Low	130 mW
One Low One High	95 mW

Propagation Delay Time = 40 ns typ

LOGIC DIAGRAM
1/4 OF DEVICE SHOWN

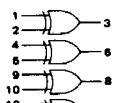


SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner.



@ Test Temperature		I_{OL} (mA)	I_{OH} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_{PD} (Volts)	V_F (Volts)	V_R (Volts)	V_{CEX} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	V_{max} (Volts)
MC1912	−55°C	11.4	-0.12	1.40	2.10	-	0	4.00	-	-	4.50	5.50	-
	+25°C	12.0	-0.12	1.10	2.00	5.00	0	4.00	4.50	5.00	4.50	5.50	8.00
	+125°C	10.8	-0.12	0.80	2.00	-	0	4.00	-	-	4.50	5.50	-
MC1812	0°C	12.0	-0.12	1.20	2.00	-	0.45	4.00	-	-	5.00	5.00	-
	+25°C	12.0	-0.12	1.10	1.90	5.00	0.45	4.00	5.00	5.00	5.00	5.00	8.00
	+75°C	11.4	-0.12	0.95	1.80	-	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC1912 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1812 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{PD}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	3	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	3	-	1,2	-	-	-	-	-	-	14	-	-	7
		3	-	0.40	-	0.40	-	0.45		-	0.45	-	0.45	-	0.50		3	-	-	1,2	-	-	-	-	-		-	-	
	V_{OH}	3	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	3	1	2	-	-	-	-	-		-	-	
		3	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	3	2	1	-	-	-	-	-		-	-	
Short-Circuit Current	I_{SC}	3	-	-1.34	-	-1.34	-	-1.30	mAdc	-	-1.30	-	-1.30	-	-1.25	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	1,3,7
Reverse Current	$2\,I_R$	1	-	4.0	-	4.0	-	10.0	µAdc	-	10	-	10	-	20	µAdc	-	-	-	-	-	-	1	-	-	-	14	-	2,7
		2	-	4.0	-	4.0	-	10.0	µAdc	-	10	-	10	-	20	µAdc	-	-	-	-	-	-	2	-	-	-	14	-	1,7
Output Leakage Current	I_{CEX}	3	-	-	-	50	-	-	µAdc	-	-	-	100	-	-	µAdc	-	-	-	-	-	-	-	3,14	-	-	-	-	1,7
Forward Current	$2\,I_F$	1	-	-3.20	-	-3.20	-	-3.00	mAdc	-	-2.80	-	-2.80	-	-2.67	mAdc	-	-	-	-	-	1	-	-	-	-	14	-	7
		2	-	-3.20	-	-3.20	-	-3.00	mAdc	-	-2.80	-	-2.80	-	-2.67	mAdc	-	-	-	-	-	2	-	-	-	-	14	-	7
Power Drain Current (Total Device)	I_{PDH}	14	-	-	-	34	-	-	mAdc	-	-	-	39	-	-	mAdc	-	-	-	-	-	14	-	-	-	-	-	-	7
	I_{max}	14	-	-	-	47	-	-	mAdc	-	-	-	53	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	1,4,7,9,12
Switching Times																	Pulse In	Pulse Out											
	t_{pd+}	1,3	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	3	-	-	-	-	-	-	14	-	-	-	2,7
	t_{pd-}	1,3	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	3	-	-	-	-	-				-	-	2,7

PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

See the **Additional Support** section of the *DSP56300 Family Manual* for detailed information on the multiple support options available to you.

Table 1 DSP56301 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM/AD
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301/D