FEATURES

- **Pin Compatible with AD7510 DI, AD7511 DI**
- **JFET Switches Rather than CMOS**
- **Highly Resistant to Static Discharge Damage**
- **Radiation Resistant**
- **No SCR Latch-up Problems**
- **Low "ON" Resistance — 75Ω Max**
- **Superior "OFF" Isolation and Crosstalk**
- **Digital Inputs Compatible with TTL and CMOS**
- **No Pull-Up Resistors Required to Insure Break-Before-Make Action with TTL Inputs**
- **Available in Die Form**

ORDERING INFORMATION †

TYPICAL 25°C RESISTANCE	CERDIP 16-PIN	OPERATING TEMPERATURE RANGE
60Ω	SW7510EQ	IND
80Ω	SW7510FQ	IND
60Ω	SW7511AQ* SW7511EQ	MIL IND
80Ω	SW7511BQ* SW7511FQ	MIL IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

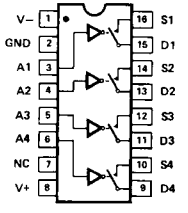
GENERAL DESCRIPTION

The SW-7510/7511 are monolithic linear devices, each containing four independently selectable SPST analog switches. The SW-7510 operates normally-open with logic-low inputs. The SW-7511 operates normally-closed with logic-low inputs. All logic inputs are fully TTL input compatible.

Performance advantages include exceptionally high "OFF" isolation, low leakage current and low crosstalk. Data conversion, position controllers, choppers, demodulators and programmable-gain amplifiers are popular SW-7510/7511 circuit applications.

The PMI Bipolar-JFET process reduces susceptibility to electrostatic destruction and offers a high resistance to radiation exposure. Plus, total freedom from the intrinsic SCR latch-up problems encountered in equivalently manufactured CMOS products.

PIN CONNECTIONS

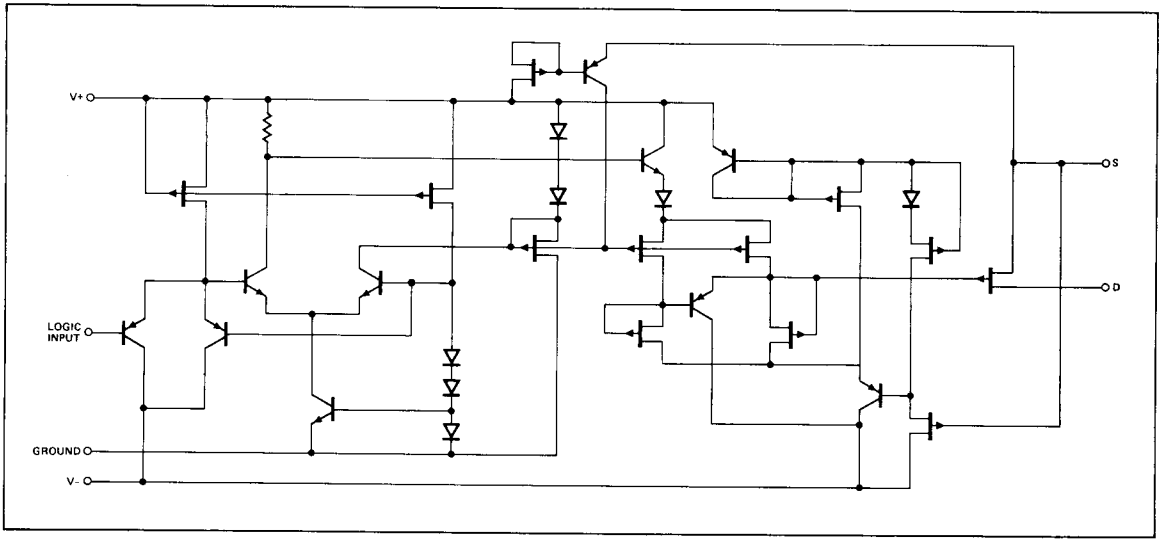


16-PIN HERMETIC DUAL-IN-LINE (Q-Suffix)

CONTROL LOGIC:

SW-7510: Switch "ON" for Address "HIGH"
SW-7511: Switch "ON" for Address "LOW"

SCHEMATIC DIAGRAM (Typical SW-7510 Switch)



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

Operating Temperature Range,
SW-7511AQ, BQ ..... –55°C to +125°C
SW-7510/7511EQ, FQ ..... –25°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply To V– Supply 36V
V+ Supply to Ground 36V
Logic Input Voltage ..... (–2V or V–) to V+ Supply
Analog Input Voltage
Continuous ..... V– Supply to V+ Supply +20V
1% Duty Cycle and Driving All 4 Inputs with
500µs Pulse ..... V– Supply –15V to V+ Supply +20V
Maximum Current Through Any Pin 25mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V and T_A = +25°C, unless otherwise noted.

			SW-7510E SW-7511A/E			SW-7510F SW-7511B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	V_D = 0V, I_{DS} = 1mA	—	60	75	—	80	100	Ω
ΔR_{ON} vs. V_D (V_S)	ΔR_{ON}	$V_D \leq$ 10V, I_D = 1mA	—	15	—	—	15	—	%
R_{ON} Match of Switches	R_{ON} Match	V_D = 0V, I_{DS} = 1mA	—	1.5	10	—	1.5	10	%
Analog Voltage Range	V_A	I_S = 1mA (Note 5)	+10 –10	+11 –15	— —	+10 –10	+11 –15	— —	V
"OFF" Leakage Current	$I_{S(OFF)}$, $I_{D(OFF)}$	V_S = +10V, V_D = –10V, (Note 1)	—	—	1.0	—	—	3.0	nA
"ON" Leakage Current	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D$ = +10V, (Note 1)	—	—	1.0	—	—	3.0	nA
Logic "1" Voltage	V_{INH}	(Note 5)	2.0	—	—	2.0	—	—	V
Logic "0" Voltage	V_{INL}	(Note 5)	—	—	0.8	—	—	0.8	V
Logic "0" Current	I_{INL}	V_{IN} = +0.4V	—	1.5	3.5	—	1.5	3.5	µA
Logic Input Capacitance	C_{DIG}	V_{IN} = +0.4V	—	1.5	—	—	1.5	—	pF
"ON" Switching Time	t_{ON}	V_S = –5V, R_L = 1kΩ, C_L = 7pF, (Note 4)	—	350	450	—	450	550	ns
"OFF" Switching Time	t_{OFF}	V_S = –5V, R_L = 1kΩ, C_L = 7pF, (Note 4)	—	260	300	—	350	450	ns
"OFF" Isolation	ISO_{OFF}	(Note 2)	—	66	—	—	66	—	dB
Crosstalk	C_T	(Note 3)	—	70	—	—	70	—	dB
Analog "OFF" Capacitance	$C_{S(OFF)}$, $C_{D(OFF)}$	V_S =)V, V_D = 0	—	6.5	—	—	6.5	—	pF
Analog "ON" Capacitance	$C_{S(ON)}$, $C_{D(ON)}$	V_S = 0V, V_D = 0	—	14	—	—	14	—	pF
Feedthrough Capacitance	$C_{DS(OFF)}$	V_S = 0V	—	0.8	—	—	0.8	—	pF
Channel Capacitance	$C_{SS(OFF)}$, $C_{DD(OFF)}$	V_S = 0V V_S = 0V	— —	0.4 0.4	— —	— —	0.4 0.4	— —	pF
Positive Supply Current	I+	Logic Inputs at "0" or "1"	—	5.0	9.0	—	3.0	9.0	mA
Negative Supply Current	I–	Logic Inputs at "0" or "1"	—	2.8	5.0	—	1.7	5.0	mA

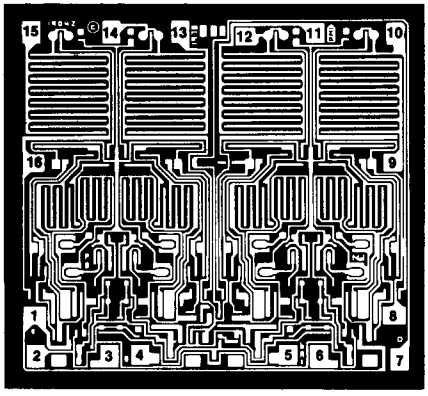
NOTES:
1. The conditions listed specify the worst case leakage currents. The leakage currents apply equally to source (S) or drain(D).
2. OFF isolation is measured by driving the source of any OFF switch and observing the voltage which appears on the drain. The conditions are: R_L = 680Ω, C_L = 7pF, V_S = $5V_{RMS}$, f = 100kHz.
3. Crosstalk is measured by driving source of any OFF switch and observing voltage which appears on any other "ON" output drain. The conditions are: R_L = 680Ω, C_L = 7pF, V_S = $5V_{RMS}$, f = 100kHz.
4. Sample tested.
5. Guaranteed by R_{ON} and leakage tests. For normal operation maximum analog signal voltages should be restricted to less than (V+) –4V.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ for SW-7511AQ, BQ; $-25°C \le T_A \le +85°C$ for SW-7510EQ, FQ and SW-7511EQ, FQ, unless otherwise noted.

			SW-7510E SW-7511A/E			SW-7510F SW-7511B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_{DS} = 1mA$	—	—	100	—	—	150	Ω
ΔR_{ON} vs. Temperature	ΔR_{ON} Drift	$V_D = 0V$, $I_{DS} = 1mA$	—	0.4	—	—	0.5	—	%/°C
Analog Voltage Range	V_A	$I_S = 1mA$ (Note 4)	+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	V
"OFF" Leakage Current	$I_{S(OFF)}$, $I_{D(OFF)}$	$V_S = +10V$, $V_D = -10V$, (Notes 1, 3)	—	—	90	—	—	100	nA
"ON" Leakage Current	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = +10V$, (Notes 1, 3)	—	—	90	—	—	100	nA
Logic "1" Voltage	V_{INH}	(Note 4)	2.0	—	—	2.0	—	—	V
Logic "0" Voltage	V_{INL}	(Note 4)	—	—	0.8	—	—	0.8	V
Logic "0" Current	I_{INL}	$V_{IN} = +0.4V$	—	—	5.0	—	—	7.0	μA
"ON" Switching Time	t_{ON}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$ (Note 2)	—	—	600	—	—	1000	ns
"OFF" Switching Time	t_{OFF}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$ (Note 2)	—	—	500	—	—	750	ns
Positive Supply Current	I+	Logic Inputs at "0" or "1"	—	—	13	—	—	13	mA
Negative Supply Current	I−	Logic Inputs at "0" or "1"	—	—	7.5	—	—	7.5	mA

NOTES:
1. The conditions listed specify the worst case leakage currents. The leakage currents apply equally to source S or drain D.
2. Guaranteed by design.
3. Tested at 125°C only for "A" and "B" grades.
4. Guaranteed by R_{ON} and leakage tests.

DICE CHARACTERISTICS



DIE SIZE 0.095 × 0.087 inch, 8265 sq. mils
(2.413 × 2.210 mm, 5.333 sq. mm)

SW-7510/SW-7511

1. NEGATIVE SUPPLY (SUBSTRATE)
2. GROUND
3. ADDRESS (A1)
4. ADDRESS (A2)
5. ADDRESS (A3)
6. ADDRESS (A4)
7. DISABLE (NO CONNECT)
8. POSITIVE SUPPLY
9. DRAIN (D4)
10. SOURCE (S4)
11. DRAIN (D3)
12. SOURCE (S3)
13. DRAIN (D2)
14. SOURCE (S2)
15. DRAIN (D1)
16. SOURCE (S1)

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at V+ = +15V, V− = −15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-7510N/ SW-7511N LIMIT	SW-7510G/ SW-7511G LIMIT	UNITS
"ON" Resistance	R_{ON}	V_D = 0V, I_{DS} = 1mA	75	100	Ω MAX
Logic "1" Voltage	V_{INH}	(Note 1)	2.0	2.0	V MIN
Logic "0" Voltage	V_{INL}	(Note 1)	0.8	0.8	V MAX
Logic "0" Current	I_{INL}	V_{IN} = +0.4V	3.5	3.5	μA MAX
Positive Supply Current	I+	Logic Inputs at "0"	9	9	mA MAX
Negative Supply Current	I−	Logic Inputs at "0"	5	5	mA MAX

NOTES:
1. Guaranteed by R_{ON} and leakage tests.

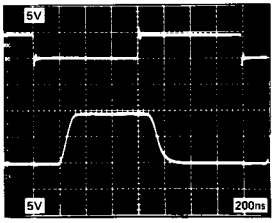
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = +15V, V− = −15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-7510N/ SW-7511N TYPICAL	SW-7510G/ SW-7511G TYPICAL	UNITS
"ON" Resistance	R_{ON}	V_D = 0V, I_{DS} = 1mA	60	80	Ω
R_{ON} vs. Temperature	R_{ON} Drift	V_D = 0V, I_{DS} = 1mA	0.4	0.5	%/°C
"ON" Switching Time	t_{ON}	V_S = −5V, R_L = 1kΩ, C_L = 7pF	350	450	ns
"OFF" Switching Time	t_{OFF}	V_S = −5V, R_L = 1kΩ, C_L = 7pF	260	350	ns

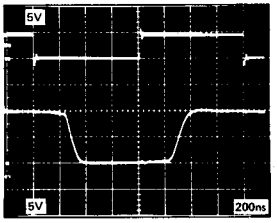
TYPICAL PERFORMANCE CHARACTERISTICS (Apply to all models, unless otherwise noted)

LARGE-SIGNAL SWITCHING



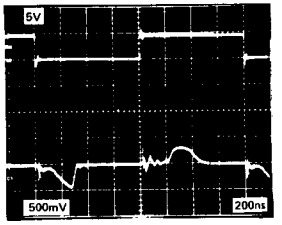
V_A = +10V, R_L = 1kΩ, C_L = 13pF

LARGE-SIGNAL SWITCHING



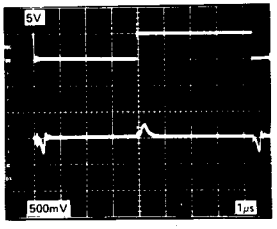
V_A = -10V, R_L = 1kΩ, C_L = 100pF

SMALL-SIGNAL SWITCHING



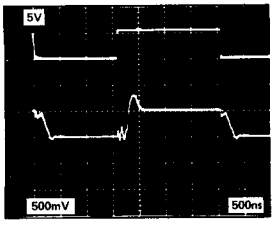
V_A = 0V, R_L = 1kΩ, C_L = 13pF

SMALL-SIGNAL SWITCHING WITH FILTERING



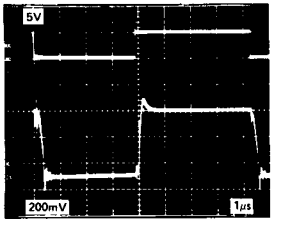
V_A = 0V, R_L = 1kΩ, C_L = 100pF

SMALL-SIGNAL SWITCHING



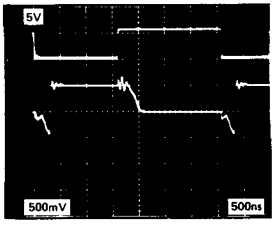
V_A = -500mV, R_L = 1kΩ, C_L = 13pF

SMALL-SIGNAL SWITCHING WITH FILTERING



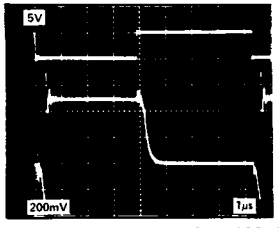
V_A = -500mV, R_L = 1kΩ, C_L = 100pF

SMALL-SIGNAL SWITCHING



V_A = 500mV, R_L = 1kΩ, C_L = 13pF

SMALL-SIGNAL SWITCHING WITH FILTERING

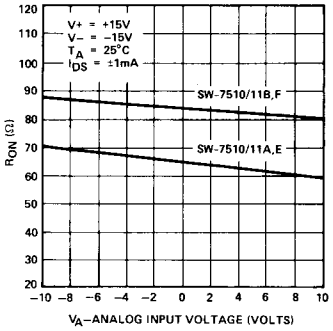


V_A = 500mV, R_L = 1kΩ, C_L = 100pF

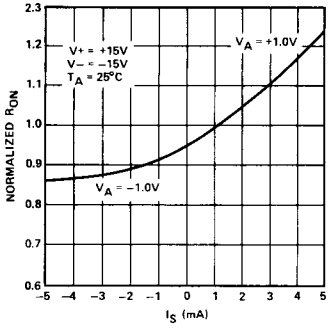
NOTE:
Upper Photo Traces: Logic Control Signal A_X (5V/DIV)
Lower Photo Traces: Switch Outputs V_D

TYPICAL PERFORMANCE CHARACTERISTICS (Apply to all models, unless otherwise noted)

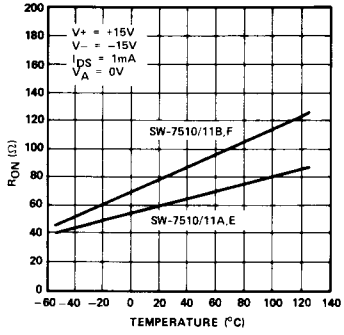
"ON" RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)



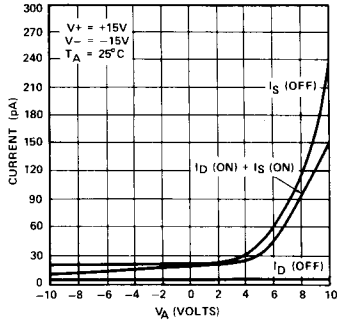
NORMALIZED R_{ON} vs SWITCH CURRENT (I_S)



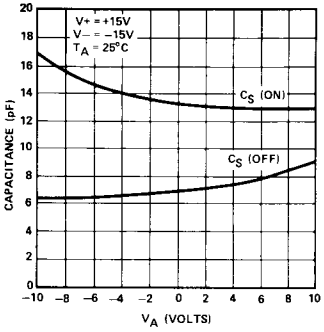
R_{ON} vs TEMPERATURE



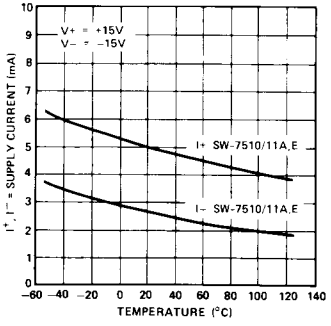
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE



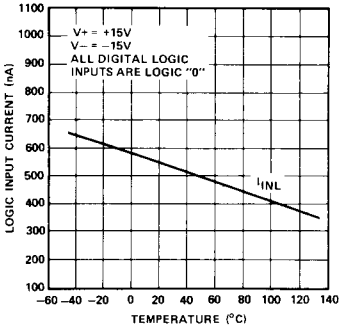
SWITCH CAPACITANCES vs ANALOG VOLTAGE (V_A)



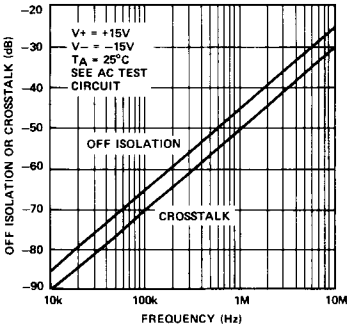
SUPPLY CURRENTS vs TEMPERATURE



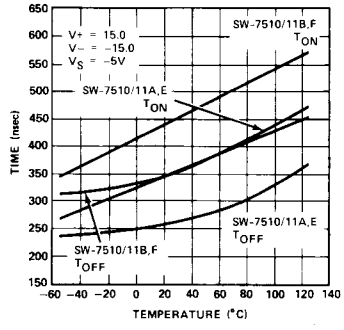
DIGITAL INPUT CURRENT I_{INL} vs TEMPERATURE



CROSSTALK AND "OFF" ISOLATION vs FREQUENCY

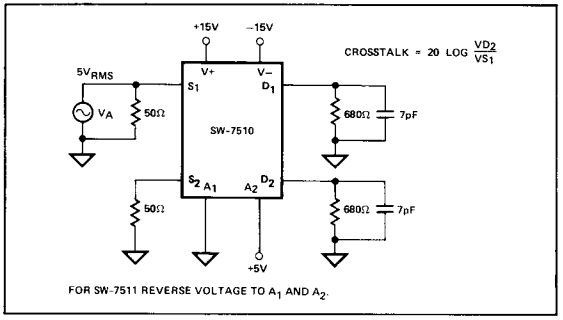


SWITCHING TIMES vs TEMPERATURE

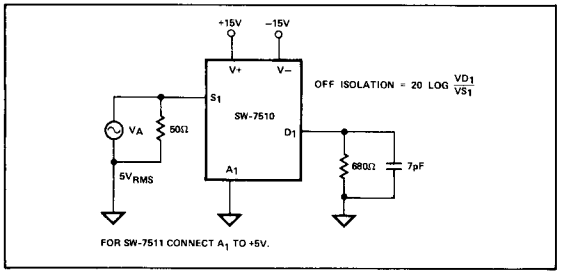


AC TEST CIRCUITS

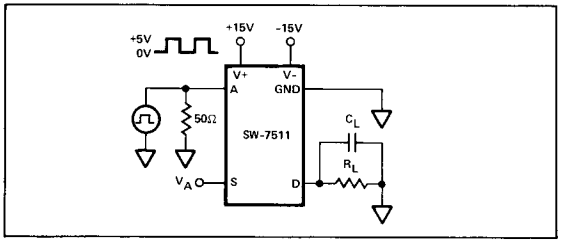
CROSSTALK MEASUREMENT CIRCUIT



ISOLATION MEASUREMENT CIRCUIT



SWITCHING TIME TEST CIRCUIT



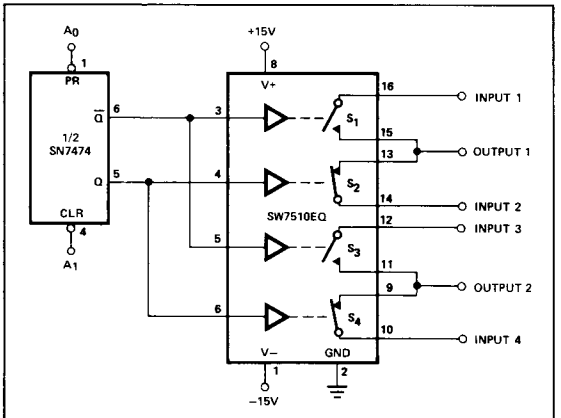
APPLICATIONS INFORMATION

This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P, and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

Proper switching requires the "Source" terminal be connected to the input driving signal.

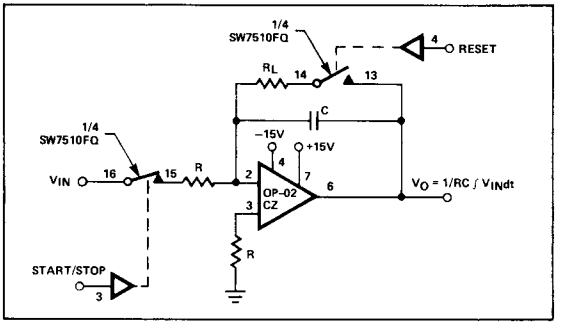
LATCHING DPDT SWITCH



Truth Table

Command		State of Switches After Command	
A_0	A_1	S2 and S3	S1 and S3
1	1	same	same
0	1	on	off
1	0	off	on
0	0	INDETERMINATE	

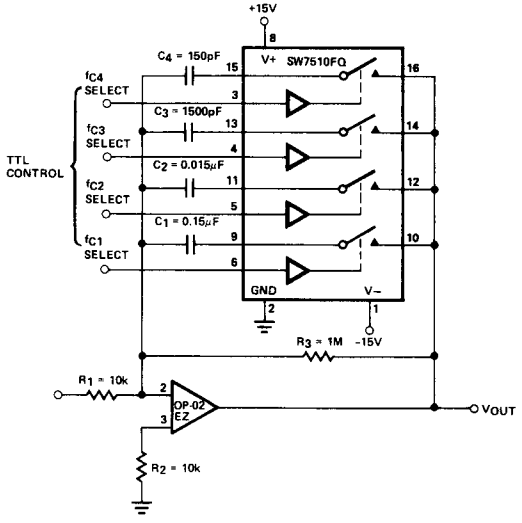
INTEGRATOR WITH ANALOG RESET AND START/STOP CAPABILITY

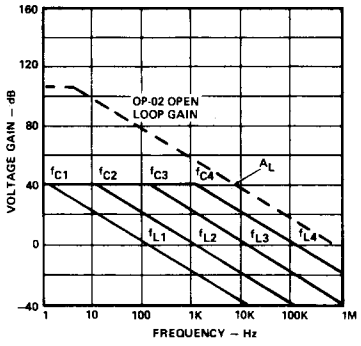


NOTE: Applications show SW-7510. For SW-7511 applications the logic is inverted.

TYPICAL APPLICATIONS

ACTIVE LOW-PASS FILTER WITH DIGITALLY SELECTED BREAK FREQUENCY





A_L (VOLTAGE GAIN BELOW BREAK FREQUENCY) =

$$\frac{R_3}{R_1} = 100\ (40dB)$$

$$f_C\ (\text{BREAK FREQUENCY}) = \frac{1}{2\pi R_3 C_X}$$

$$f_L\ (\text{UNITY GAIN FREQUENCY}) = \frac{1}{2\pi R_1 C_X}$$

NOTE: Applications show SW-7510. For SW-7511 applications the logic is inverted.