FEATURES

- **Members of the Texas Instruments Widebus™ Family**
- **Universal Bus Transceiver (UBT™) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Modes**
- **Translate Between GTL/GTL+ Signal Levels and LVTTL Logic Levels**
- **Support Mixed-Mode (3.3-V and 5-V) Signal Operation on A-Port and Control Inputs**
- **B-Port Transition Time Optimized for Distributed Backplane Loads**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on A-Port Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Distributed V_{CC} and GND-Pin Configuration Minimizes High-Speed Switching Noise**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Ceramic Flat (WD) Packages**

DESCRIPTION

The 'GTL16612A devices are 18-bit universal bus transceivers (UBT) that provide LVTTL-to-GTL+ and GTL+-to-LVTTL signal-level translation. They allow for transparent, latched, clocked, or clock-enabled modes of data transfer. These devices provide a high-speed interface between cards operating at LVTTL logic levels and backplanes operating at GTL+ signal levels. High-speed (about two times faster than standard LVTTL or TTL) backplane operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and output edge control (OEC™). Improved GTL+ OEC circuits minimize bus settling time and have been designed and tested using several backplane models.

Figure 1 shows actual device output waveforms using a synchronous clock at 75 MHz. The test backplane is a 16-slot, 14-inch board with loaded impedance of 33 Ω. V_{TT} is 1.5 V, V_{REF} is 1 V, and R_{TT} pullup resistor is 50 Ω. The driver is in slot 8, with receivers in alternate slots 1, 3, 5, 7, 10, 12, 14, and 16. Receiver slot-1 signals are shown. The signal becomes progressively worse as the receiver moves closer to the driver or the spacing between receiver cards is reduced. The clock is independent of the data, and the system clock frequency is limited by the backplane flight time to about 80-90 MHz. This frequency can be increased even more (30% to 40%) if the clock is generated and transmitted together with the data from the driver card (source synchronous).

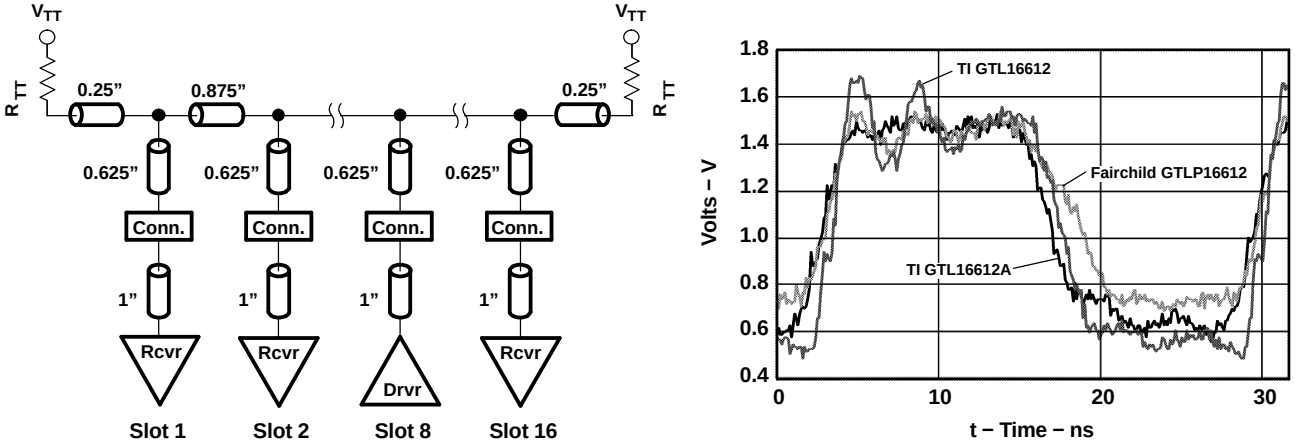


Figure 1. Test Backplane Model With Output Waveform Results

DESCRIPTION (CONTINUED)

Additional design considerations can be found in *Application Information* at the end of this data sheet.

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, clocked, and clock-enabled modes. These UBTs can replace any of the functions shown in Table 1.

Table 1. 'GTL16612A UBT Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	'245, '623, '645	'863	'861	'16245, '16623	'16863
Buffer/driver	'241, '244, '541		'827	'16241, '16244, '16541	'16825
Latched transceiver	'543			'16543	'16472
Latch	'373, '573	'843	'841	'16373	'16843
Registered transceiver	'646, '652			'16646, '16652	'16474
Flip-flop	'374, '574		'821	'16374	
Standard UBT					'16500, '16501
Universal bus driver					'16835
Registered transceiver with CLK enable	'2952			'16470, '16952	
Flip-flop with CLK enable	'377	'823			'16823
Standard UBT with CLK enable					'16600, '16601
'GTL16612A UBT replaces all above functions					

GTL+ is the Texas Instruments (TI™) derivative of the Gunning transceiver logic (GTL) JEDEC standard JESD 8-3. The AC specification of the 'GTL16612A is given only at the preferred higher noise margin GTL+, but this device can be used at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

The B port normally operates at GTL or GTL+ levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port.

To improve signal integrity, the 'GTL16612A B-port output transition time is optimized for distributed backplane loads.

V_{CC} (5 V) supplies the internal and GTL circuitry, while V_{CC} (3.3 V) supplies the LVTTL output buffers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ also is low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that for A to B, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

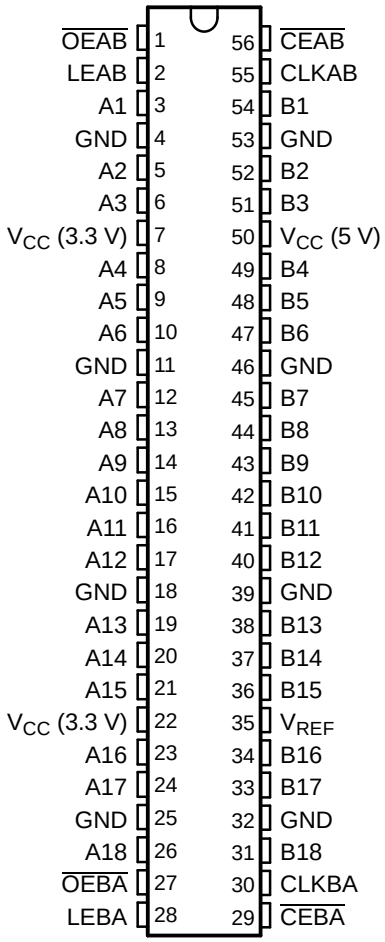
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

The SN54GTL16612A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74GTL16612A is characterized for operation from –40°C to 85°C.

SN54GTL16612A . . . WD PACKAGE
SN74GTL16612A . . . DGG OR DL PACKAGE
(TOP VIEW)

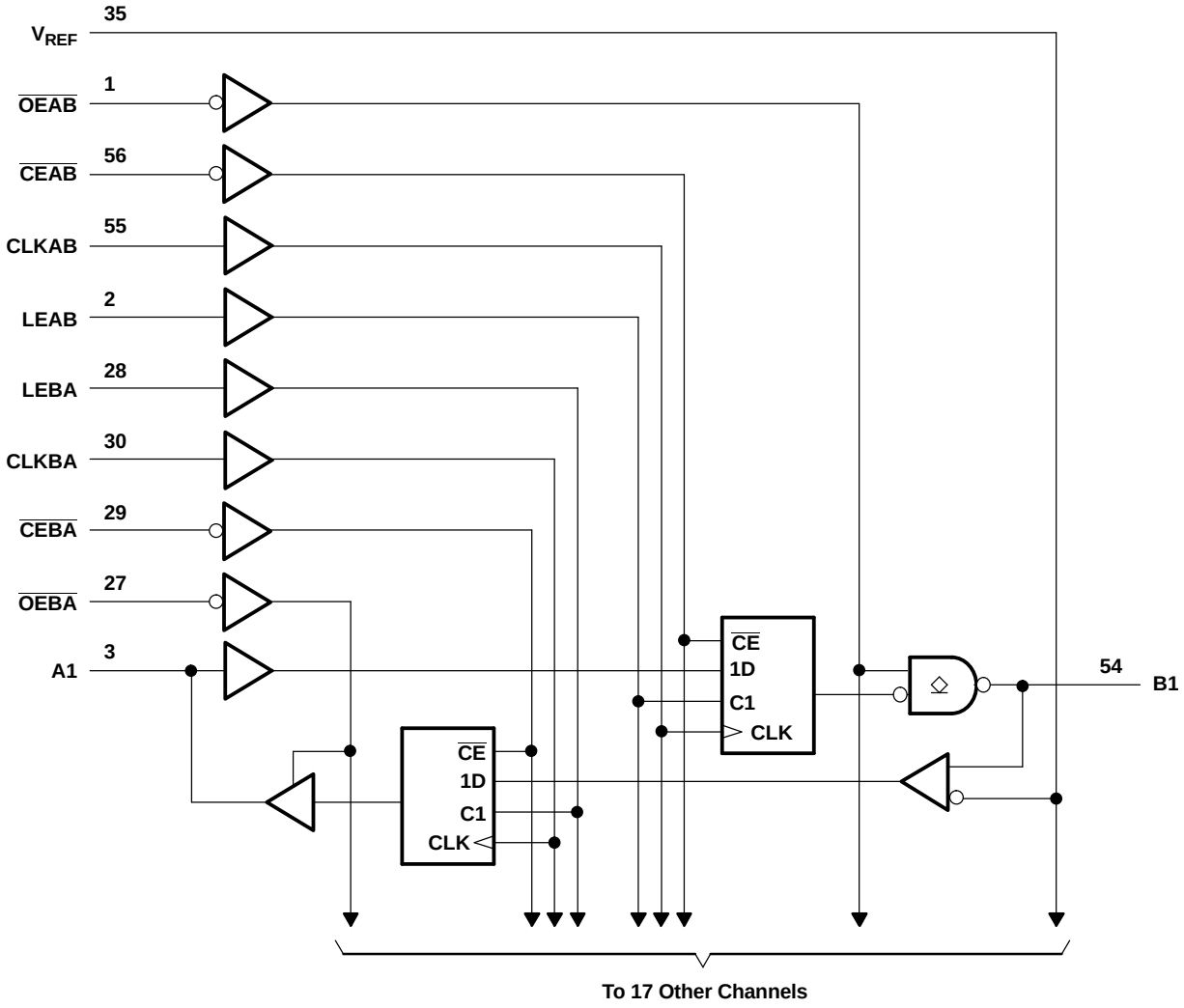


FUNCTION TABLE(1)

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0(2)	Latched storage of A data
L	L	L	L	X	B_0(3)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0(3)	Clock inhibit

(1) A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.
(2) Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
(3) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	3.3 V	–0.5	4.6	V
		5 V	–0.5	7	
V_I	Input voltage range(2)	A-port and control inputs	–0.5	7	V
		B port and V_{REF}	–0.5	4.6	
V_O	Voltage range applied to any output in the high or power-off state(2)	A port	–0.5	7	V
		B port	–0.5	4.6	
I_O	Current into any output in the low state	A port		128	mA
		B port		80	
I_O	Current into any A-port output in the high state(3)			64	mA
	Continuous current through each V_{CC} or GND			±100	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance(4)	DGG package		64	°C/W
		DL package		56	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions(1)(2)(3)

			SN54GTL16612A			SN74GTL16612A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	3.3 V	3.15	3.3	3.45	3.15	3.3	3.45	V
		5 V	4.75	5	5.25	4.75	5	5.25	
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	1.35	1.5	1.65	
V_{REF}	Supply voltage	GTL	0.74	0.8	0.87	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}			V_{TT}	V
		Except B port			5.5			5.5	
V_{IH}	High-level input voltage	B port	V_{REF} + 50 mV			V_{REF} + 50 mV			V
		Except B port	2			2			
V_{IL}	Low-level input voltage	B port			V_{REF} – 50 mV			V_{REF} – 50 mV	V
		Except B port			0.8			0.8	
I_{IK}	Input clamp current				–18			–18	mA
I_{OH}	High-level output current	A port			–32			–32	mA
I_{OL}	Low-level output current	A port			64			64	mA
		B port			34			34	
T_A	Operating free-air temperature		–55		125	–40		85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) Normal connection sequence is GND first, V_{CC} = 5 V second, and V_{CC} = 3.3 V, I/O, control inputs, V_{TT}, and V_{REF} (any order) last.
(3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances as long as they do not exceed the DC absolute I_{OL} ratings. Similarly, V_{REF} can be adjusted to optimize noise margins, but normally is 2/3 V_{TT}.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54GTL16612A			SN74GTL16612A			UNIT
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IK}		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	A port	V_{CC} (3.3 V) = 3.15 V to 3.45 V, V_{CC} (5 V) = 4.75 V to 5.25 V	I_{OH} = –100 µA	V_{CC} (3.3 V) – 0.2			V_{CC} (3.3 V) – 0.2			V
		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OH} = –8 mA	2.4			2.4			
			I_{OH} = –32 mA	2			2			
V_{OL}	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 64 mA			0.6			0.55	
	B port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V, I_{OL} = 34 mA				0.65			0.65	
I_I	Control inputs	V_{CC} (3.3 V) = 0 or 3.45 V, V_{CC} (5 V) = 0 or 5.25 V	V_I = 5.5 V			10			10	µA
	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = 5.5 V			1000			20	
			V_I = V_{CC} (3.3 V)			1			1	
			V_I = 0			–30			–30	
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = V_{CC} (3.3 V)			5			5	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			1000			100	µA
$I_{I(hold)}$	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	–75			–75			
			V_I = 0 to V_{CC} (3.3 V)(2)			±500			±500	
I_{OZH}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_O = V_{CC} (3.3 V)			1			1	µA
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 1.5 V				10			10	
I_{OZL}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 0				–1			–1	µA
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 0.65 V				–10			–10	
I_{CC} (3.3 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND(3), V_I = V_{TT} or GND(4)	Outputs high			1			1	mA
			Outputs low			5			5	
			Outputs disabled			1			1	
I_{CC} (5 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND(3), V_I = V_{TT} or GND(4)	Outputs high			120			120	mA
			Outputs low			120			120	
			Outputs disabled			120			120	
ΔI_{CC} (3.3 V)(5)		V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, One A-port or control input at 2.7 V, Other A-port or control inputs at V_{CC} (3.3 V) or GND				1			1	mA
C_i	Control inputs	V_I = 3.15 V or 0			4	12		4		pF
C_{io}	A port	V_O = 3.15 V or 0			8.5	18		8.5		pF
	B port	V_O = 1.5 V or 0				10		8		

(1) All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) This is the V_I for A-port or control inputs.
(4) This is the V_I for B port.
(5) This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (unless otherwise noted) (see Figure 2)

			SN54GTL16612A(1)		SN74GTL16612A		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			85		85	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		3.3		ns
		CLKAB or CLKBA high or low	5.7		5.7		
t_{su}	Setup time	A before CLKAB↑	1		1		ns
		B before CLKBA↑	2.7		1.8		
		A before LEAB↓	1.7		0.5		
		B before LEBA↓	1.2		1.2		
		$\overline{CEAB}$ before CLKAB↑	1.3		1.2		
		$\overline{CEBA}$ before CLKBA↑	1.8		1.4		
t_h	Hold time	A after CLKAB↑	3.2		1.9		ns
		B after CLKBA↑	4.3		0.5		
		A after LEAB↓	3.2		2.7		
		B after LEBA↓	4.2		3.5		
		$\overline{CEAB}$ after CLKAB↑	2.4		1.2		
		$\overline{CEBA}$ after CLKBA↑	1.1		1.1		

(1) Product preview

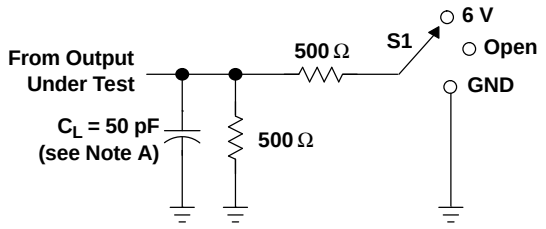
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16612A(1)			SN74GTL16612A			UNIT
			MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
f_{max}			85			85			MHz
t_{PLH}	A	B	2		7.3	2.5		6.9	ns
t_{PHL}			2.2		7.4	2.5		6.9	
t_{PLH}	LEAB	B	2.2		7.5	3.2		7.3	ns
t_{PHL}			2.3		7.9	3.2		7.3	
t_{PLH}	CLKAB	B	2.1		8	3.4		7.8	ns
t_{PHL}			2.5		7.9	3.4		7.8	
t_{en}	$\overline{OEAB}$	B	1.8		7.4	2.8		7	ns
t_{dis}			1.8		7	2.8		7	
t_r	Transition time, B outputs (20% to 80%)			2.6			2.6		ns
t_f	Transition time, B outputs (80% to 20%)			2.6			2.6		ns
t_{PLH}	B	A	1.4		6.3	1.5		5.7	ns
t_{PHL}			1.3		6.2	1.5		5.7	
t_{PLH}	LEBA	A	1.5		6.1	1.8		5.7	ns
t_{PHL}			1		6	1.8		5.7	
t_{PLH}	CLKBA	A	1.8		5.8	2.3		5.5	ns
t_{PHL}			2		5.9	2.3		5.5	
t_{en}	$\overline{OEBA}$	A	0.5		6.2	1.8		6.1	ns
t_{dis}			1.3		6.6	1.8		6.1	

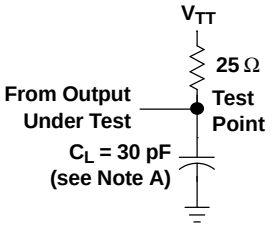
(1) Product preview
(2) All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

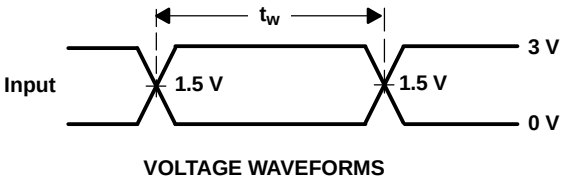


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

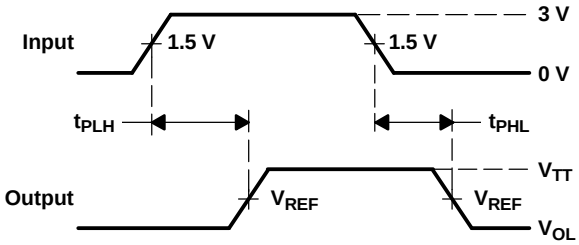
LOAD CIRCUIT FOR A OUTPUTS



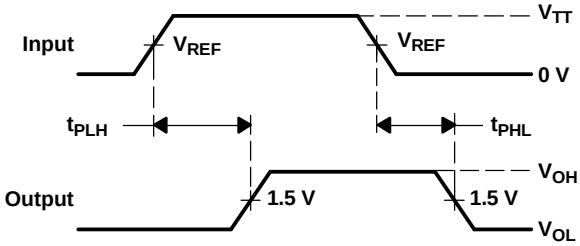
LOAD CIRCUIT FOR B OUTPUTS



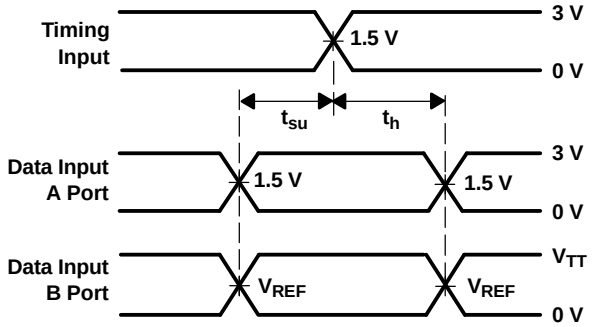
VOLTAGE WAVEFORMS
PULSE DURATION



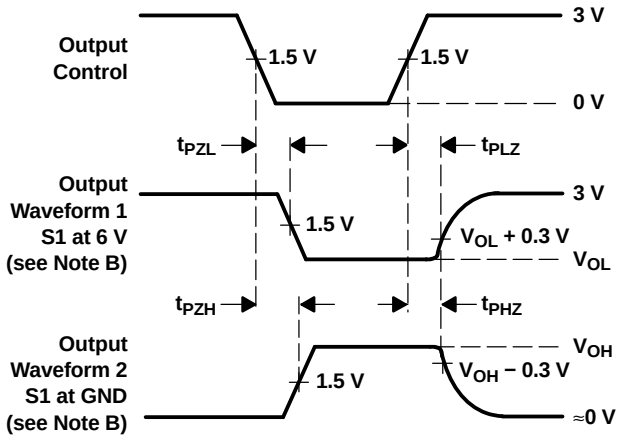
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

APPLICATION INFORMATION

GTL Background Information

GTL was approved as JEDEC standard JESD 8-3 in 1993 and originally was created as a reduced-swing I/O driver technology to support high-speed buses and backplanes. The GTL bus is designed to work with low voltage swings. The input buffer works like an analog comparator rather than like an inverter, which allows the GTL inputs to switch quickly without needing to be driven rail to rail. GTL drivers were designed to pull a 1.2-V signal down to 0.4 V when switched on. This, however, placed the reference voltage for the input comparator at 0.8 V, which made it susceptible to ground-bounce noise. A variant of GTL, called GTL+, is being used to address this noise-margin concern. The GTL+ termination voltage is raised to 1.5 V, with the driver pulling down to a V_{OL} of 0.5 V. This moved the reference voltage to 1 V and out of the range of most ground bounces.

TI GTL devices operate at, and are specified for, both GTL and the improved-noise-margin GTL+ standard. However, the 'GTL16612A devices deviate from this history. They are designed with slow rising and falling edges, to offer significant system frequency improvement in heavily loaded backplanes. They are AC specified only at GTL+ because most applications are moving to this improved-noise-margin standard; they operate at either GTL or GTL+.

Devices named GTL or GTLP indicate reduced voltage-swing operation at a V_{TT} of 1.2 V (GTL standard) or 1.5 V (improved-noise-margin GTL+ standard). Fast-edge GTL devices are best for point-to-point or lower-frequency backplanes. Slow-edge GTL devices extend backplane operations to cover even higher frequencies.

Input Characteristics

The input characteristics are identical on both A and B ports. Both ports are very high impedance and have an input diode to provide protection against high negative-voltage spikes. The input diode conducts and prevents more sensitive components from being destroyed as the result of electrostatic discharges or line reflections.

GTL Output Characteristics

The principle of the GTL bus is based on open-drain drivers, as shown in Figure 3.

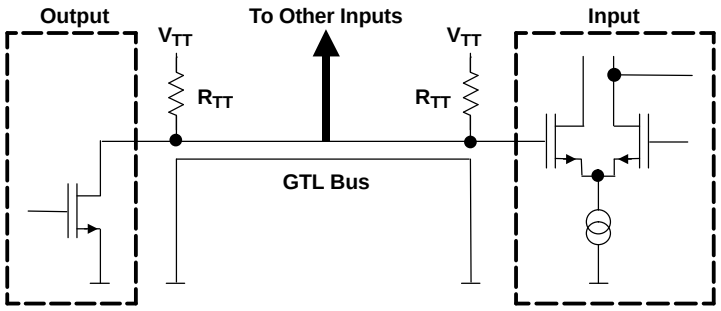


Figure 3. GTL Bus: An Open-Drain Bus

The devices actively drive the bus low, whereas, the termination voltage source (V_{TT}) pulls it high. Only the pullup resistor (R_{TT}), which usually is of a low resistance, limits the current. The pullup resistor value should match the fully loaded backplane impedance, not the trace impedance, to provide an optimum termination of the bus and avoid line reflections. The resistance of the GTL output is in the range of a few ohms. However, in the high state, the output transistor is in the high-impedance state. R_{TT} needs to be greater than 25 Ω at GTL+ signal levels, not to exceed the 'GTL16612A absolute maximum output current of 80 mA, and should be greater than 50 Ω at GTL+ signal levels, not to exceed the recommended output current limit of 34 mA.

APPLICATION INFORMATION

OEC

The 'GTL16612A GTL output consists of an improved edge-control circuit that provides optimized rise and fall times, typically 2.6 ns (20% to 80%), for backplanes under various loading conditions.

Using the definition of slew rate $\Delta t/\Delta v = t_r$ or $t_f/(V_{OH} - V_{OL})$, the slew rate of the device typically is 5 ns/V. As a comparison, these values are significantly more than those of previous GTL or standard TTL devices, which are usually about 1 ns/V, or less.

Termination Voltage, V_{TT}

The termination voltage (V_{TT}) should be derived from a voltage regulator that can provide up to 50-mA current per signal line. There are various voltage regulators that meet these requirements. Depending on the application, the regulators should be mounted either directly on the backplane or on the daughter boards. It is highly recommended that ceramic bypass capacitors be used (due to high impedance) at the termination resistors because several signal lines may be switching simultaneously, causing considerable current fluctuations at the termination voltage.

Reference Voltage, V_{REF}

The GTL reference voltage (V_{REF}) can be derived using a simple voltage divider between V_{TT} and GND with an R-to-2R ratio and a bypass capacitor (0.01–0.1 μF) as close to the V_{REF} terminal as possible (see Figure 4). Generating V_{REF} from V_{TT} ensures the maximum possible signal-to-noise ratio (SNR) even with an unstable termination voltage. It also is recommended to generate V_{REF} locally on each plug-in card, instead of on the backplane.

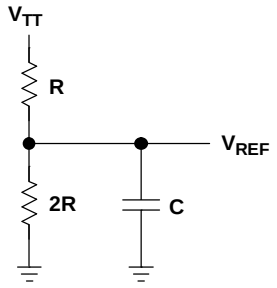


Figure 4. Suggested Connection of V_{REF} Terminal

Partial Power Down

Device power can be switched off without having to remove the device from the system. This is a partial power down. 'GTL16612A can be used in a partial-power-down application where V_{CC} = 0 because the inputs and outputs are at high impedance and are able to tolerate active bus signals. This is reflected in the I_{off} parameter, which specifies the maximum input or output leakage current.

Bus-Hold Circuit

Bus hold on A-port inputs (LVTTL side) prevents any unused or floating inputs from damaging the device. To change the logic state stored by the bus-hold circuit, a current of about 250-300 μA must be overridden. There is no bus hold on the B port (GTL side). A bus-hold circuit on the GTL side would defeat the purpose of the open-drain outputs, which take on the high-impedance state to allow the bus to achieve a logic high state via the pullup resistors.

APPLICATION INFORMATION

Source-Synchronous Clock Applications

When the clock originates at the driver card and is carried out with the data, the backplane maximum frequency can be achieved. This is possible because the backplane flight time no longer is the limiting factor.

Figure 5 shows results of the 'GTL16612A operating at 100 MHz in a source-synchronous mode.

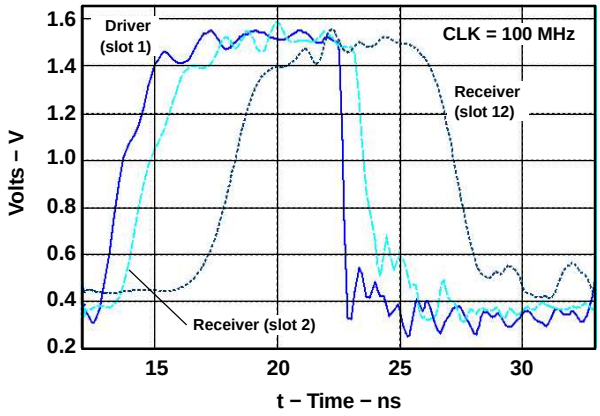


Figure 5. Source-Synchronous Clock

Summary

'GTL16612A devices provide significant benefits when designing high-speed parallel backplanes.

- B port specifically optimized for distributed backplane levels
- Improved B-port GTL edge-control circuitry provides better signal integrity at higher frequencies.
- Reduced power consumption over BTL technology
- Similar to 'LVTH16601, with the B port operating at GTL+ signal levels
- Data throughput is 1.35 Gbit/s at 75-MHz clock speed.
- Provide about two times the data throughput over existing TTL devices, using existing parallel backplane designs

Additional information on GTL devices and backplane design considerations can be found at http://www.ti.com/sc/gtl.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74GTL16612ADGGR	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
SN74GTL16612ADL	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
SN74GTL16612ADLR	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		

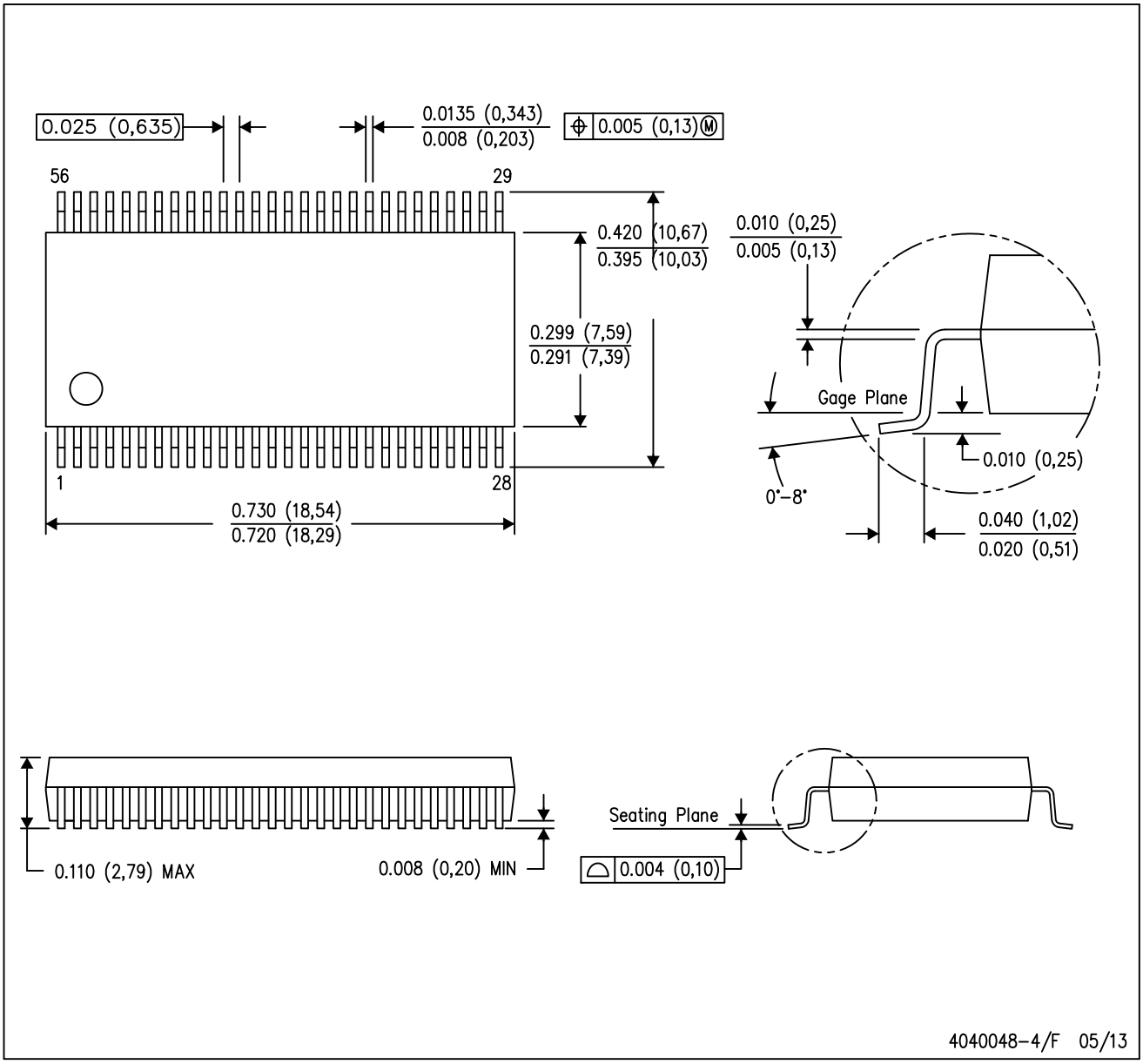
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

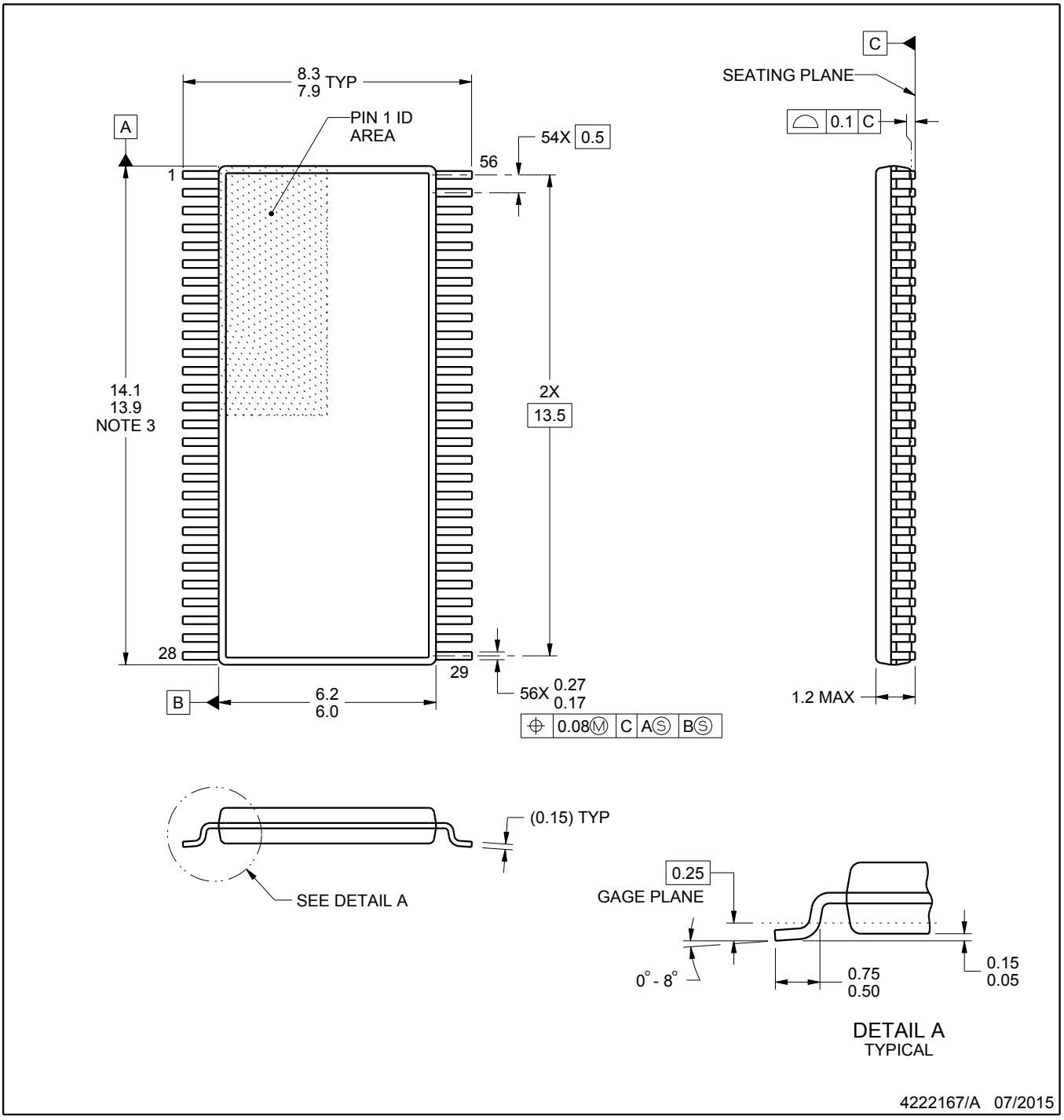
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DGG0056A

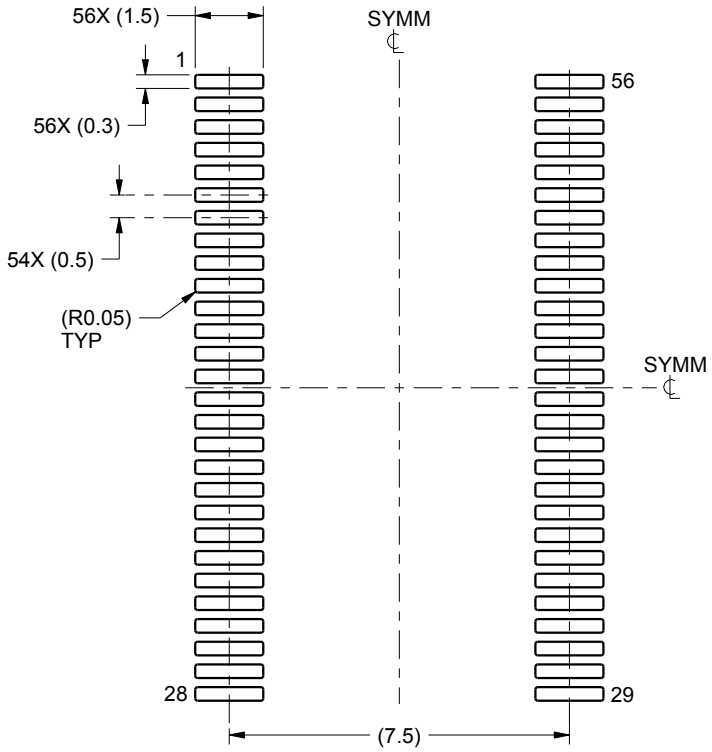
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

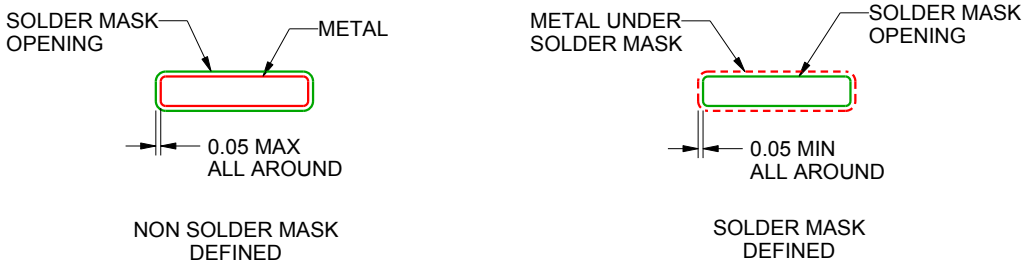


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

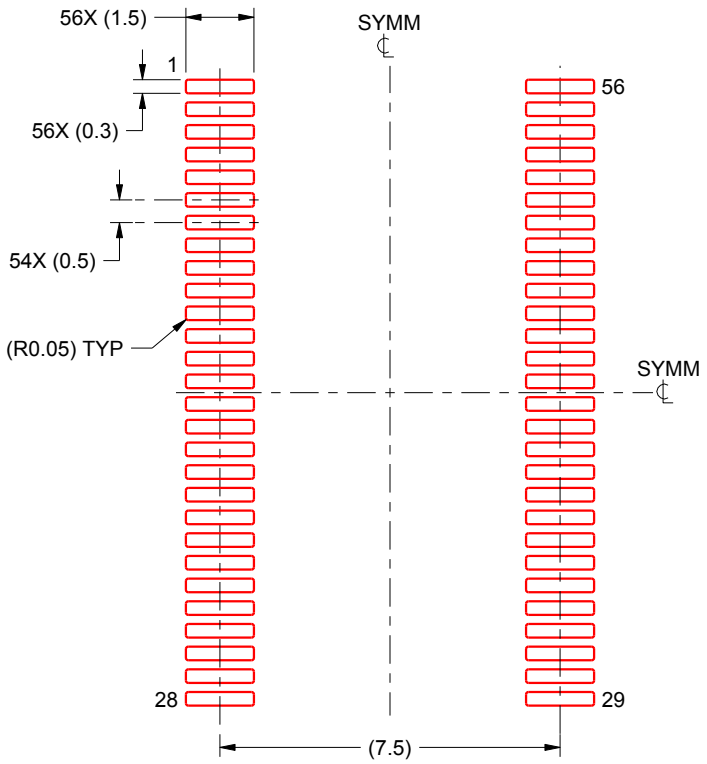


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265