Semiconductor Corporation

CS4303

107 dB, D/A Converter for Digital Audio

2

Features

- Stereo Delta-Sigma D/A converter
  8× Interpolation Filter
  64× Delta-Sigma DAC
- Single +5V Operation
- Adjustable System sampling Rates including 32 kHz, 44.1 kHz and 48 kHz
- 107 dB Dynamic Range Over the Audio Bandwidth
- ±0.0002 dB Passband Ripple
- Flexible Serial Input Port
  Supports Multiple Input Formats
  16 or 18 Bit Input Words

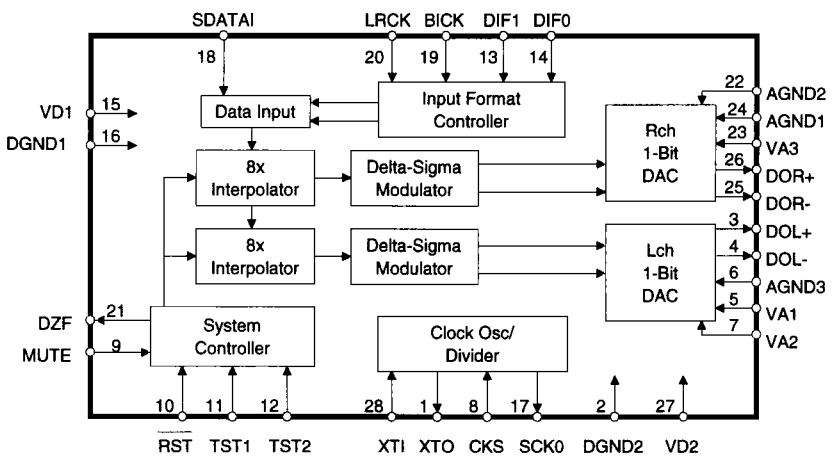
General Description

The CS4303 is a high performance delta-sigma D/A converter for digital audio systems which require wide dynamic range. The CS4303 includes 8× interpolation and a 64× oversampled delta-sigma modulator that outputs a 1-bit signal to an external analog low pass filter. The 1's density of the 1-bit signal is proportional to the digital input.

The CS4303 has a configurable input serial port that provides four interface formats. The master clock rate can be either 256 or 384 times the input word rate, supporting various audio environments.

Ordering Information:

Model	Temp. Range	Package Type
CS4303-KS	0° to 70°C	28-pin plastic SOIC
CS4303-KP	0° to 70°C	28-pin plastic DIP



Preliminary Product Information This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS (T_A = 25°C; VD1, VA1, VA2, VA3, VD2 = +5.0V ; Full-scale Output Sinewave, 991 Hz; Input Word Rate = 48 kHz; BICK = 3.072 MHz; Logic "1" = VD, Logic "0" = DGND)

Parameter			Symbol	Min	Typ	Max	Units
Dynamic Performance							
Dynamic Range	(Note 1)			-	107	-	dB
Total Harmonic Distortion + Noise	(digital fullscale input)		THD+N	-	100	-	dB
Interchannel Isolation				-	115	-	dB
Power supplies							
Power Supply Current	$\overline{RST}$ = High:	VD1		-	27	-	mA
		VA1, VA2, VA3		-	4	-	mA
		VD2		-	2	-	mA
	$\overline{RST}$ = Low:	VD1		-	5	-	mA
		VA1, VA2, VA3		-	0.1	-	mA
		VD2		-	1	-	mA
Power Dissipation	($\overline{RST}$ = High)			-	165	300	mW

Note 1. Assumes ideal conversion of 1-bit data to an analog signal

DIGITAL FILTER CHARACTERISTICS (T_A = 25°C; VD1, VA1, VA2, VA3, VD2 = +5V± 5%; Input Word Rate = 48 kHz)

Parameter		Symbol	Min	Typ	Max	Units
Pass Band	±0.0002 dB corner		0	-	21.8	kHz
	to -3 dB corner		0	-	23.5	kHz
Stop Band			26.2	-	-	kHz
Pass Band Ripple			-	-	±0.0002	dB
Stop Band Attenuation			90	-	-	dB
Group Delay	(IWR = Input Word Rate)		-	33/IWR	-	s
Deviation from Linear Phase			-	-	0	deg

ABSOLUTE MAXIMUM RATINGS (AGND1, AGND2, AGND3, DGND1, DGND2 = 0V; All Voltages With Respect to Ground)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:					
Positive Digital		VD	-0.3	6.0	V
Positive Analog	(VA1,VA2,VA3,VD2)	VA	-0.3	6.0	V
|VA - VD|			-	0.4	V
Input Current		I_{IN}	-	±10	mA
Digital Input Voltage			-0.3	VD + 0.3	V
Ambient Operating Temperature			-10	70	°C

Specifications are subject to change without notice.

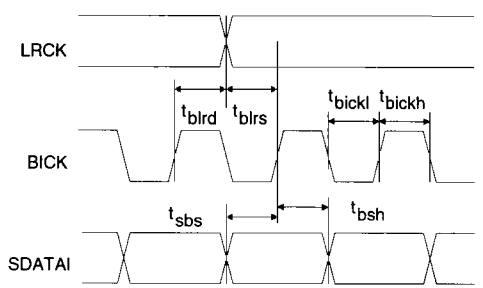
DIGITAL CHARACTERISTICS (T_A = 25°C; VD1, VA1, VA2, VA3, VD2 = 5V ± 5%; Input Word Rate = 48 kHz)

Parameter		Symbol	Min	Typ	Max	Units
Digital Input Voltage	High-level	V_{IH}	VD - 1.0	-	-	V
	Low-level	V_{IL}	-	-	1.0	V
Digital Output Voltage	High-level I_o = -20µA	V_{OH}	4.4	-	-	V
	Low-level I_o = +20µA	V_{OL}	-	-	0.1	V
Input Leakage Current		I_{IN}	-	±1.0	-	µA

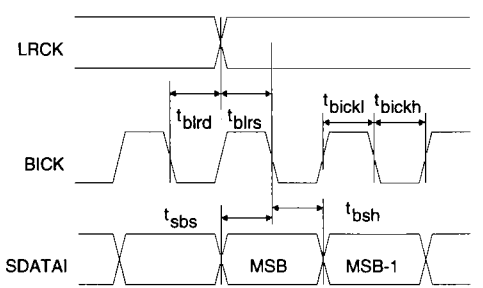
SWITCHING CHARACTERISTICS (T_A = 25 °C; VA1, VA2, VA3, VD1, VD2 = 5V ± 5%; Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
Master Clock Frequency using Internal Oscillator:						
CKS=H	(384 x Fs)	XTI/XTO	10.7	-	19.2	MHz
CKS=L	(256 x Fs)	-	7.1	-	13.9	MHz
Master Clock Frequency using External Clock:						
CKS=H	(384 x Fs)	XTI/XTO	0.384	-	19.2	MHz
CKS=L	(256 x Fs)	-	0.256	-	13.9	MHz
XTI/XTO Pulse Width Low			21	-	-	ns
XTI/XTO Pulse Width High			21	-	-	ns
BICK Pulse Width Low		t_{bickl}	30	-	-	ns
BICK Pulse Width High		t_{bickh}	30	-	-	ns
BICK Period		t_{bickw}	80	-	-	ns
BICK rising to LRCK edge delay	(Note 2)	t_{blrd}	35	-	-	ns
BICK rising to LRCK edge setup time	(Note 2)	t_{blrs}	35	-	-	ns
SDATAI valid to BICK rising setup time	(Note 2)	t_{sbs}	35	-	-	ns
BICK rising to SDATAI hold time	(Note 2)	t_{bsh}	35	-	-	ns
RST Minimum Pulse Width Low			2 periods of XTI/XTO			

Note: 2. "BICK rising" refers to modes 0, 1, and 3. For mode 2, replace "BICK rising" with "BICK falling."



Serial Data Input Timing (Modes 0, 1 and 3)



Serial Data Input Timing (Mode 2)

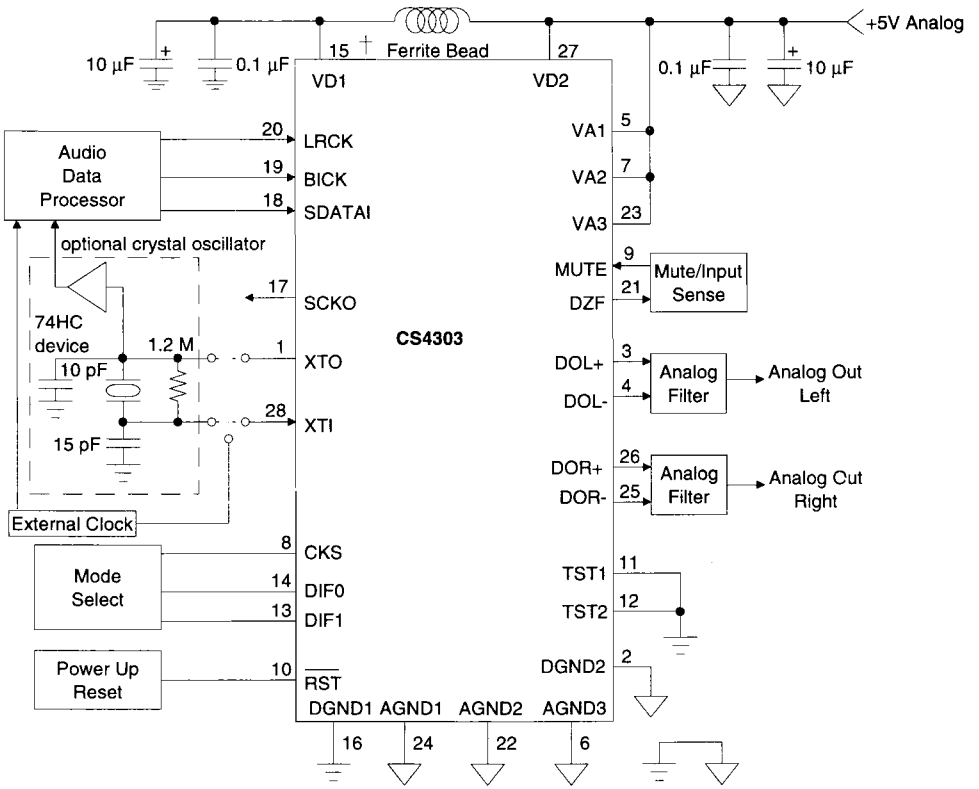


Figure 1. CS4303 Typical Connection Diagram

GENERAL DESCRIPTION

The CS4303 is a stereo digital-to-analog system designed for digital audio. The system accepts data at standard audio frequencies, such as 48 kHz, 44.1 kHz, and 32 kHz. The architecture includes an 8× oversampling filter followed by a 64× oversampled one-bit delta-sigma modulator and 1-bit DAC as shown in Figure 2. The 1-bit data is passed through an external analog low-pass filter to produce the audio signal.

The primary purpose of using delta-sigma modulation techniques is to avoid the limitations of laser trimmed resistive DAC architectures by using an inherently linear 1-bit DAC. The advantages of a 1-bit DAC include: ideal differential linearity, no distortion mechanisms due to resistor matching errors and no linearity drift over time and temperature due to variations in resistor values.

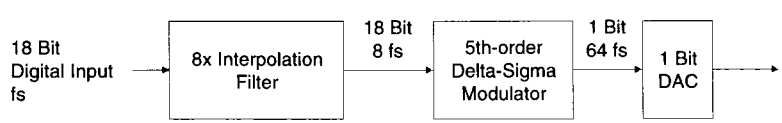


Figure 2. CS4303 Architecture

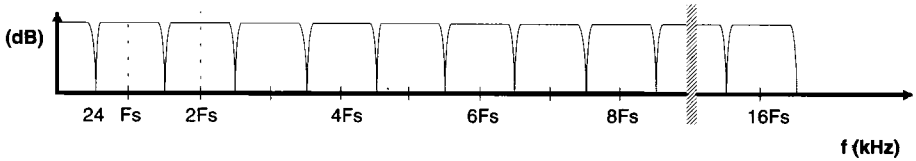


Figure 3. CS4303 Interpolation Filter Input

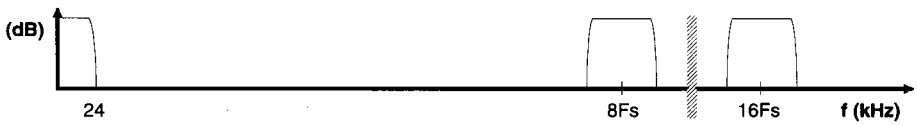


Figure 4. CS4303 Interpolation Filter Output

Digital Interpolation Filter

The digital interpolation filter increases the sample rate by a factor of 8 and eliminates images of the baseband audio signal which exist at multiples of the input sample rate, Fs (Figure 3). This allows for the selection of a less complex analog filter based on out-of-band noise attenuation requirements rather than anti-image filtering. Following the interpolation filter, the resulting frequency spectrum (Figure 4) has images of the input signal at multiples of eight times the input sample rate, 8Fs. These images are removed by the analog filter required to filter the 1-bit data.

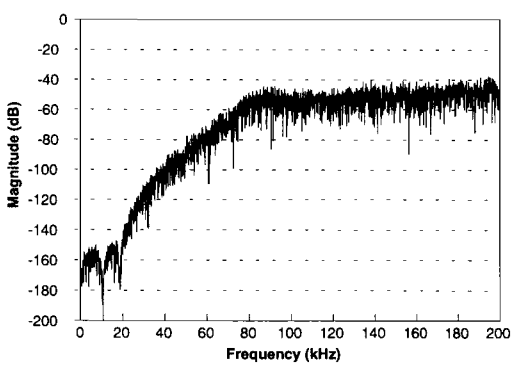


Figure 5. 1-bit Modulator Output (Fs = 48 kHz)

Delta-Sigma Modulator

The interpolation filter is followed by a fifth-order delta-sigma modulator which converts the 8Fs multi-bit interpolation filter output into 1-bit data at 64 times Fs. The frequency spectrum of the 1-bit delta- sigma modulator output is shown in Figure 5 for an Fs of 48 kHz.

One-Bit DAC

The CS4303 incorporates a differential output to maximize the output level and minimize the amount of gain required in the analog filter. Figure 6 shows each output as well as the differentially summed output for an arbitrary 1-bit data stream.

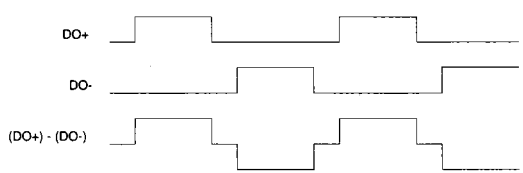


Figure 6. CS4303 Differential Outputs

Return-to-zero coding is utilized where each occurence of a 1 is 75% high and returns low for 25% of the bit period as shown in Figure 7. This technique ensures that the energy within each 1 includes the effects of finite rise and fall times regardless of the previous or next state and minimizes distortion.

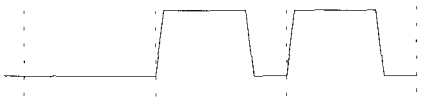


Figure 7. Return to Zero Encoding

SYSTEM DESIGN

System Clock Input

The master clock (XTI/XTO) input to the DAC is used to operate the digital interpolation filter and the delta-sigma modulator. The master clock can be either a crystal placed across the XTI and XTO pins, or an external clock input to the XTI pin with the XTO pin left floating.

The frequency of XTI/XTO is determined by the desired Input Word Rate, IWR, and the setting of the Clock Select pin, CKS. IWR is the frequency at which words for each channel are input to the DAC and is equal to the LRCK frequency. Setting CKS low selects an XTI/XTO frequency of 256× IWR while setting CKS high selects 384× IWR. Table 1 illustrates various audio word rates and corresponding frequencies used in the DAC.

The remaining system clocks, LRCK and BICK, must be synchronously derived from XTI/XTO. If the CS4303 internal oscillator is used, the circuit must be configured and XTO buffered as shown in Figure 1. XTI/XTO can be divided to produce LRCK and BICK using a synchronous counter such as 74HC590. Notice that the value of the capacitor on XTO is 10 pF and the XTI capacitor is 15 pF, which allows for 5 pF of gate and stray capacitance.

LRCK (kHz)	CKS	XTI/XTO (MHz)
32	low	8.192
44.1	low	11.2896
44.1	high	16.9344
48	low	12.288

Table 1. Common Clock Frequencies

Serial Data Interface

Data is input to the CS4303 via three serial input pins; SDATAI is the serial data input, BICK is the serial data clock and LRCK defines the channel and delineation of data. The DAC supports four serial data formats which are selected via the digital input format pins DIF0 and DIF1. The different formats control the relationship of LRCK to SDATAI and the edge of BICK used to latch data. Table 2 lists the four formats, along with the associated figure number. Format 0 is compatible with existing 16-bit D/A converters and digital filters. Format 1 is an 18-bit version of format 0. Format 2 is similar to Crystal ADCs and many DSP serial ports. Format 3 is compatible with the I^2S serial data protocol. Formats 2 and 3 support 18-bit input or 16-bit followed by two zeros. In all four serial input formats, the serial data is MSB-first and 2's-complement format.

Formats 0, 2 and 3 will operate with 16-bit data and 16 BICK pulses as well. See Figure 11 for

DIF1	DIF0	Format	Figure
0	0	0	8
0	1	1	8
1	0	2	9
1	1	3	10

Table 2. Digital Input Formats

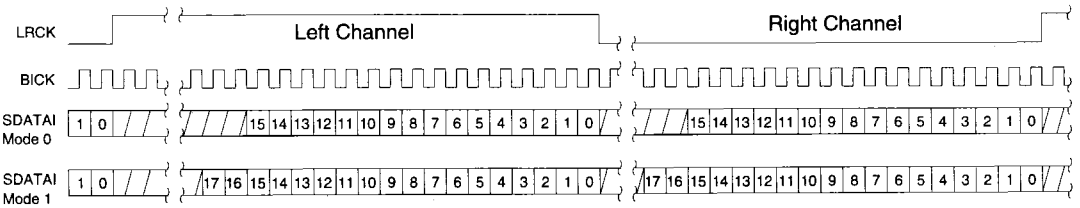


Figure 8. Digital Input Formats 0 & 1

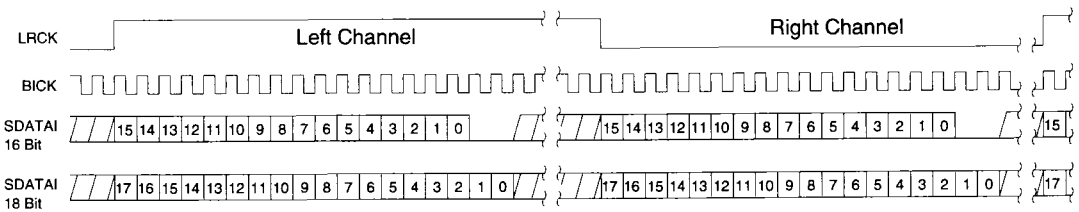


Figure 9. Digital Input Format 2

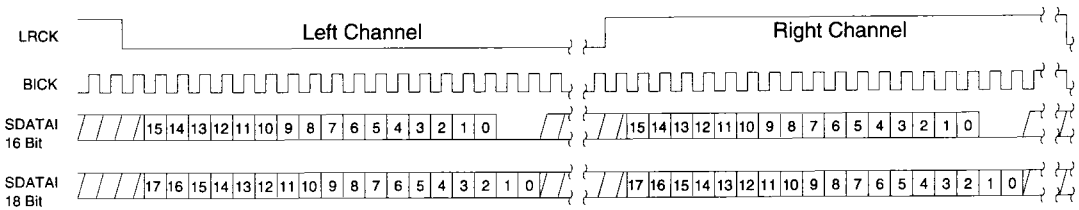


Figure 10. Digital Input Format 3

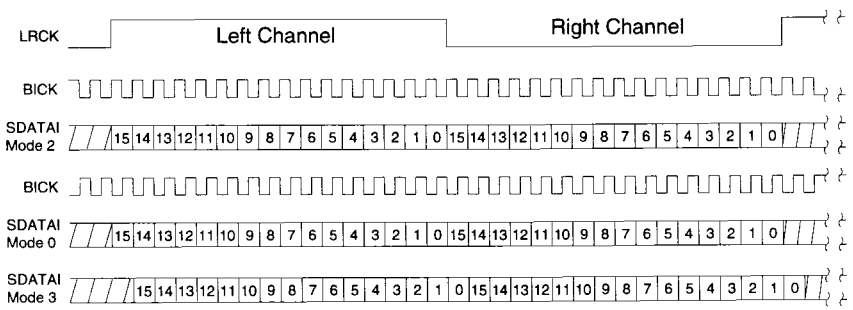


Figure 11. Digital Input Formats 0, 2 and 3 with 16 BICK Periods

16-bit timing. However, the use of BICK = 64× IWR is recommended to minimize the possibility of performance degradation resulting from BICK coupling on the supply voltages.

Reset

$\overline{\text{RST}}$ is an active low signal that resets the digital filter and delta-sigma modulator and synchronizes LRCK with internal control signals. The CS4303 DOL+\- and DOR+\- outputs are forced to zero during reset.

Power-Up Considerations

Upon initial application of power to the DAC, the digital filter registers will be indeterminate. $\overline{\text{RST}}$ should be low during power-up to prevent this erroneous information from being output from the DAC. Bringing $\overline{\text{RST}}$ high will initialize these registers.

Muting

The Mute functions of the CS4303 involve the recognition of 0 input data for 4096 consecutive LRCK cycles. If the MUTE pin is HIGH, the DATA outputs will be forced to 0 following 4096 LRCK cycles with 0 input data. If left LOW, the MUTE circuit will ignore 0 input data. The DZF, Data Zero Flag, pin will go HIGH following 0 input data for 4096 consecutive LRCK cycles regardless of the Mute pin status. The DZF output can be used to control an external muting circuit.

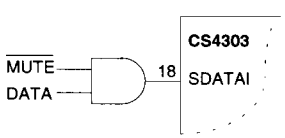


Figure 12. Muting Implementation

A two stage MUTE operation can be implemented by forcing SDATAI to 0 using an AND gate as shown in Figure 12. The first mute occurs following 33 LRCK cycles when the 0 input data propagates to the output of the DAC. Following a total of 4096 LRCK cycles with 0 input data the output of the CS4303 will mute. Upon release of the MUTE command and non-zero input data, the CS4303 output mute will immediately release. However, 33 LRCK cycles are required for input data to propagate to the output.

Analog Output and Filtering

The primary function of the analog filter is to attenuate the noise generated by the delta-sigma modulator beyond the audio passband. The selection of the filter transfer function is based on the optimization of out-of-band noise attenuation, passband amplitude and phase requirements. The computer simulated frequency spectrum of the 1-bit delta-sigma modulator output is shown in Figure 5 for an Fs of 48 kHz. Figures 13-15 show the results of computer simulations demonstrating the attenuation of out-of-band noise with 3, 5 and 7 pole Butterworth filters. The filter corner frequencies were selected to achieve a maximum attenuation of 0.2 dB at 20kHz.

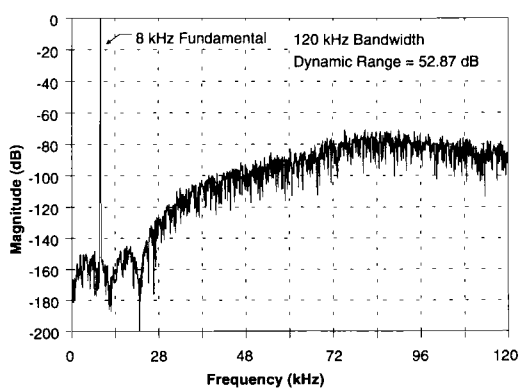


Figure 13. Simulated Noise Attenuation 3rd Order Filter

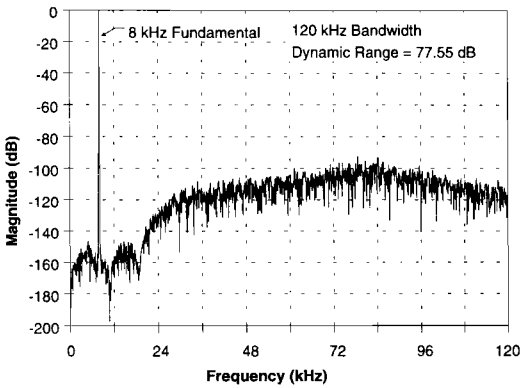


Figure 14. Simulated Noise Attenuation Fifth Order Filter

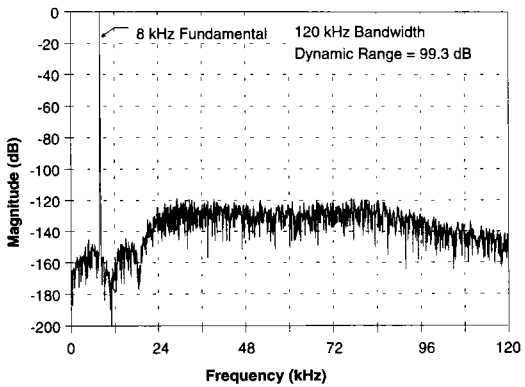


Figure 15. Simulated Noise Attenuation Seventh Order Filter

The suggested filter of Figures 16-19 is a 5-pole Butterworth modified to realize a 6-pole response. Implementing a pole as a passive RC in the input of the analog circuit along with a high slew rate op-amp will eliminate slew rate related distortion. This architecture provides matched loading for the differential outputs and a noise-free pole for additional out-of-band noise attenuation.

Measuring System Performance

The effects of out-of-band noise must be considered when making THD+N and dynamic range measurements. The dynamic range specifications of Figures 13-15 are identical over a 20kHz bandwidth but differ by 46 dB over the 120kHz bandwidth. The proper use of a measurement bandlimiting filter is critical for evaluating the in-band performance of systems with low-order analog filters. The measurement bandwidth must be properly limited to prevent out-of-band energy from dominating the measurements.

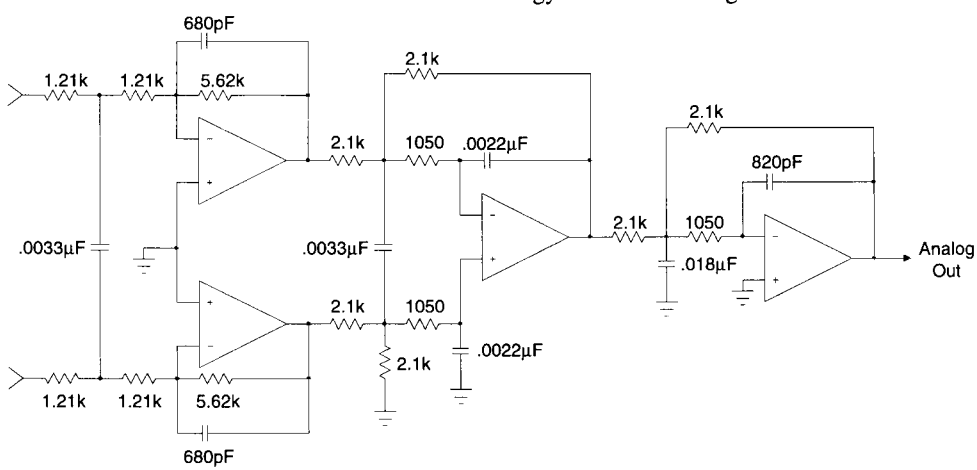


Figure 16. Suggested 6-Pole Analog Filter

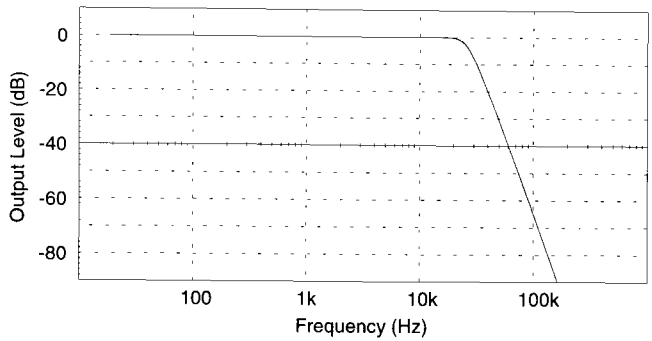


Figure 17. Simulated Analog Filter Frequency Response

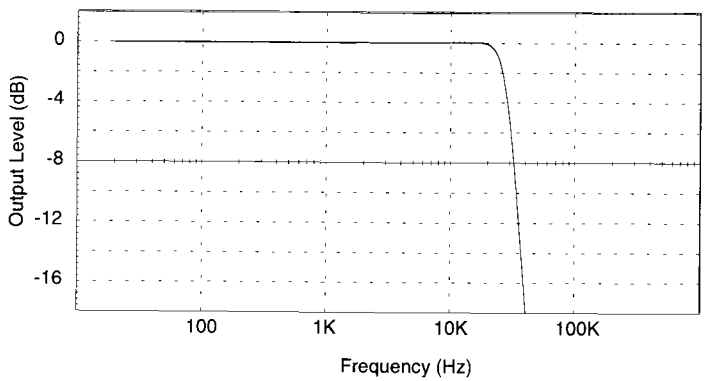


Figure 18. Simulated Analog Filter Frequency Response Expanded Scale

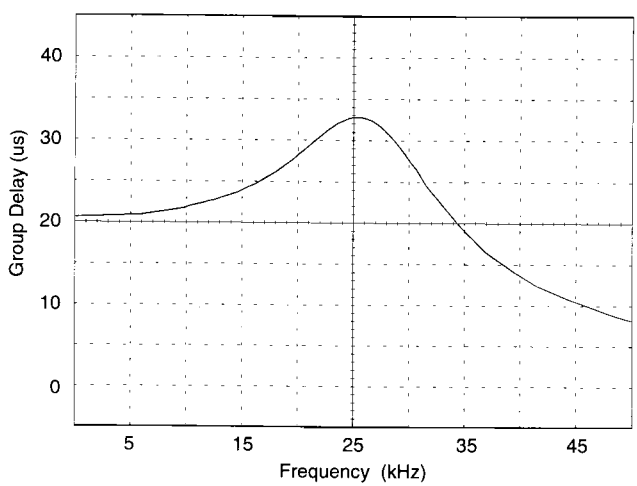


Figure 19. Simulated Analog Filter Group Delay

System Performance Measurements

The following collection of CS4303 measurement plots (IWR = 48 kHz) were taken from a CDB4303 evaluation board with an Audio Precision Dual Domain System One. All FFT plots are 16,384 point. Several of the plots are influenced by inadequate dithering of the test signal.

Figure 20 shows the **unmuted noise**. This data was taken by feeding the CS4303 all zero's. This plot shows the noise shaping characteristics of the delta-sigma modulator combined with the analog filter.

Figure 21 shows the A-weighted **THD+N vs signal amplitude** for a dithered 1kHz input signal. The small variations in THD + N at around -70 dB are caused by inadequate dithering of the test signal. The System One was set to 18-bit triangular dither.

Figures 22 and 23 show the **fade-to-noise linearity**. The input test signal is a dithered 500 Hz sine wave which gradually fades from -60 dB level to -120 dB. During the fading, the output level from the CS4303 is measured and compared to the ideal level. Notice the very close tracking of the output level to the ideal, even at low level inputs of -90 dB. The gradual shift of the plot away from zero at signal levels < -100 dB is caused by the background noise starting to dominate the measurement. Figure 22 shows the result with 18-bit dithered data. The 1 dB shift at -95 dB is due to inadequate dither. Figure 23 shows the result with 16-bit dithered data.

Figure 24 shows a 16K **FFT plot result, with a 1 kHz -100 dB 17-bit dithered input**. Notice the lack of distortion components.

Figure 25 shows the **monotonicity test** result plot. The input data to the CS4303 is +1 LSB, -1 LSB four times, then +2 LSB, -2 LSB four times and so on, until +10 LSB, -10 LSB. This data pattern is taken from track 21 of the CD-1 test disk. Notice the increasing staircase envelope, with no decreasing elements. Notice also the clear resolution of the LSB. For this test, one LSB is a 16-bit LSB.

The following tests were done by filtering the analog output of the CS4303 with the System One analyzer 1 kHz notch filter to reduce the peak signal level. The resulting signal was then amplified and applied to the DSP module, avoiding distortion in the System One A/D converter.

Figure 26 shows a **16K FFT Plot with a 1 kHz, 0 dB** input. Notice the low order harmonic distortion at < -100 dB.

Figure 27 shows a **16K FFT Plot with a 1 kHz, -10 dB** input. Notice the almost complete absence of distortion, with a small residual 2nd harmonic below -120 dB.

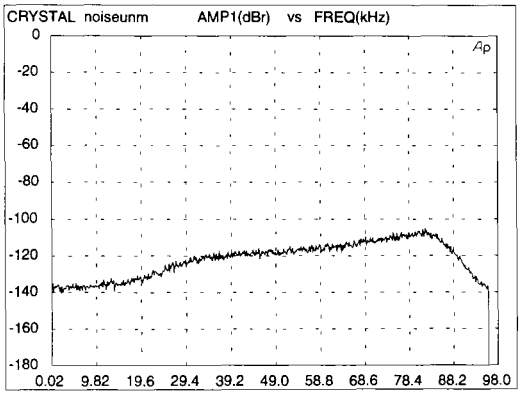


Figure 20. Unmuted Noise

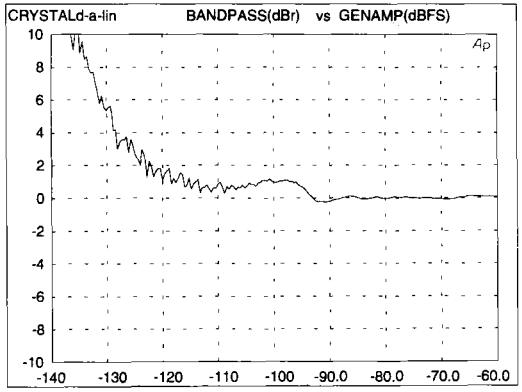


Figure 22. Fade to Noise Dithered 18-bit Linearity

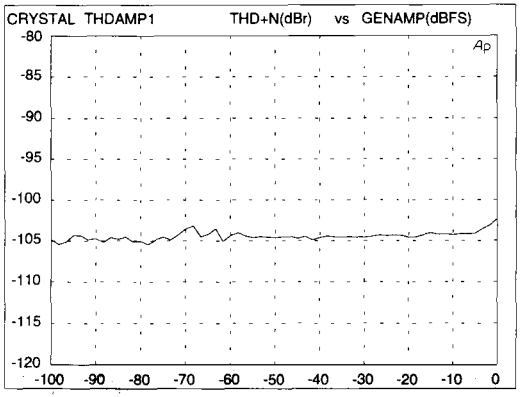


Figure 21. 1 kHz A-weighted THD + N vs Level

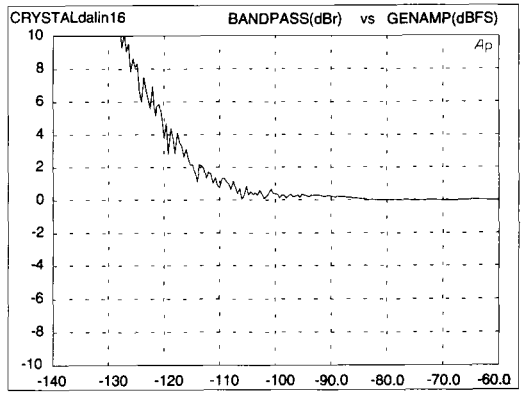


Figure 23. Fade to Noise Dithered 16-bit Linearity

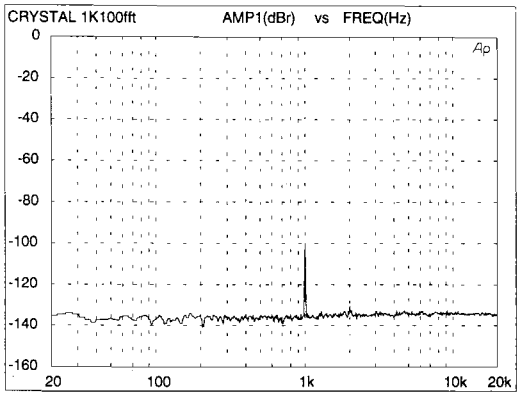


Figure 24. 1 kHz -100 dB FFT

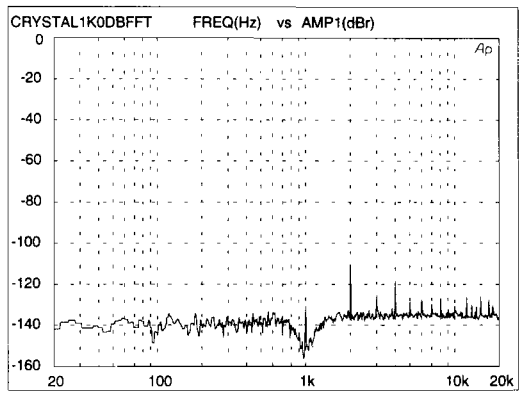


Figure 26. 1kHz 0 dB FFT

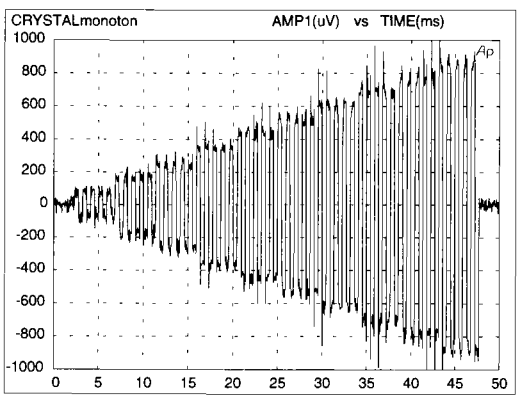


Figure 25. Monotonicity Test (16-bit Data)

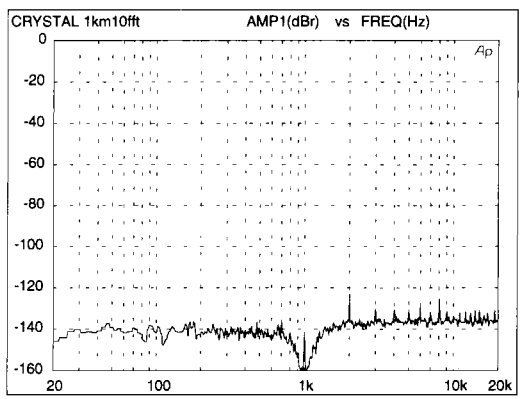
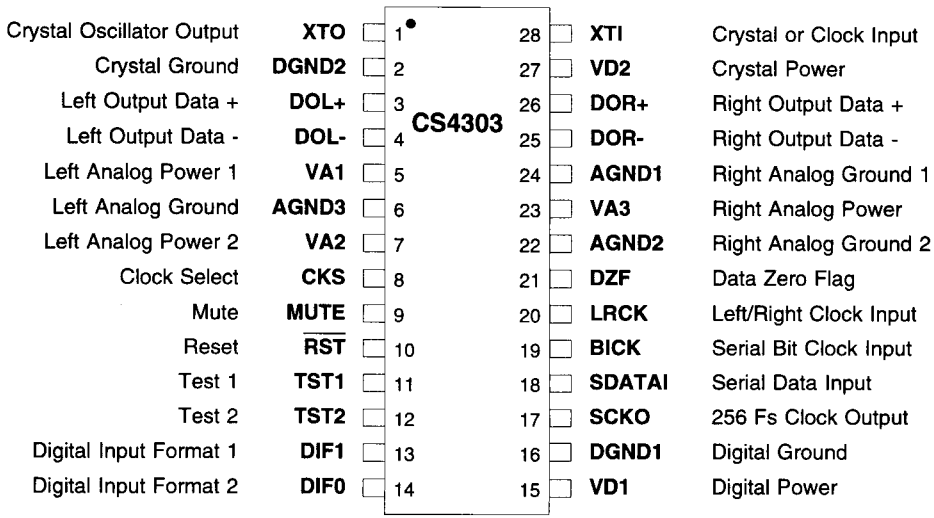


Figure 27. 1 kHz -10 dB FFT

PIN DESCRIPTIONS



Power Supply Connections

VA1, VA2, VA3 - Analog Power, PINS 5, 7, 23.
Positive analog supplies. Nominally +5 volts.

AGND1, AGND2, AGND3 - Analog Grounds, PINS 6, 22, 24.
Analog ground reference.

VD1 - Digital Power, PIN 15.
Positive supply for the digital section. Nominally +5 volts.

DGND1 - Digital Ground, PIN 16.
Ground for the digital section.

VD2 - Crystal Power, PIN 27.
Positive supply for the crystal oscillator. Nominally +5 volts.

DGND2 - Crystal Ground, PIN 2.
Crystal ground reference.

Digital Inputs

XTI - Crystal or Clock Input, PIN 28.

A crystal oscillator can be connected between this pin and XTO, or an external CMOS clock can be input on XTI. The frequency must be either 256× or 384× the input word rate based on the clock select pin, CKS.

MUTE - Mute Input, PIN 9.

This input determines if the CS4303 will recognize an input string of 4096 zeros to initiate a muted output. If left low, the CS4303 will not mute.

DZF - Data Zero Flag, PIN 21.

This pin will go High following 0 input data for 4096 consecutive LRCK cycles regardless of the Mute pin status.

SCKO - Serial Clock Output, PIN 17

Clock output of 256× the input word rate regardless of the CKS pin status.

LRCK - Left/Right Clock, PIN 20.

This input determines which channel is currently active on the Serial Data Input pin, SDATAI. The format of LRCK is controlled by DIF0 and DIF1.

BICK - Serial Bit Input Clock, PIN 19.

Clocks the individual bits of the serial data in from the SDATAI pin. The polarity with respect to the serial data is controlled by DIF0 and DIF1.

SDATAI - Serial Input, PIN 18.

Two's complement MSB-first serial data of either 16 or 18 bits is input on this pin. The data is clocked into the CS4303 via the BICK clock and the channel is determined by the LRCK clock. The format for the previous two clocks is determined by the Digital Input Format pins, DIF0 and DIF1.

DIF0, DIF1 - Digital Input Format, PINS 14, 13.

These two pins select one of four formats for the incoming serial data stream. These pins set the format of the BICK and LRCK clocks with respect to SDATAI. The formats are listed in Table 2.

CKS - Clock Speed Select, PIN 8.

Selects the clock frequency input on the XTI pin. CKS low selects 256× the input word rate (LRCK frequency) while CKS high selects 384×.

$\overline{\text{RST}}$ - Reset, PIN 10.

When reset is low, the filters and modulators are held in reset.

TST1, TST2 - Test Inputs, PINS 11, 12.

Allows access to the CS4303 test modes, which are reserved for factory use. Must be tied to DGND.

Digital Outputs

XTO - Crystal Oscillator Output, PIN 1.

When a crystal oscillator is used, it is tied between this pin and XTI. When an external clock is input, this pin should be left floating.

DOL+, DOL- - Digital Left Channel Output, PINS 3, 4.

Differential digital output data for the left channel.

DOR+, DOR- - Digital Right Channel Output, PINS 26, 25.

Differential digital output data for the right channel.