HARRIS

HA-5330/883

Very High Speed Precision Monolithic Sample and Hold Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragragh 1.2.1
- Maximum Acquisition (10V Step to 0.1%) 500ns
  (10V Step to 0.01%) 900ns
- TTL Compatible Control Input
- Power Supply Rejection .....≥86dB
- Low Droop Rate (Max at +125°C) 100μV/μs
- Wide Supply Range .....±11V to ±18V
- Internal Hold Capacitor
- Low Output Resistance

Applications

- Precision Data Acquisition Systems
- D/A Converter Deglitching
- Auto-Zero Circuits
- Peak Detectors

Description

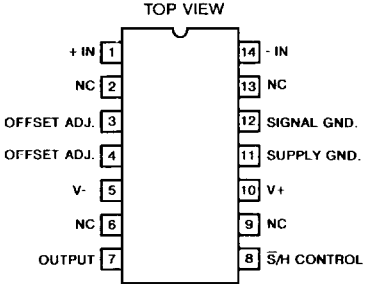
The HA-5330/883 is a very fast sample and hold amplifier designed primarily for use with high speed A/D converters. It utilizes the Harris Dielectric Isolation process to achieve a 900ns acquisition time to 12-bit accuracy and a droop rate of 100μV/μs at +125°C. The circuit consists of an input transconductance amplifier capable of producing large amounts of charging current, a low leakage analog switch, and an integrating output stage which includes a 90pF hold capacitor.

The analog switch operates into a virtual ground, so charge injection on the hold capacitor is constant and independent of V_{IN}. Charge injection is held to a low value by compensation circuits and, if necessary, the resulting 0.5mV (TYP) hold step error can be adjusted to zero via the Offset Adjust terminals. Compensation is also used to minimize leakage currents which cause voltage droop in the Hold mode.

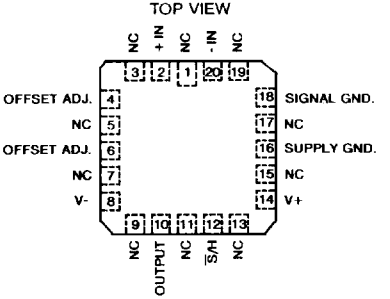
The HA-5330/883 will operate at reduced supply voltages (to ±11V) with a reduced signal range. This monolithic device is available in a Ceramic 14-pin DIP, and a 20 pad Ceramic LCC package.

Pinouts

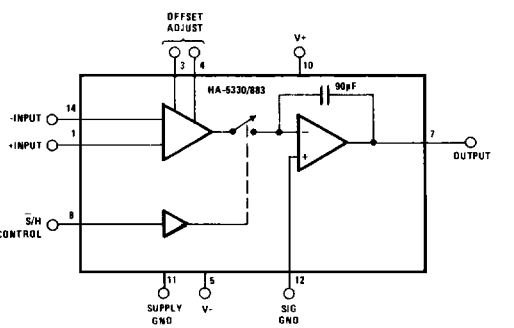
HA1-5330/883 (CERAMIC DIP)
TOP VIEW



HA4-5330/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



NOTE: Pin Numbers Correspond to DIP Package Only.

Absolute Maximum Ratings

Voltage Between V+ and Supply/Signal GND ..... +20V
Voltage Between V- and Supply/Signal GND ..... -20V
Voltage Between Supply GND and Signal GND ..... ±2.0V
Differential Input Voltage ..... ±24V
Digital Input Voltage ($\overline{S}$/H Pin) ..... +8V, -6V
Output Current (Note 1) 17mA
Storage Temperature Range ..... $-65^oC < T_A < +150^oC$
Lead Temperature (Soldering 10 Seconds) ..... $+275^oC$
Junction Temperature ..... $+175^oC$
ESD Classification ..... < 2000V

NOTE: 1. Internal power dissipation may limit output current below ±17mA.

Thermal Information

Thermal Resistance, Junction-to-Ambient (θ_{jC})
Ceramic DIP Package ..... $15^oC/W$
Ceramic LCC Package ..... $19^oC/W$
Thermal Resistance, Junction-to-Ambient (θ_{jA})
Ceramic DIP Package ..... $75^oC/W$
Ceramic LCC Package ..... $76^oC/W$
Power Dissipation (at $+75^oC$)
Ceramic DIP Package 1.33W
Ceramic LCC Package 1.32W
Power Dissipation Derating Factor (Above $+75^oC$)
Ceramic DIP Package ..... 13.3W mW/^oC
Ceramic LCC Package ..... 13.2W mW/^oC

Recommended Operating Conditions

Operating Temperature Range ..... $-55^oC < T_A < +125^oC$
Operating Supply Voltage (V_{SUPPLY}) ..... ±15V
Analog Input Voltage (V_S) ..... ±10V
Logic Level Low (V_{IL}) ..... 0V to 0.8V
Logic Level High (V_{IH}) ..... 2.0V to 5.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at V+ = +15V; V- = -15V; V_{IL} = 0.8V (Sample); V_{IH} = 2.0V (Hold); C_H = Internal = 90pF, -Input Tied to Output, SIG. GND = SUPPLY GND; Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}		1	+25°C	-2	2	mV
			2, 3	+125°C, -55°C	-2	2	mV
Input Bias Current	I_{B+}		1	+25°C	-500	500	nA
			2, 3	+125°C, -55°C	-500	500	nA
	I_{B-}		1	+25°C	-500	500	nA
			2, 3	+125°C, -55°C	-500	500	nA
Input Offset Current	I_{IO}		1	+25°C	-500	500	nA
			2, 3	+125°C, -55°C	-500	500	nA
Open Loop Voltage Gain	$+A_{VOL}$	R_L = 1kΩ, V_{OUT} = +10V	1	+25°C	2×10^6	-	V/V
			2, 3	+125°C, -55°C	2×10^6	-	V/V
	$-A_{VOL}$	R_L = 1kΩ, V_{OUT} = -10V	1	+25°C	2×10^6	-	V/V
			2, 3	+125°C, -55°C	2×10^6	-	V/V
Common Mode Rejection Ratio	-CMRR	V+ = 25V, V- = -5V, V_{OUT} = 10V, $V_{\overline{S}/H}$ = 10.8V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB
	+CMRR	V+ = 5V, V- = -25V, V_{OUT} = -10V, $V_{\overline{S}/H}$ = -9.2V	1	+25°C	86	-	dB
			2, 3	+125°C, -55°C	86	-	dB
Output Current	$+I_O$	V_{OUT} = +10V	1	+25°C	10	-	mA
			2, 3	+125°C, -55°C	10	-	mA
	$-I_O$	V_{OUT} = -10V	1	+25°C	-	-10	mA
			2, 3	+125°C, -55°C	-	-10	mA
Output Voltage Swing	$+V_{OUT}$	R_L = 1kΩ	1	+25°C	+10.0	-	V
			2, 3	+125°C, -55°C	+10.0	-	V
	$-V_{OUT}$	R_L = 1kΩ	1	+25°C	-	-10.0	V
			2, 3	+125°C, -55°C	-	-10.0	V
Power Supply Current	$+I_{CC}$		1	+25°C	-	22	mA
			2, 3	+125°C, -55°C	-	22	mA
	$-I_{CC}$		1	+25°C	-23	-	mA
			2, 3	+125°C, -55°C	-23	-	mA
Power Supply Rejection Ratio	+PSRR	V+ = +13.5V, +16.5V, V- = -15V, -15V	1	+25°C	86	-	dB
			2, 3	-55°C, +125°C	86	-	dB
	-PSRR	V+ = +15V, +15V, V- = -13.5V, -16.5V	1	+25°C	86	-	dB
			2, 3	-55°C, +125°C	86	-	dB
Digital Input Current	I_{IN1}	V_{IN1} = 0V	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	40	µA
	I_{IN2}	V_{IN2} = 5.0V	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	40	µA
Digital Input Voltage	V_{IL}		1	+25°C	-	0.8	V
			2, 3	+125°C, -55°C	-	0.8	V
	V_{IH}		1	+25°C	2.0	-	V
			2, 3	+125°C, -55°C	2.0	-	V
Output Voltage Droop Rate	V_D		2	+125°C	-100	100	µV/µs

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at V+ = +15V, V- = -15V, V_{IL} = 0.8V (Sample), V_{IH} = 2.0V (Hold), C_H = Internal = 90pF, SIG. GND. = SUPPLY GND., -Input Tied to Output, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Acquisition Time 0.1%	$+t_{acq}$ (0.1%)	$R_L = 2k\Omega$, $C_L = 50pF$, $A_V = +1$ $V_{OUT} = 0V, +10V$	2	+25°C	-	500	ns
				+125°C, -55°C	-	500	ns
	$-t_{acq}$ (0.1%)	$R_L = 2k\Omega$, $C_L = 50pF$, $A_V = +1$ $V_{OUT} = 0V, -10V$	2	+25°C	-	500	ns
				+125°C, -55°C	-	500	ns
Acquisition Time 0.01%	$+t_{acq}$ (0.01%)	$R_L = 2k\Omega$, $C_L = 50pF$, $A_V = +1$ $V_{OUT} = 0V, +10V$	2	+25°C	-	900	ns
				+125°C, -55°C	-	900	ns
	$-t_{acq}$ (0.01%)	$R_L = 2k\Omega$, $C_L = 50pF$, $A_V = +1$ $V_{OUT} = 0V, -10V$	2	+25°C	-	900	ns
				+125°C, -55°C	-	900	ns
Output Voltage Droop Rate	V_D		2	+25°C, -55°C	-10	10	µV/µs

NOTE: 2. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Test Circuit

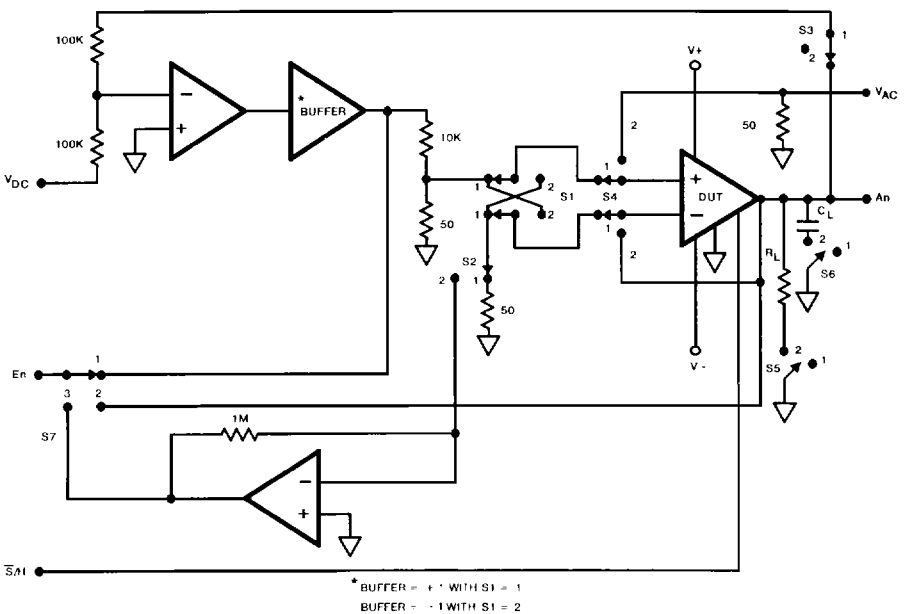


CHART A. TEST CIRCUIT CONDITIONS (SEE TEST CIRCUIT)

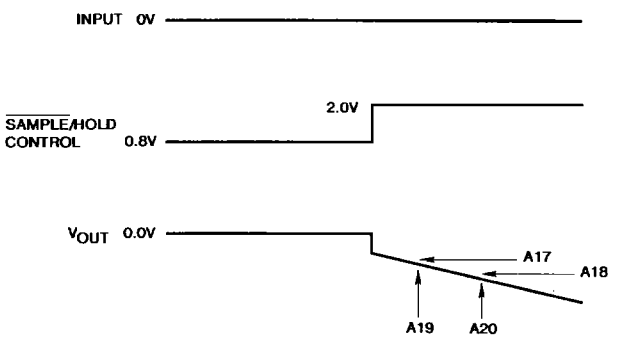
PARAMETERS	NOTE	APPLY (IN VOLTS) OR MEASURE (m)						SWITCH POSITION							MEASURE		MEASURED PARAMETER OR EQUATION	UNITS
		V+	V-	VDC	$\overline{S}$/H	En	An	S1	S2	S3	S4	S5	S6	S7	VALUE	UNIT		
V_{IO}	-	+15	-15	0.0	0.8	m	-	1	1	1	1	1	1	1	E1	V	$V_{IO} = -E1/200$	mV
I_{IO}	-	+15	-15	0.0	0.8	-	-	-	-	-	-	-	-	-	-	V	$I_{IO} = (I_{B+})-(I_{B-})$	nA
I_{B+}	-	+15	-15	0.0	0.8	m	-	2	2	1	1	1	1	3	E7	V	$I_{B+} = (E1-E7)/10^6$	nA
I_{B-}	-	+15	-15	0.0	0.8	m	-	1	2	1	1	1	1	3	E10	V	$I_{B-} = (E1-E10)/10^6$	nA
$+I_{CC}$	-	+15	-15	0.0	0.8	-	-	1	1	1	1	1	1	1	-	mA	Measure $+V_{CC}$ Current	mA
$-I_{CC}$	-	+15	-15	0.0	0.8	-	-	1	1	1	1	1	1	1	-	mA	Measure $-V_{CC}$ Current	mA
-PSRR	- -	+15 +15	-13.5 -16.5	0.0 0.0	0.8 0.8	m m	-	1	1	1	1	1	1	1	E13 E14	V V	$-PSSR = 20Log_{10} \left\lvert \frac{3V}{(E13-E14)/200} \right\rvert$	dB
+PSRR	- -	+13.5 +16.5	-15 -15	0.0 0.0	0.8 0.8	m m	-	1	1	1	1	1	1	1	E15 E16	V V	$+PSRR = 20Log_{10} \left\lvert \frac{3V}{(E15-E16)/200} \right\rvert$	dB
+CMRR	3	+5	-25	+10	-9.2	m	-	1	1	1	1	1	1	1	E17	V	$+CMRR = 20Log_{10} \left\lvert \frac{10V}{(E1-E17)/200} \right\rvert$	dB
-CMRR	4	+25	-5	-10	+10.8	m	-	1	1	1	1	1	1	1	E18	V	$-CMRR = 20Log_{10} \left\lvert \frac{10V}{(E1-E18)/200} \right\rvert$	dB
I_{IN1}	-	+15	-15	0.0	0.0	-	-	1	1	1	1	1	1	1	-	µA	Measure $\overline{S}$/H Current	µA
I_{IN2}	-	+15	-15	0.0	5.0	-	-	1	1	1	1	1	1	1	-	µA	Measure $\overline{S}$/H Current	µA
Droop Rate	-	+15	-15	0.0	2.0	-	m m	1	1	2	2	2	1	2	A17, A19 A18, A20	V, ms V, ms	Droop Rate $= \frac{A18-A17}{A20-A19}$, A20-A19 = 10ms	µA/µs
$-I_O$	-	+15	-15	-13	0.8	-10mA	-	1	1	1	1	1	1	2	-	V	Measure En Volts	V
$+I_O$	-	+15	-15	+13	0.8	+10mA	-	1	1	1	1	1	1	2	-	V	Measure En Volts	V
$+V_{OUT}$	5	+15	-15	-14	0.8	m	-	1	1	1	1	2	1	2	E23	V		V
$-V_{OUT}$	5	+15	-15	+14	0.8	m	-	1	1	1	1	2	1	2	E24	V		V
$+A_{VOL}$	5 -	+15 +15	-15 -15	0.0 -10	0.8 0.8	m m	- -	1 1	1 1	1 1	1 1	2 2	1 1	1 1	E25 E26	V V	$+A_{VOL} = 20Log_{10} \left\lvert \frac{10V}{(E25-E26)/200} \right\rvert$	dB
$-A_{VOL}$	5 -	+15 +15	-15 -15	0.0 +10	0.8 0.8	m m	- -	1 1	1 1	1 1	1 1	2 2	1 1	1 1	E27 E28	V V	$-A_{VOL} = 20Log_{10} \left\lvert \frac{10V}{(E27-E28)/200} \right\rvert$	dB

NOTES:

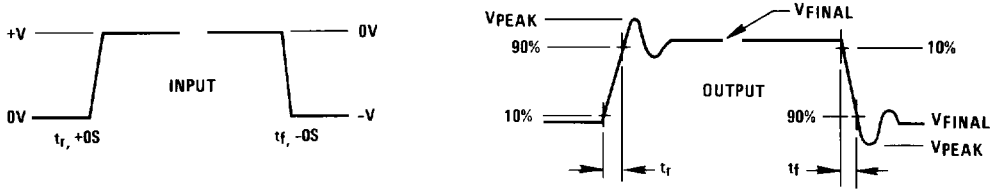
3. Package GND to -10V for this test.
4. Package GND to +10V for this test.
5. R_{LDC} = 1kΩ.

Timing Waveforms

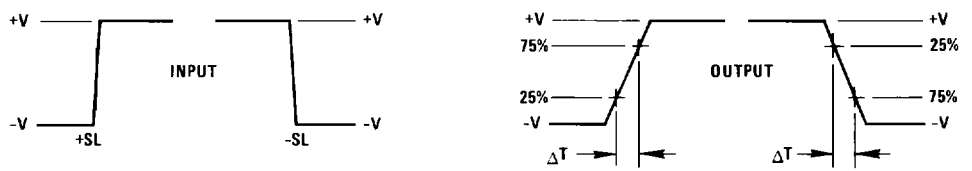
DROOP RATE WAVEFORMS



OVERSHOOT, RISE & FALL TIME WAVEFORMS

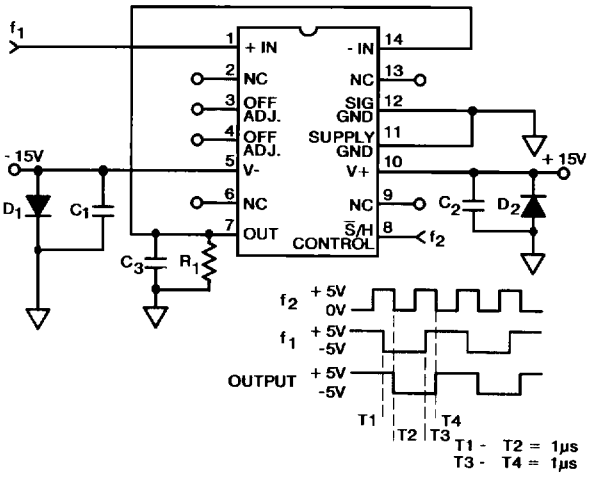


SLEW RATE WAVEFORMS

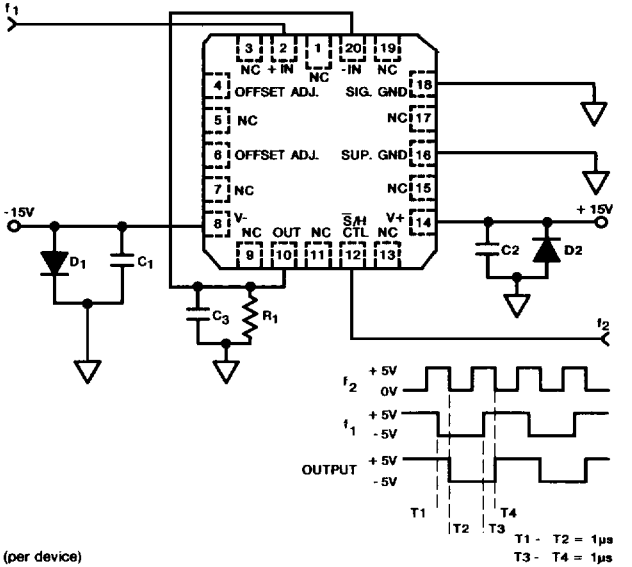


Burn-In Circuits

HA-5330/883 (CERAMIC DIP)



HA-5330/883 (CERAMIC LCC)



NOTES:
R_1 = 510Ω, 5%, 1/2 Watt (per device)
C_1 = C_2 =0.1µF (per device)
C_3 = 47pF, 10%, 50V (per device)
D_1 = D_2 = 1N4002 or Equivalent (per board)
f_2 = 250kHz, TTL Levels, 50% Duty Cycle
f_1 = 125kHz, +5V to -5V, 50% Duty Cycle

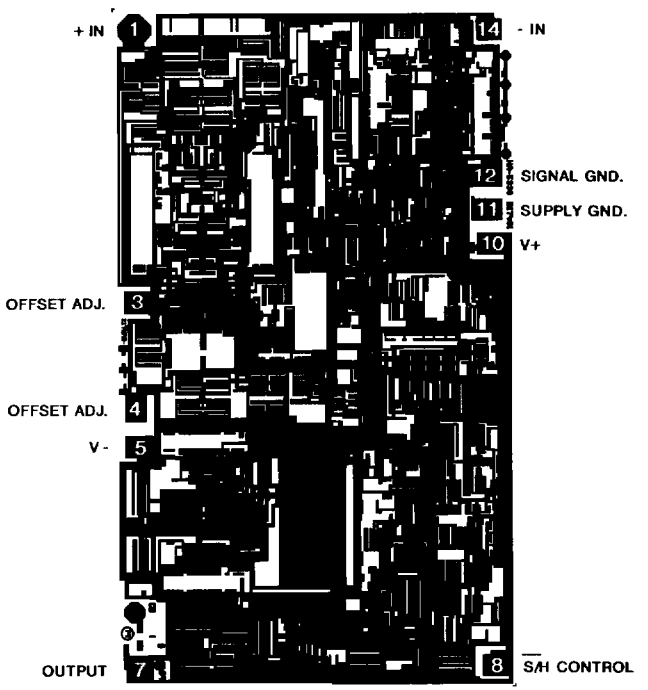
Die Characteristics

DIE DIMENSIONS: 99 x 166 x 19 mils
METALLIZATION:
Type: Al
Thickness: 16kÅ ± 2kÅ
GLASSIVATION:
Type: Silox
Thickness: 14kÅ ± 2.0kÅ
WORST CASE CURRENT DENSITY: 1.36 x 10^5A/cm^2

TRANSISTOR COUNT:
HA-5330/883 205
PROCESS: Bipolar DI
DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460°C (Max)
Ceramic LCC - 420°C (Max)

Metallization Mask Layout

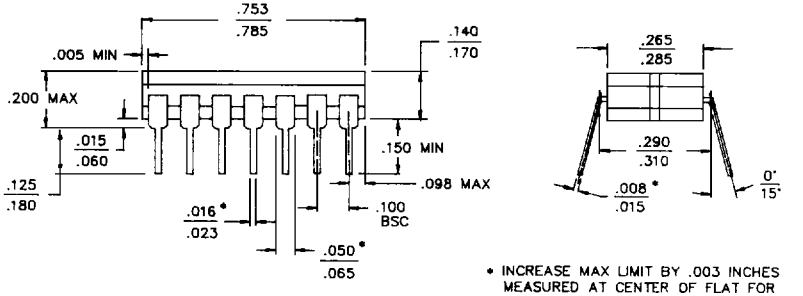
HA-5330/883



NOTE: Pad Numbers Correspond to DIP Package Only.

Packaging†

14 PIN CERAMIC DIP

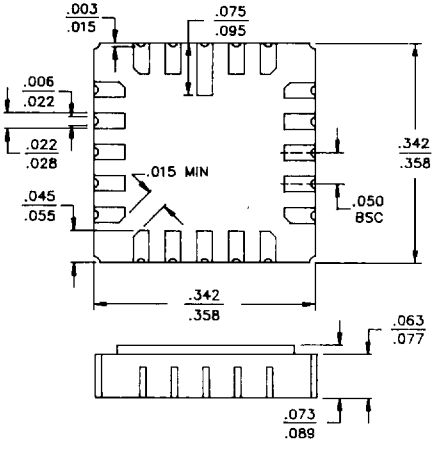


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ±10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ±10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$ Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

DESIGN INFORMATION

Very High Speed Precision Monolithic Sample and Hold Amplifier

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Applying the HA-5330

The HA-5330 has the uncommitted differential inputs of an op amp, allowing the Sample/Hold function to be combined with many conventional op amp circuits. See the Harris Application Note 517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01 to 0.1μF, ceramic) should be provided from each power supply terminal to the Supply Gnd terminal on pin 11.

Applications

The HA-5330 is configured as a unity gain noninverting amplifier by simply connecting the output (pin 7) to the inverting input (pin 14). As an input device for a fast, successive-appoximation A/D converter, it offers an extremely high throughput rate. Also, the HA-5330's pedestal error is adjustable to zero by using an Offset Adjust potentiometer (10K to 50K) center tapped to V-.

The ideal ground connections are pin 12 (Signal Ground) directly to the system Signal Ground (Analog Ground), and pin 11 (Supply Ground) directly to the system Supply Common.

Hold Capacitor

The HA-5330 includes a 90pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Characterisitics section is based on this internal capacitor).

Output Stage

The HA-5330 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the $\overline{S}$/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration. D.C. Output Resistance at +25°C is typically $1 \times 10^{-5}\Omega$ for Sample Mode and 0.2Ω for Hold Mode.

Glossary of Terms

Acquisition Time:

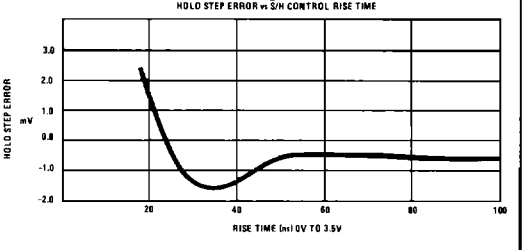
The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Aperture Time:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Hold Step Error:

Hold step error is the output shift due to charge transfer from the sample to the hold mode. It is also referred to as "offset step" or "pedestal error".



Effective Aperture Delay Time (EADT):

The difference between propagation time from the analog input to the $\overline{S}$/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}$/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors will correspond to a value of V_{IN} that occured before the Hold command.

Aperture Uncertainty:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at V+ = +15V, V- = -15V, V_{IL} = 0.8V (Sample), V_{IH} = 2.0V (Hold), C_H = Internal = 90pF, SIG. GND. = Supply GND., -Input Tied to Output; Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYP	UNITS
Hold Step Error	V_{IN} = 0V, V_{IH} = +3.5V t_r = 22ns	+25°C	0.5	mV
Rise Time	V_i =200mV Step R_L = 2kΩ, C_L = 50pF	+25°C	70	ns
Overshoot	V_i =200mV Step R_L = 2kΩ, C_L = 50pF	+25°C	10	%
Slew Rate	V_i =20V Step R_L = 2kΩ, C_L = 50pF	+25°C	90	V/µs
Aperture Time	From Computer Simulation Only	+25°C	20	ns
Effective Aperture Delay Time		+25°C	-25	ns
Aperture Uncertainty		+25°C	0.1	ns
Hold Mode Settling Time (0.01%)		+25°C	100	ns
Hold Mode Feedthrough Attenuation	$20V_{p-p}$, 100kHz	Full	-88	dB
Output Resistance				
Hold Mode	D.C.	+25°C	0.2	Ω
Sample Mode	D.C.	+25°C	10^{-5}	Ω
Input Resistance	From Computer Simulation Only	Full	15×10^6	Ω
Input Capacitance		+25°C	3	pF
Total Output Noise				
Sample	D.C. to 4.0MHz	+25°C	230	μV_{RMS}
Hold	D.C. to 4.0MHz	+25°C	190	μV_{RMS}