

74AC16245 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

D3451, MARCH 1990 – REVISED APRIL 1993

- Member of the Texas Instruments *Widebus™* Family
- Packaged in Shrink Small-Outline 300-mil Package Using 25-mil Center-to-Center Pin Spacings
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Packaged in Plastic Shrink and Plastic Thin Shrink Small-Outline Packages Using 25-mil Center-to-Center Pin Spacings

description

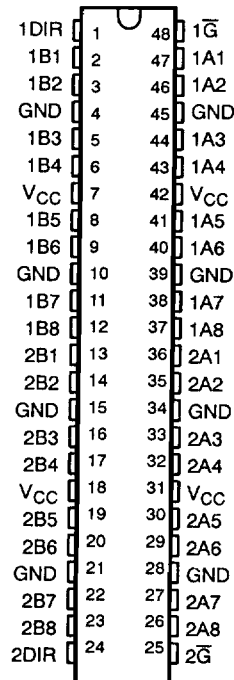
The 74AC16245 is a 16-bit bus transceiver organized as a dual-octal noninverting 3-state transceiver and is designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The enable input (\bar{G}) can be used to disable the devices so that the buses are effectively isolated.

The 74AC16245 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74AC16245 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE

CONTROL INPUTS		OPERATION
\bar{G}	DIR	
L	L	B data to A bus
L	H	A data to bus
H	X	Isolation

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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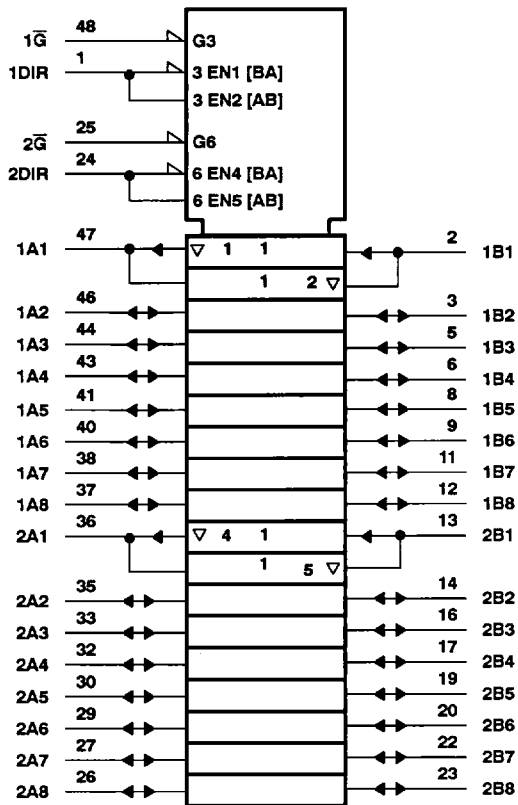
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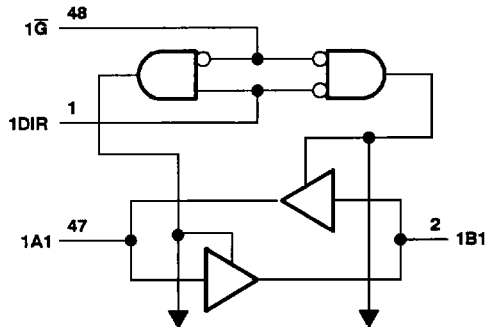
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logic symbol†

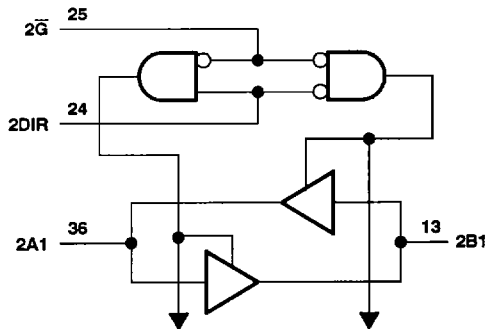


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Transceivers



To Seven Other Transceivers

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	– 0.5 V to 7 V
Input voltage range, V_I (see Note 1)	– 0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	– 0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 400 mA
Storage temperature range	– 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 2)	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 5.5$ V	3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V		0.9	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 5.5$ V		1.65	
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3$ V		–4	mA
		$V_{CC} = 4.5$ V		–24	
		$V_{CC} = 5.5$ V		–24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V		12	mA
		$V_{CC} = 4.5$ V		24	
		$V_{CC} = 5.5$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	–40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage power supply.

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WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
I _{OH} = -75 mA [†]	5.5 V				3.85			
V _{OL}	I _{OL} = 50 μA	3 V	0.1			0.1		V
		4.5 V	0.1			0.1		
		5.5 V	0.1			0.1		
	I _{OL} = 12 mA	3 V	0.36			0.44		
		4.5 V	0.36			0.44		
		5.5 V	0.36			0.44		
I _{OL} = 75 mA [†]	5.5 V				1.65			
I _I	V _I = V _{CC} or GND	5.5 V	±0.1			±1		μA
I _{OZ}	V _I = V _{CC} or GND	5.5 V	±0.5			±5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	8			80		μA
C _I	V _I = V _{CC} or GND	5 V	4.5					pF
C _O	V _I = V _{CC} or GND	5 V	16					

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	2.5	7.6	10.4	2.5	11.9	ns
t _{PHL}			3.1	9	12.3	3.1	13.5	
t _{PZH}	\bar{G}	A or B	2.8	8.6	11.8	2.8	13.2	ns
t _{PZL}			3.9	12	16.2	3.9	18	
t _{PHZ}	\bar{G}	A or B	5.3	8.4	10.4	5.3	11.2	ns
t _{PLZ}			4.4	7.7	9.7	4.4	10.3	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (see Figure 1)

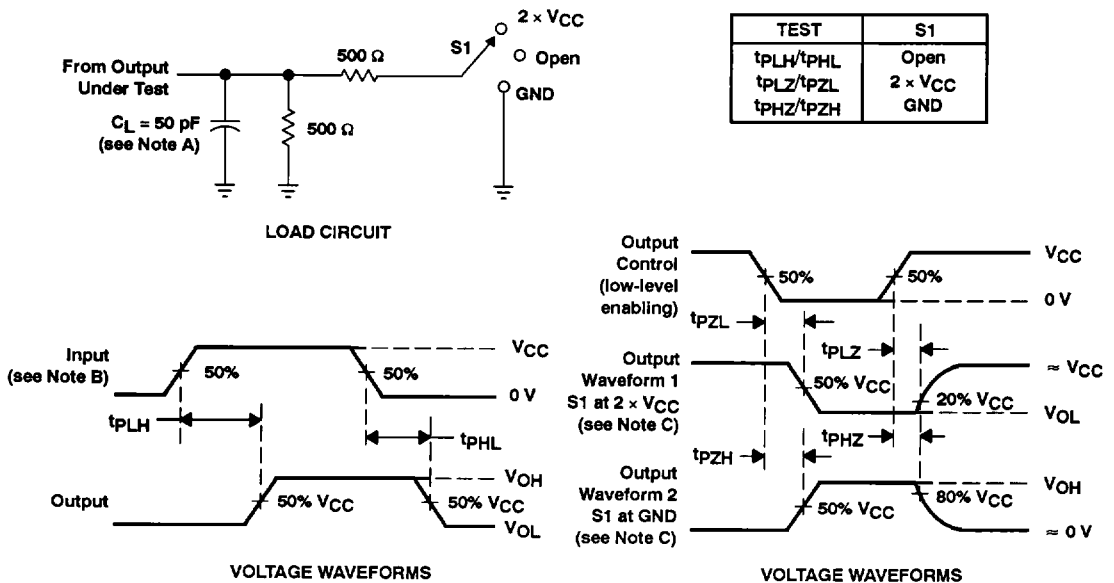
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	2	4.6	6.9	2	7.9	ns
t _{PHL}			2.5	5.2	7.9	2.5	8.9	
t _{PZH}	\bar{G}	A or B	2.3	4.9	7.5	2.3	8.6	ns
t _{PZL}			3	6.2	9.5	3	10.7	
t _{PHZ}	\bar{G}	A or B	5	7.2	9.1	5	9.8	ns
t _{PLZ}			4.2	6.2	8.1	4.2	8.7	



operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	43	pF
			8	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PPR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

