April 1998

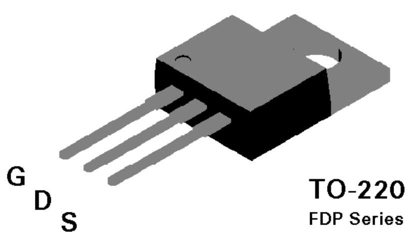
FDP6035L/FDB6035L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

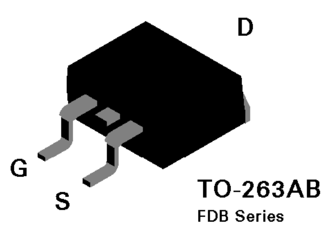
General Description

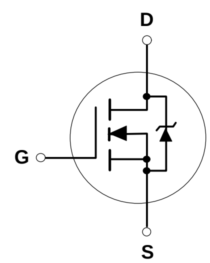
These N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as DC/DC converters and high efficiency switching circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 58 A, 30 V. $R_{DS(ON)} = 0.011\ \Omega$ @ V_{GS}=10 V
  $R_{DS(ON)} = 0.019\ \Omega$ @ V_{GS}=4.5 V.
- Low gate charge (typical 34 nC).
- Low Crss (typical 175 pF).
- Fast switching speed.







Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	FDP6035L	FDB6035L	Units
V_{DSS}	Drain-Source Voltage	30		V
V_{GSS}	Gate-Source Voltage	±20		V
I_D	Drain Current - Continuous	58		A
	- Pulsed	175		
P_D	Maximum Power Dissipation @ T_C = 25°C	75		W
	Derate above 25°C	0.5		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
THERMAL CHARACTERISTICS				
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5		°C/W

Electrical Characteristics T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)							
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 15 V, I_D = 21 A				150	mJ
I_{AR}	Maximum Drain-Source Avalanche Current					21	A
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA		30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C			37		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V				10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V				100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V				-100	nA
ON CHARACTERISTICS (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 250 µA		1	1.6	3	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp.Coefficient	I_D = 250 µA, Referenced to 25 °C			-4		mV/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 26 A			0.0095	0.011	Ω
			T_J =125 °C		0.014	0.019	
		V_{GS} = 4.5 V, I_D = 21 A			0.015	0.019	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V		60			A
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 10 V		15			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 26 A			37		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz			1230		pF
C_{oss}	Output Capacitance				640		pF
C_{rss}	Reverse Transfer Capacitance				175		pF
SWITCHING CHARACTERISTICS (Note 1)							
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 15 V, I_D = 58 A			7.6	15	nS
t_r	Turn - On Rise Time	V_{GS} = 10 V, R_{GEN} = 24 Ω			150	210	nS
$t_{D(off)}$	Turn - Off Delay Time				29	46	nS
t_f	Turn - Off Fall Time				17	27	nS
Q_g	Total Gate Charge	V_{DS}= 12 V, I_D = 58 A, V_{GS}= 10 V			34	46	nC
Q_{gs}	Gate-Source Charge				6		nC
Q_{gd}	Gate-Drain Charge				8		nC
DRAIN-SOURCE DIODE CHARACTERISTICS							
I_S	Maximum Continuous Drain-Source Diode Forward Current					58	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 26 A (Note 1)			0.91	1.3	V
			T_J = 125°C		0.8	1.2	

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

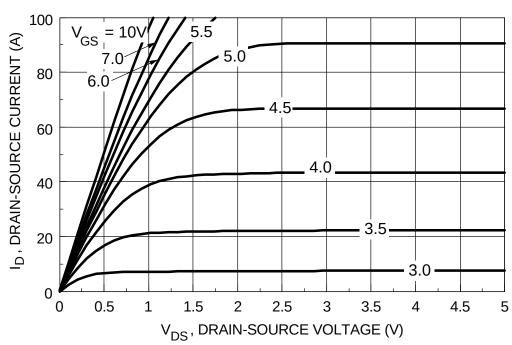


Figure 1. On-Region Characteristics.

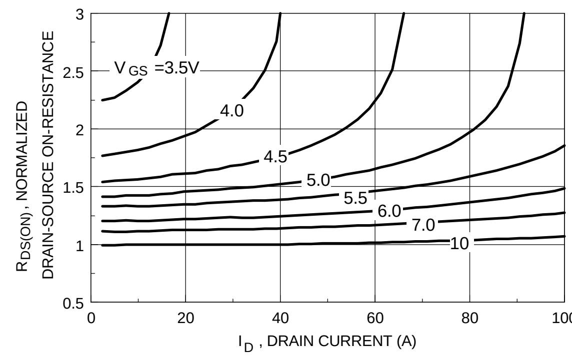


Figure 2. On-Resistance Variation with Drain Current and Gate

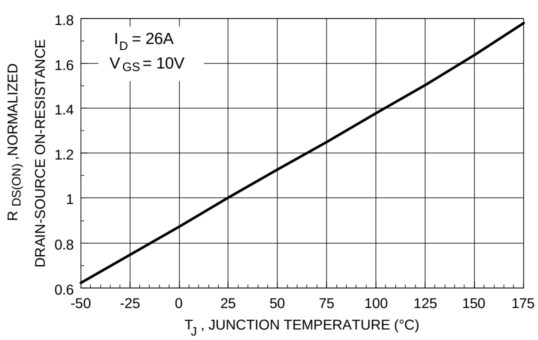


Figure 3. On-Resistance Variation with Temperature.

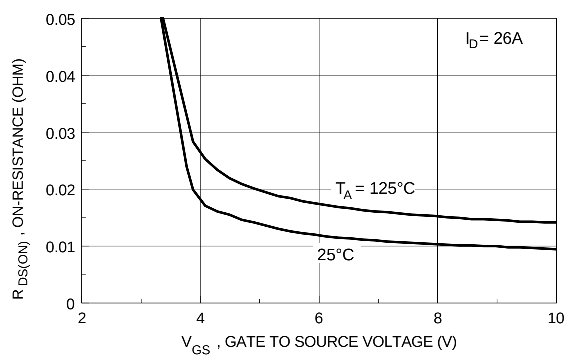


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

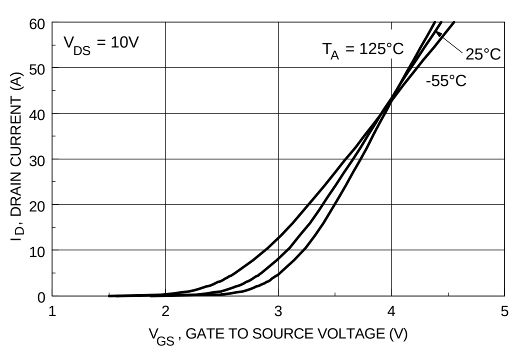


Figure 5. Transfer Characteristics.

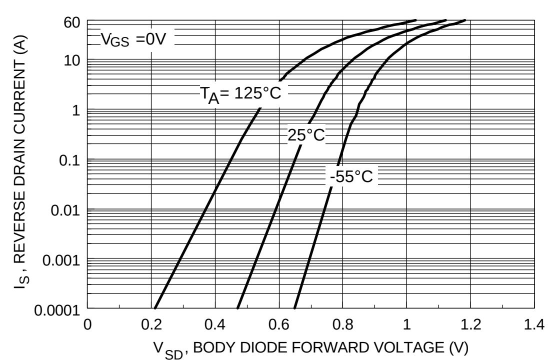


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics (continued)

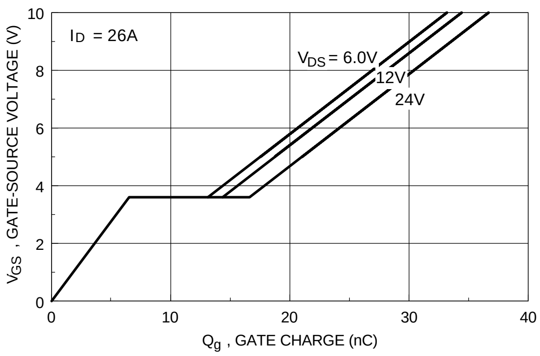


Figure 7. Gate Charge Characteristics.

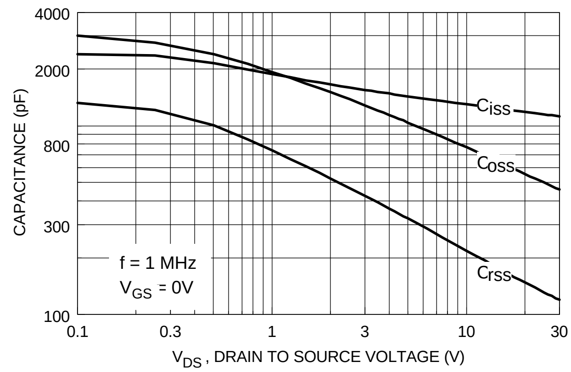


Figure 8. Capacitance Characteristics.

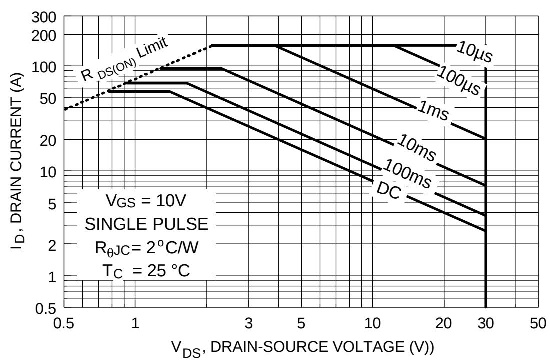


Figure 9. Maximum Safe Operating Area.

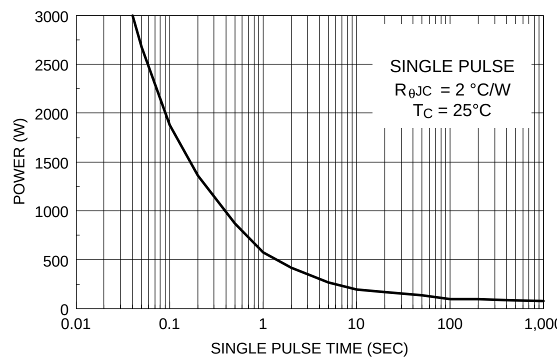


Figure 10. Single Pulse Maximum Power Dissipation.

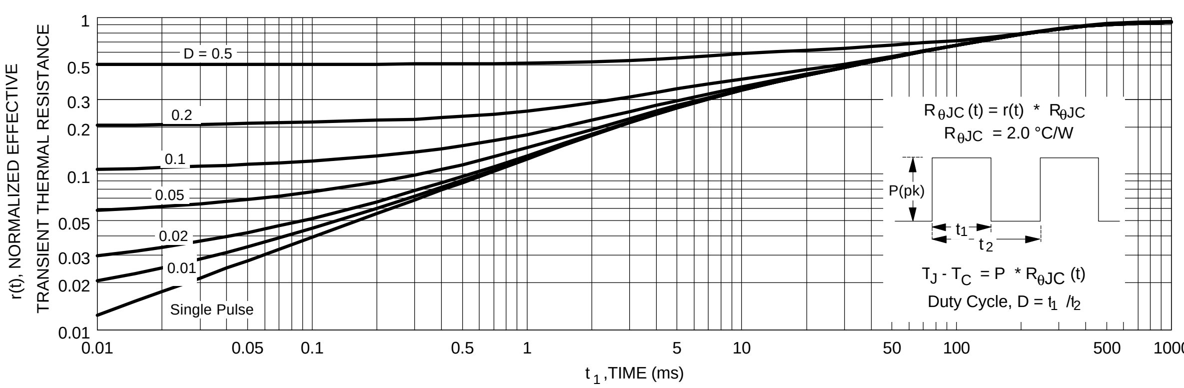


Figure 11. Transient Thermal Response Curve.

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