19-3437; Rev 1; 12/04

EVALUATION KIT AVAILABLE

MAXIM

10.7Gbps, +3.3V, Compact VCSEL Driver

General Description

The MAX3975 is a +3.3V driver designed to directly modulate common-anode vertical cavity surface emitting lasers (VCSELs) at data rates up to 10.7Gbps. The driver output can be connected directly to the VCSEL, requiring no external components for biasing. With a 2.5mm x 2.5mm chip-scale package (UCSP™), transmit disable, output-current monitor, and 0°C to +85°C operation, the MAX3975 is ideal for 850nm XFP/XENPAK transceivers.

The MAX3975 delivers 3mA to 12mA of modulation current, with 1.5mA to 10mA of bias current (peak current 22mA). Typical switching time is 28ps (20% to 80%) with 8ps of deterministic jitter.

Applications

10 Gigabit Ethernet Transceivers

XFP/XENPAK/X2/XPAK Optical Transceivers

SONET VSR Optical Transmitters

10 Gigabit Fibre-Channel Transceivers

Ordering Information

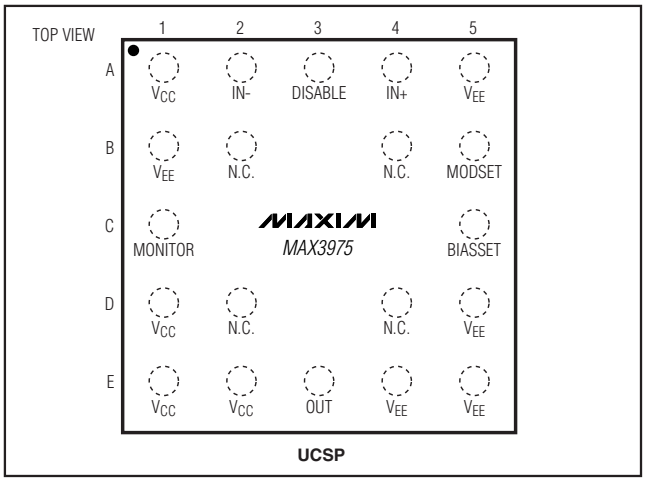
PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3975UBA-T	0°C to +85°C	20 UCSP-20 (2.5mm × 2.5mm)	B25-4

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

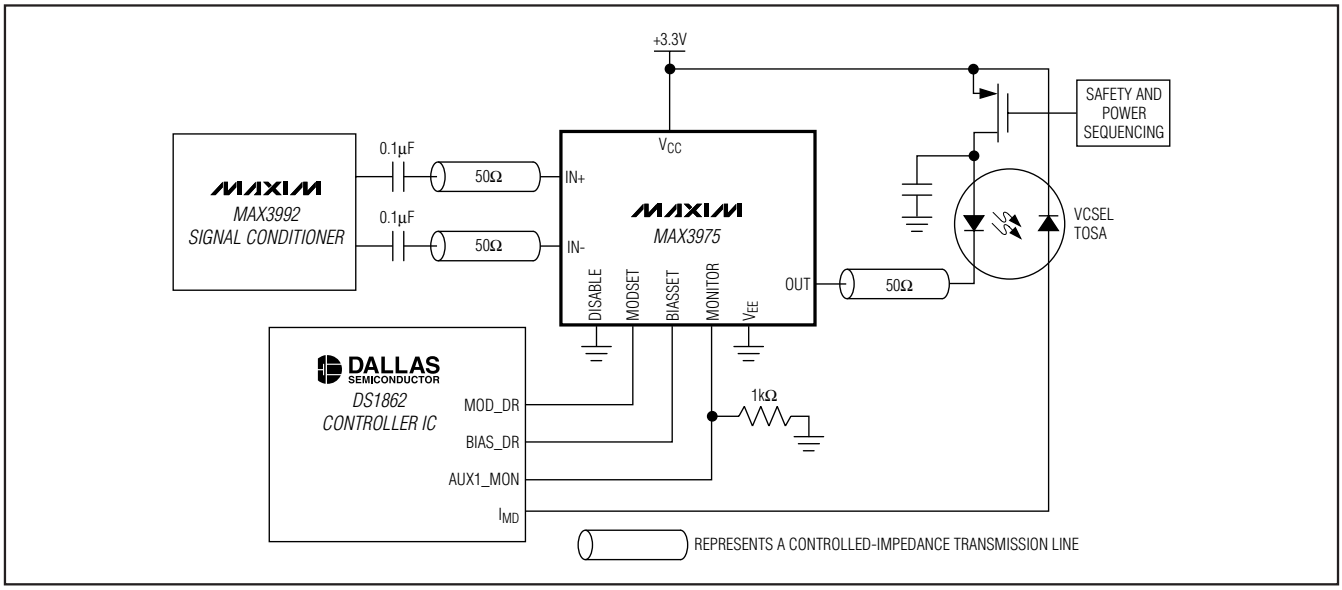
- ♦ **2.5mm x 2.5mm Chip-Scale Package (5 x 5 Array UCSP)**
- ♦ **Single +2.97V to +3.63V Supply Voltage**
- ♦ **28ps Switching Time**
- ♦ **DC-Coupled Output**
- ♦ **3mA to 12mA Modulation Current**
- ♦ **1.5mA to 10mA Bias Current**
- ♦ **Output Disable Circuit**
- ♦ **Output-Current Monitor**

Pin Configuration



UCSP

Typical Application Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

10.7Gbps, +3.3V, Compact VCSEL Driver

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}) .....-0.5V to +4.5V
Voltage at IN+, IN- .....(V_{CC} - 1.75V) to (V_{CC} + 0.5V)
Differential Input Voltage (IN+ - IN-) .....±1.5V
Voltage at DISABLE..... -0.5V to (V_{CC} + 0.5V)
Voltage at MODSET, BIASSET ..... -0.5V to +2.0V
Voltage at MONITOR.....-0.5V to V_{CC}
Continuous Current at OUT.....30mA
Voltage at OUT 4V
Continuous Power Dissipation (T_A = +85°C)
20-Bump UCSP (derate 10.0mW/°C above +85°C) 650mW
Operating Junction Temperature.....+150°C
Storage Temperature Range .....-55°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V, R_{LOAD} = 50Ω, $I_{MOD} + I_{BIAS} \le \frac{(V_{CC} - V_{OUT-MIN} - 1.2V)}{50}$, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V, I_{BIAS} = 6.0mA, I_{MOD} = 6.0mA, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Current (Includes Bias and Modulation Currents)	I_{CC}	I_{BIAS} = 10mA, I_{MOD} = 12mA$_{P-P}$, DISABLE = low		106	135	mA
		I_{BIAS} = 1.5mA, I_{MOD} = 3mA$_{P-P}$, DISABLE = low		55	70	
		DISABLE = high		34	50	
SIGNAL INPUT						
Input Impedance		Single ended	42	50	58	Ω
Input Sensitivity	V_{IN-MIN}	(Figure 2)			250	mV$_{P-P}$
Input Overload	V_{IN-MAX}	(Figure 2)	1000			mV$_{P-P}$
LASER MODULATION						
Output Resistance	R_T		42	50	58	Ω
Minimum Modulation	$I_{MOD-MIN}$				3	mA
Maximum Modulation	$I_{MOD-MAX}$		12			mA
Modulation Current When DISABLE = High		V_{IN} = 1000mV$_{P-P}$ (Note 1)		100	250	µA$_{P-P}$
Voltage at OUT	V_{OUT}	(Note 2)	0.7			V
Deterministic Jitter	DJ	(Notes 1, 3)		8	18	ps$_{P-P}$
Random Jitter	RJ	(Note 1)		0.35	0.8	ps$_{RMS}$
Output Switching Time	t_R, t_F	20% to 80% (Notes 1, 4)		28	36	ps
Current Gain from MODSET to OUT				10		mA/mA
LASER BIAS						
Minimum Bias Current	$I_{BIAS-MIN}$				1.5	mA
Maximum Bias Current	$I_{BIAS-MAX}$		10			mA
Current Gain from BIASSET to OUT				10		mA/mA
Bias-Set Current Threshold for Disable		(Note 5)	10	25		µA
Output Current when Disabled		$I_{BIASSET}$ ≤ 10µA or DISABLE = high			250	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.97V to +3.63V, R_{LOAD} = 50Ω, I_{MOD} + $I_{BIAS} \le \frac{(V_{CC} - V_{OUT\text{-}MIN} - 1.2V)}{50}$, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V, I_{BIAS} = 6.0mA, I_{MOD} = 6.0mA, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MONITOR OUTPUT						
MONITOR Gain		$R_{MONITOR}$ = 1kΩ		16		mA/mA
MONITOR Offset Error			-25		+25	µA
MONITOR Gain Variation			-30		+30	%
		V_{CC} and temperature only		±8		
DISABLE INPUT						
Input High Voltage			2.0			V
Input Low Voltage					0.8	V
Input Resistance	R_{DIS}		50	76	100	kΩ
Input Current		-0.3V < $V_{DISABLE}$ < (V_{CC} + 0.3V)	-100		+100	µA
LASER CURRENT PROGRAMMING						
Reference Voltage at BIASSET and MODSET	V_{BG}			1.2		V
Gain Matching of I_{BIAS} and I_{MOD}		(Note 6)	-25		+25	%

Note 1: Guaranteed by design and characterization using the circuit shown in Figure 1.
Note 2: V_{OUT} is the minimum instantaneous voltage at the output (not the average voltage).
Note 3: Measured at 10.7Gbps with a pattern equivalent to 2^{23} - 1 PRBS.
Note 4: Measured at 2.5Gbps with a 0101 repeating pattern.
Note 5: Programming a bias set current ($I_{BIASSET}$) below the threshold disables the output currents.

Note 6: Gain Matching = $100 \times \left(\frac{\text{Bias Gain}}{\text{Modulation Gain}} - 1 \right)$

Measured under the following conditions:
I_{MOD} = 12mA, I_{BIAS} = 4mA
I_{MOD} = 3mA, I_{BIAS} = 4mA
I_{MOD} = I_{BIAS} = 4mA
I_{MOD} = I_{BIAS} = 8mA.

10.7Gbps, +3.3V, Compact VCSEL Driver

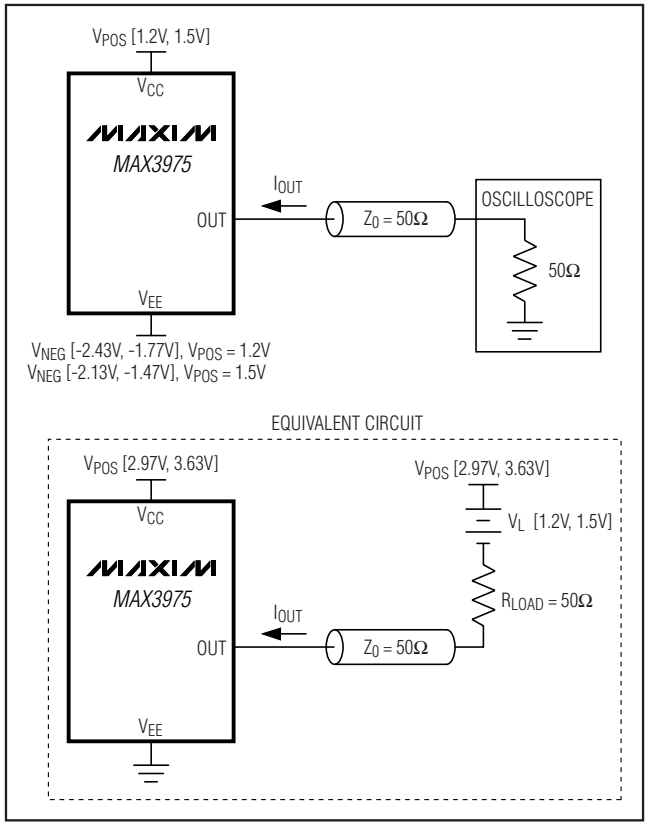


Figure 1. AC Characterization Circuit

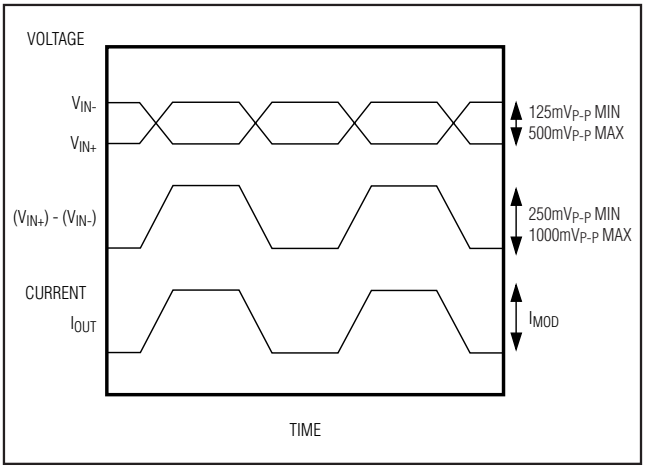
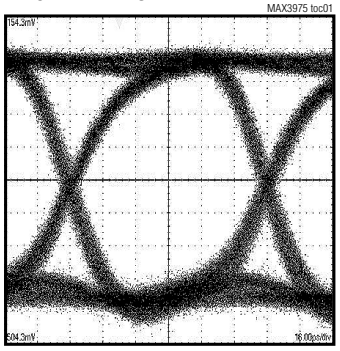


Figure 2. Required Input Signal and Output Polarity

Typical Operating Characteristics

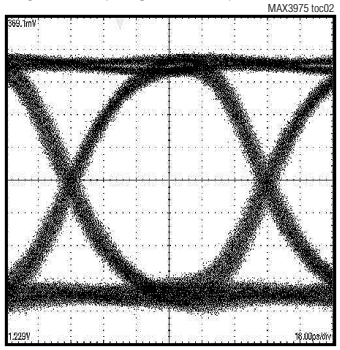
(V_{CC} = +2.97V to +3.63V, R_{LOAD} = 50Ω, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V, I_{BIAS} = 6.0mA, I_{MOD} = 6.0mA, and T_A = +25°C, unless otherwise noted.)

10.3Gbps ELECTRICAL EYE DIAGRAM (I_{BIAS} = 4mA, I_{MOD} = 5mA, 2^{23} - 1 PRBS)



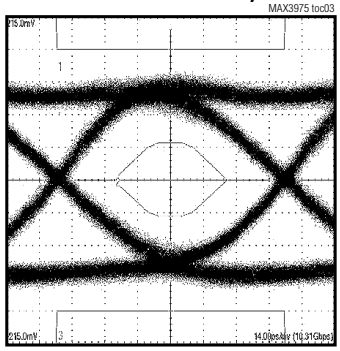
16ps/div

10.3Gbps ELECTRICAL EYE DIAGRAM (I_{BIAS} = 10mA, I_{MOD} = 12mA, 2^{23} - 1 PRBS)



16ps/div

10.3Gbps OPTICAL EYE DIAGRAM (P_{AVG} = -2.0dBm, OMA = 471µW$_{P-P}$, 2^{23} - 1 PRBS) (ADVANCED OPTICAL COMPONENTS VCSEL TOSA HFE6190-561)



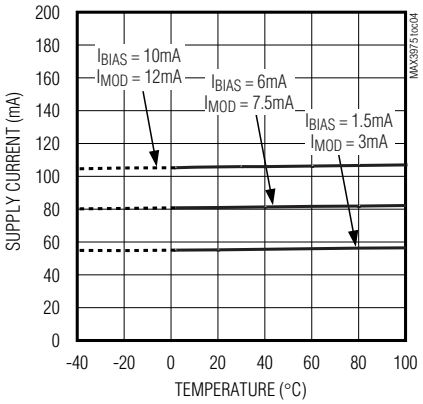
14ps/div

8GHz FILTER, 24% 10GbE MASK MARGIN

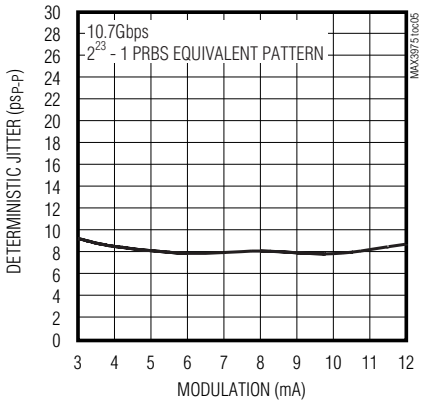
Typical Operating Characteristics (continued)

(V_{CC} = +2.97V to +3.63V, R_{LOAD} = 50Ω, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V, I_{BIAS} = 6.0mA, I_{MOD} = 6.0mA, and T_A = +25°C, unless otherwise noted.)

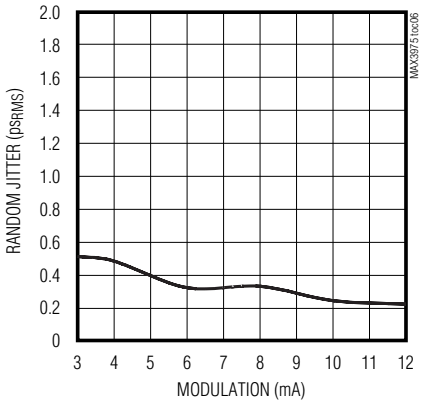
SUPPLY CURRENT vs. TEMPERATURE (INCLUDES I_{BIAS} AND I_{MOD})



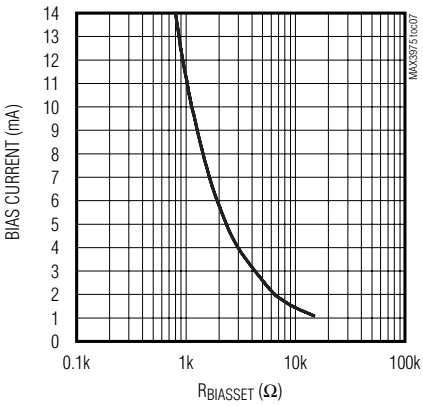
DETERMINISTIC JITTER vs. MODULATION CURRENT



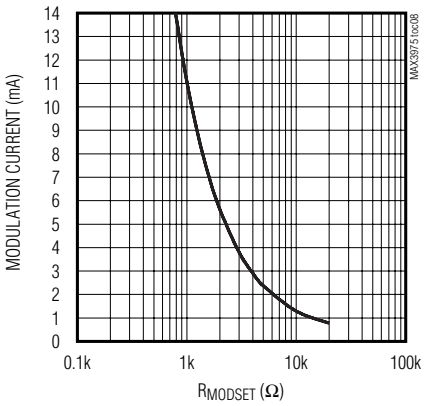
RANDOM JITTER vs. MODULATION CURRENT



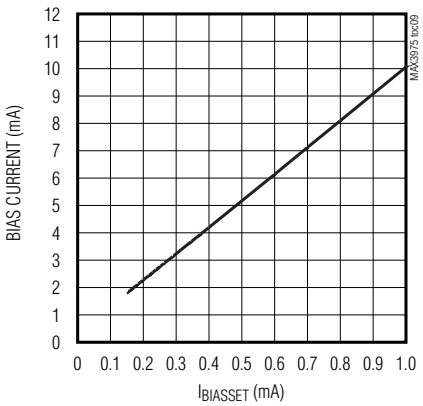
BIAS CURRENT vs. $R_{BIASSET}$



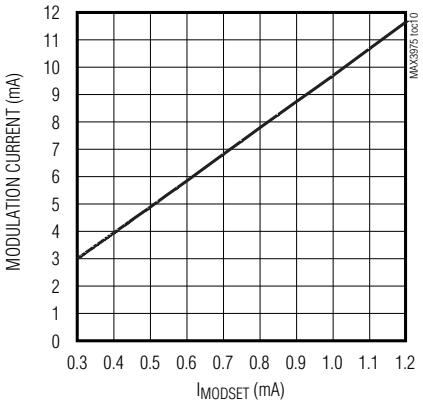
MODULATION CURRENT vs. R_{MODSET}



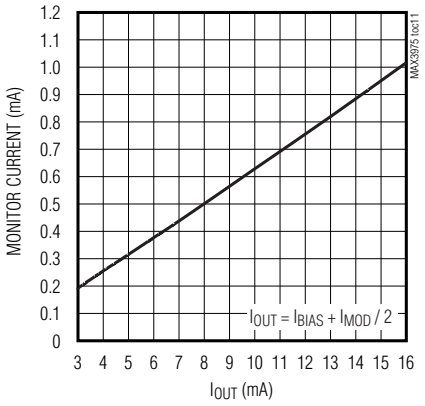
BIAS CURRENT vs. $I_{BIASSET}$



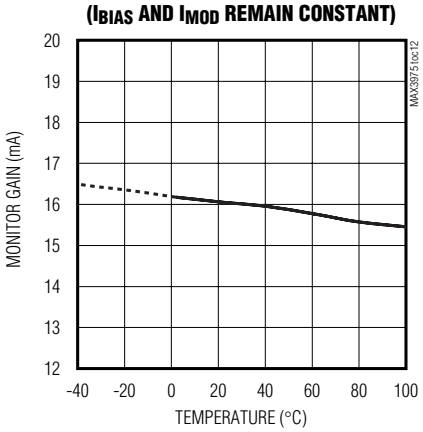
MODULATION CURRENT vs. I_{MODSET}



MONITOR CURRENT vs. I_{OUT}



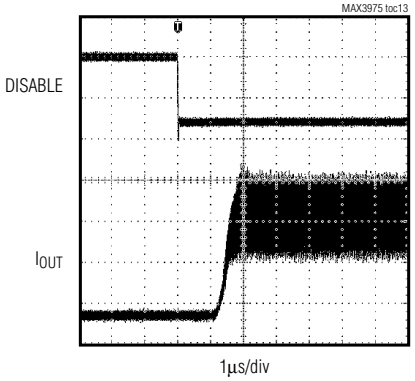
MONITOR GAIN vs. TEMPERATURE (I_{BIAS} AND I_{MOD} REMAIN CONSTANT)



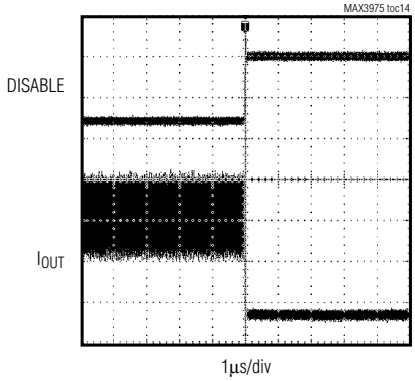
Typical Operating Characteristics (continued)

(V_{CC} = +2.97V to +3.63V, R_{LOAD} = 50Ω, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V, I_{BIAS} = 6.0mA, I_{MOD} = 6.0mA, and T_A = +25°C, unless otherwise noted.)

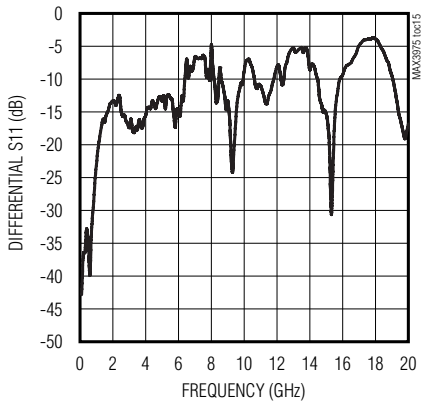
TRANSMITTER ENABLE



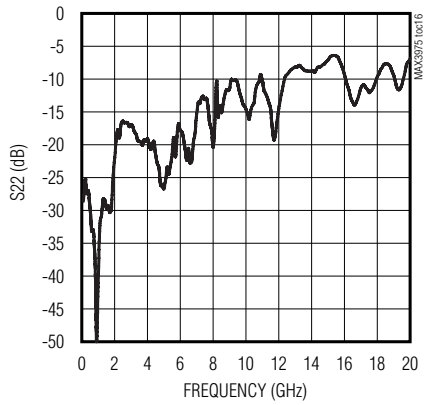
TRANSMITTER DISABLE



S_{11} vs. FREQUENCY (DIFFERENTIAL)



S_{22} vs. FREQUENCY (SINGLE ENDED)



Pin Description

PIN	NAME	FUNCTION
A1, D1, E1, E2	V_{CC}	+3.3V Supply Voltage. All V_{CC} pins must be connected to the supply voltage.
A2	IN-	Negative Data Input. Includes 50Ω to V_{CC} on-chip termination resistor.
A3	DISABLE	Transmitter Disable, TTL Compatible. Total VCSEL current is low when this pin is set to a TTL high (asserted) or left open. VCSEL current is enabled when this input is set to a TTL low (deasserted).
A4	IN+	Positive Data Input. Includes 50Ω to V_{CC} on-chip termination resistor.
A5, B1, D5, E4, E5	V_{EE}	Supply Ground. All V_{EE} pins must be connected to the supply ground.
B2, B4, D2, D4	N.C.	No Connection. These pins must be soldered to the circuit board but should not be electrically connected to any circuit nodes (left floating).
B5	MODSET	Modulation Current Set Pin, Analog. A resistor connected from this pin to V_{EE} sets the desired modulation current. Modulation current can also be programmed with a current-sinking digital-to-analog converter (DAC) or voltage DAC with series resistor. See Figure 4.
C1	MONITOR	VCSEL DC Current Monitor, Analog. Current from this output is proportional to the VCSEL DC current. Connect to V_{EE} if not required in the application.
C5	BIASSET	Bias Current Set Pin, Analog. A resistor connected from this pin to ground sets the desired bias current. Bias current can also be programmed with a current-sinking DAC or voltage DAC with series resistor. See Figure 4. Programming a current below the bias-set current threshold disables the driver output.
E3	OUT	Modulation and Bias Current Output (Current Flows from VCSEL to OUT). Connect to VCSEL cathode.

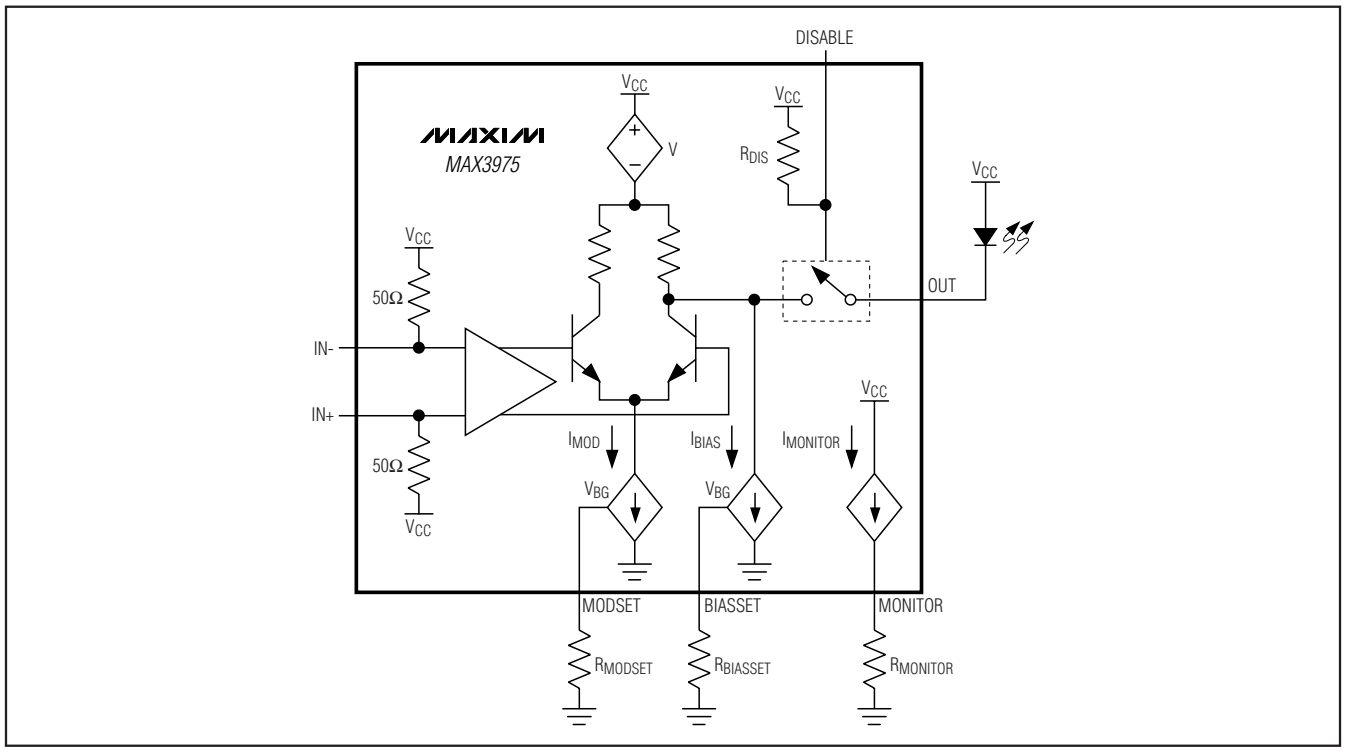


Figure 3. Functional Diagram

10.7Gbps, +3.3V, Compact VCSEL Driver

Detailed Description

The MAX3975 VCSEL driver consists of a high-speed modulator with programmable modulation and bias currents, transmitter disable circuit, and output-current monitor (Figure 3). The MAX3975 operates from a +3.3V supply and provides a 50Ω output termination, 3mA to 12mA of modulation, and 1.5mA to 10mA of bias current, allowing operation with a variety of 10Gbps VCSELs.

Modulation Circuit

The modulation circuitry consists of an input buffer, a current mirror, and a high-speed current switch. The modulator drives up to 12mA of modulation with a 50Ω VCSEL load.

The amplitude of the modulation current at OUT (I_{MOD}) is linearly proportional to the control current at MODSET and is given by the relationship:

$$I_{MOD} = I_{MODSET} \times 10$$

The control current is programmed with a resistor from MODSET to V_{EE}. The control current can also be programmed with a current-sinking DAC or voltage DAC with series resistor as shown in Figure 4.

Biasing Circuit

The biasing circuitry consists of a current mirror that is connected to the driver output. Bias and modulation currents are combined internally, eliminating the need for an external bias inductor. The biasing circuit provides up to 10mA of bias current with a 50Ω VCSEL load.

The bias current at OUT (I_{BIAS}) is linearly proportional to the control current at BIASSET and is given by the relationship:

$$I_{BIAS} = I_{BIASSET} \times 10$$

The control current is programmed with a resistor from BIASSET to V_{EE}. The control current can also be programmed with a current-sinking DAC or voltage DAC with series resistor as shown in Figure 4. Programming a set current below the bias-set current threshold disables the driver output.

Transmitter Disable

The MAX3975 is equipped with a transmitter disable control (DISABLE). The DISABLE input is a TTL-compatible, low-current digital input. When DISABLE is set to TTL high (asserted) or left open, both the modulation and bias currents are disabled. The modulation and bias currents are enabled when DISABLE is set to TTL low (deasserted), and $I_{BIASSET}$ is above the disable threshold.

Output Current Monitor

The MONITOR is a current output that provides an indication of the VCSEL DC current. Connecting a resistor ($R_{MONITOR}$) from the MONITOR output to V_{EE} gives the following relationship:

$$V_{MONITOR} = (1/16) \times (I_{BIAS} + (I_{MOD} / 2)) \times R_{MONITOR}$$

where, $(I_{BIAS} + (I_{MOD} / 2))$ = VCSEL DC current.

The voltage at the monitor output must be less than 2.18V for compliance. The recommended range for $R_{MONITOR}$ is 500Ω to 1.2kΩ, with 1kΩ being typical. MONITOR must be connected to V_{EE} if not required in the application.

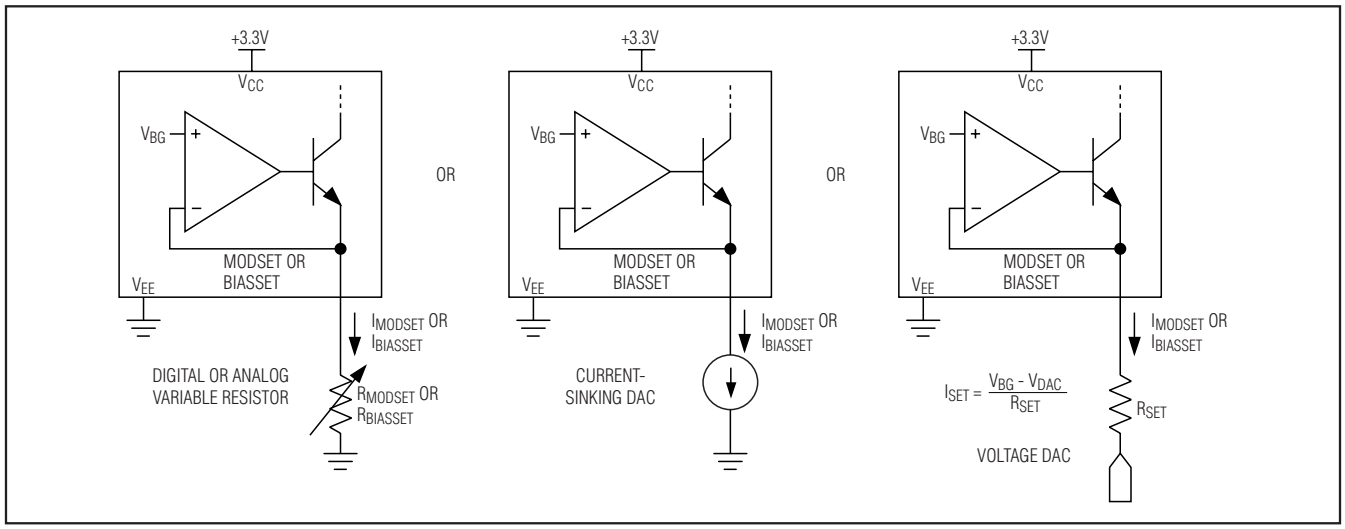


Figure 4. Bias and Modulation Current Controls

Table 1. Optical Power Relations

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVG}	$P_{AVG} = (P_0 + P_1) / 2$
Extinction Ratio	E_r	$E_r = P_1 / P_0$ $E_r = (2P_{AVG} + OMA) / (2P_{AVG} - OMA)$
Optical Power of a 1	P_1	$P_1 = 2P_{AVG} E_r / (E_r + 1)$
Optical Power of a 0	P_0	$P_0 = 2P_{AVG} / (E_r + 1)$
Optical Modulation Amplitude	OMA	$OMA = P_1 - P_0 = 2P_{AVG} (E_r - 1) / (E_r + 1)$
Laser Slope Efficiency	η	$\eta = OMA / I_{MOD}$
Modulation Current	I_{MOD}	$I_{MOD} = OMA / \eta$
Bias Current	I_{BIAS}	$I_{BIAS} = I_{TH} + (P_0 \times \eta)$

Note: *Assuming a 50% average input duty cycle and mark density.*

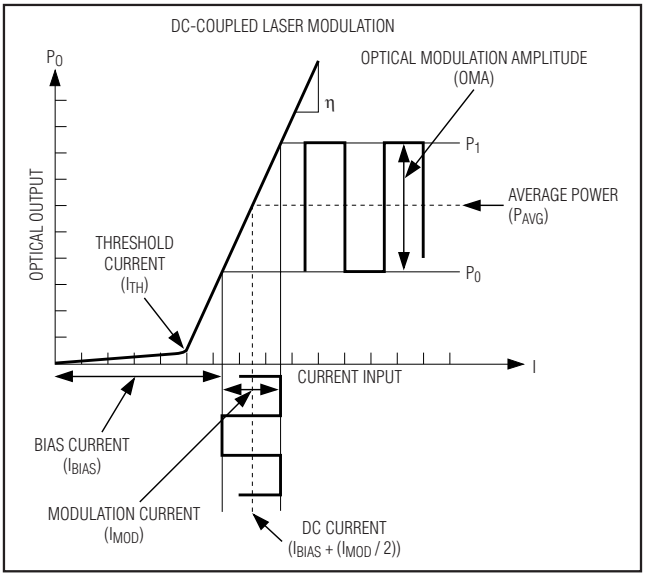


Figure 5. Optical Power Relations

Design Procedure

Interfacing with VCSELs

The MAX3975 modulating output (OUT) is optimized to interface directly to the cathode of a common-anode VCSEL. No external components are required between the VCSEL cathode and the driver output.

A 50Ω controlled-impedance transmission line with minimal length should be used between the VCSEL and the driver output. The VCSEL should be a high-speed, high-efficiency laser that requires low modulation current and generates a low voltage swing. Use a broadband supply filter at the VCSEL anode.

The minimum instantaneous voltage at OUT is 0.7V. To obtain fast edge transitions and low jitter, a VCSEL, supply voltage, and packaging technology must be selected that ensures V_{OUT} is within the operating range of the driver output.

Programming the Modulation Current

For a desired optical modulation amplitude (OMA), the required modulation current can be calculated based on the laser slope efficiency (η) using the equations in Table 1. To program the desired modulation current, connect a resistor from MODSET to V_{EE}. See the Modulation Current vs. R_{MODSET} graph in the *Typical Operating Characteristics* to select the value of R_{MODSET} that corresponds to the required modulation current. When using an external DAC as shown in Figure 4, see the Modulation Current vs. I_{MODSET} graph in the *Typical Operating Characteristics.*

Programming the Bias Current

For a desired laser average optical power, P_{AVG}, the required bias current can be calculated based on the laser slope efficiency (η) and threshold current (I_{TH}) using the equations in Table 1. To program the desired bias current, connect a resistor from BIASSET to V_{EE}. See the Bias Current vs. $R_{BIASSET}$ graph in the *Typical Operating Characteristics* to select the value of $R_{BIASSET}$ that corresponds to the required bias current. When using an external DAC as shown in Figure 4, see the Bias Current vs. $I_{BIASSET}$ graph in the *Typical Operating Characteristics.*

Closed-Loop Operation

Closed-loop power control can be implemented by using a controller IC as shown in the *Typical Application Circuit* on page 1. The controller IC monitors the photodiode current then adjusts the resistance/current seen by the BIASSET pin to maintain average power of the optical output over temperature and laser lifetime. Optical modulation amplitude (OMA) control is achieved by using a temperature indexed lookup table to control the resistance/current seen by the MODSET pin. The time constant from MODSET/BIASSET to OUT is typically 175ns.

Safety and Power Sequencing

For safety fault protection and proper power sequencing, use a low on-resistance MOSFET between the VCSEL power supply and the VCSEL anode, as shown in the *Typical Application Circuit*. A power-on-reset circuit and the safety fault signal of the controller IC (if applicable) should control the MOSFET gate.

The power-on-reset circuit should be designed to disable the VCSEL when the driver supply voltage is below 2.9V. This prevents the VCSEL from producing excessive optical output while the driver powers up/down.

UCSP Assembly Considerations

The MAX3975 is packaged in a 2.5mm x 2.5mm, chip-scale package (5 x 5 UCSP). Five of the solder ball positions (B3, C2, C3, C4, D3) are not populated (package code B25-4). For the latest application details on UCSP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note: UCSP—*A Wafer-Level Chip-Scale Package available on Maxim's website at www.maxim-ic.com/ucsp*.

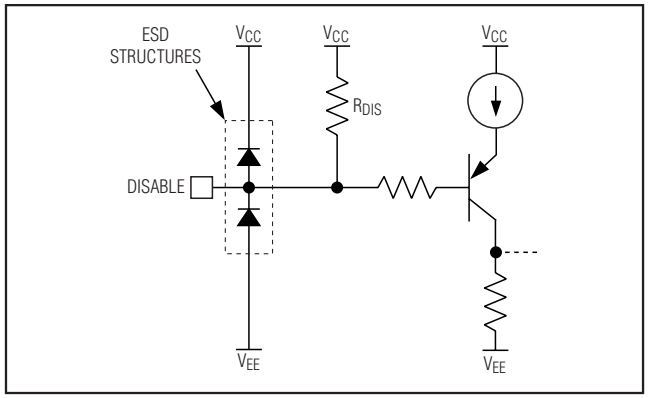


Figure 6. Simplified DISABLE Input Structure

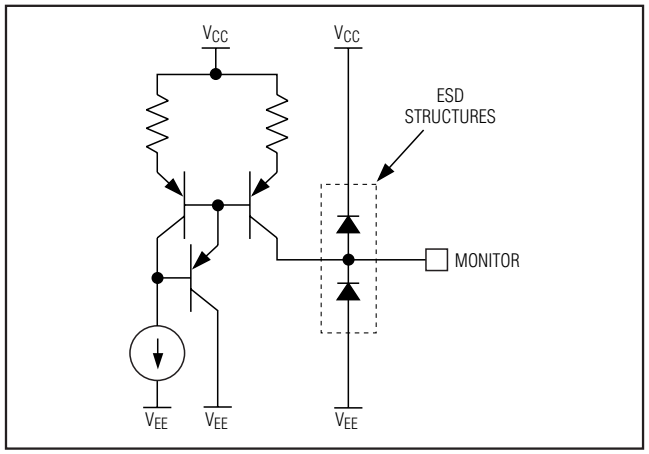


Figure 7. Simplified MONITOR Output Structure

Applications Information

Interface Models

Figures 6, 7, 8, and 9 show simplified input and output circuits.

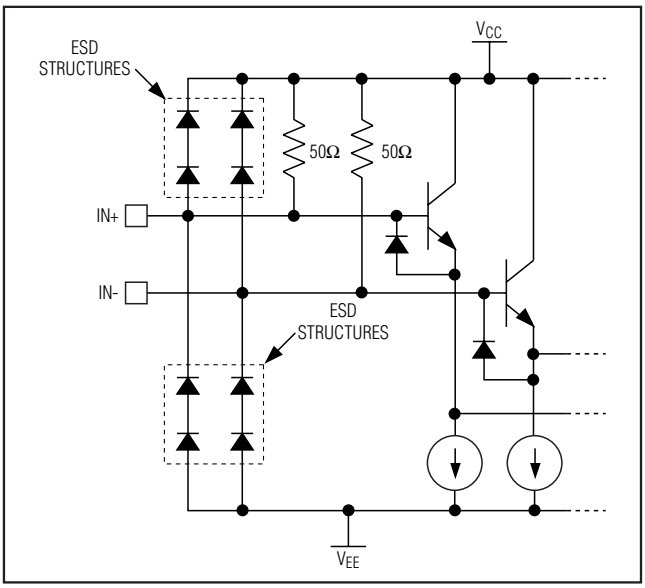


Figure 8. Simplified Data Input Structure

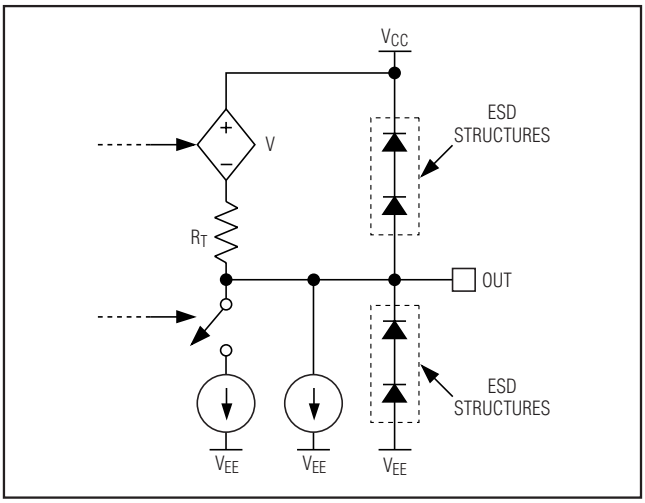


Figure 9. Simplified Data Output Structure

Layout Considerations

Design a broadband supply filter that provides low impedance between 10kHz and 15GHz. Use controlled-impedance transmission lines to interface to the high-speed input and output of the MAX3975. The parasitic capacitance at BIASSET and MODSET must be less than 20pF to ensure stability of the current controls.

Chip Information

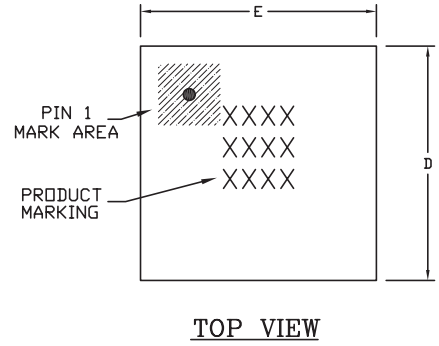
TRANSISTOR COUNT: 1387

PROCESS: SiGe Bipolar

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

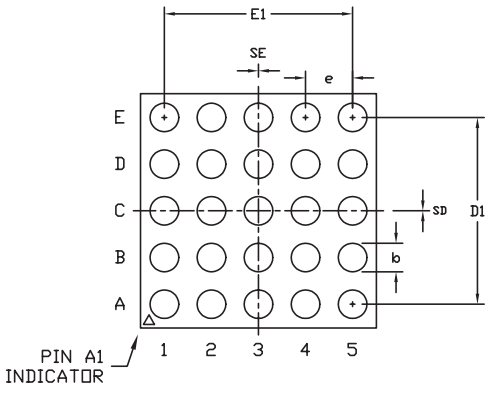
25L, UCSP.EPS



TOP VIEW

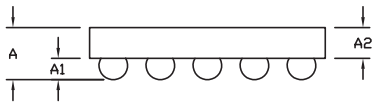
COMMON DIMENSIONS	
A	0.62±0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D	2.54±0.08
D1	2.00 BASIC
E	2.54±0.08
E1	2.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	DEPOPULATED SOLDER BALLS
B25-1	NONE
B25-2	D2, D3, D4
B25-3	B2, B3, B4
B25-4	B3, C2, C3, C4, D3



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 5x5 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0096	H	1/1

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