

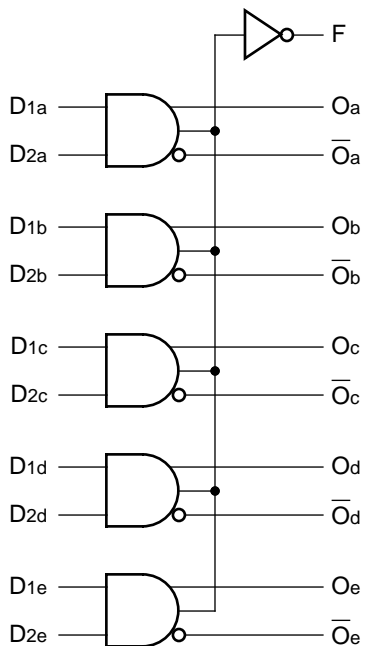
**FEATURES**

- Max. propagation delay of 1050ps
- IEE min. of -60mA
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 40% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

**DESCRIPTION**

The SY100S304 is an ultra-fast quint AND/NAND gate designed for use in high-performance ECL systems. This device also features a Function (F) output which is the wire-NOR of the AND gate outputs. The inputs on the device have 75KΩ pull-down resistors.

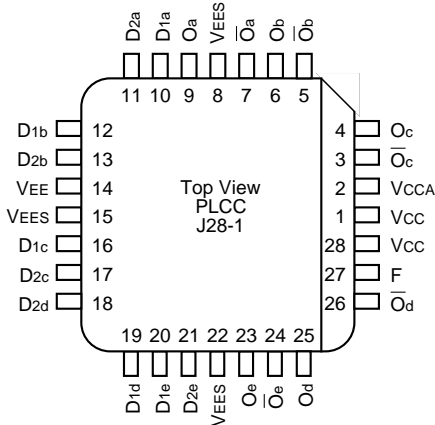
**BLOCK DIAGRAM**



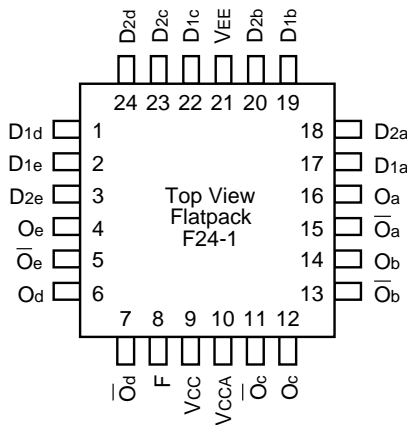
**PIN NAMES**

Pin	Function
Dna – Dne	Data Inputs (n-1...5)
E	Enable Input
Oa – Oe	Data Outputs
O-bara – O-bare	Complementary Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

**PACKAGE/ORDERING INFORMATION**



**28-Pin PLCC (J28-1)**



**24-Pin Cerpack (F24-1)**

**Ordering Information**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S304FC	F24-1	Commercial	SY100S304FC	Sn-Pb
SY100S304FCTR <sup>(1)</sup>	F24-1	Commercial	SY100S304FC	Sn-Pb
SY100S304JC	J28-1	Commercial	SY100S304JC	Sn-Pb
SY100S304JCTR <sup>(1)</sup>	J28-1	Commercial	SY100S304JC	Sn-Pb
SY100S304JZ <sup>(2)</sup>	J28-1	Commercial	SY100S304JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S304JZTR <sup>(1, 2)</sup>	J28-1	Commercial	SY100S304JZ with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

**DC ELECTRICAL CHARACTERISTICS**

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I <sub>IH</sub>	Input HIGH Current	—	—	250	μA	V <sub>IN</sub> = V <sub>IH</sub> (Max.)
	D <sub>2a</sub> — D <sub>2e</sub> D <sub>1a</sub> — D <sub>1e</sub>	—	—	250		
I <sub>EE</sub>	Power Supply Current	-60	-40	-30	mA	Inputs Open

**AC ELECTRICAL CHARACTERISTICS****CERPACK**

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

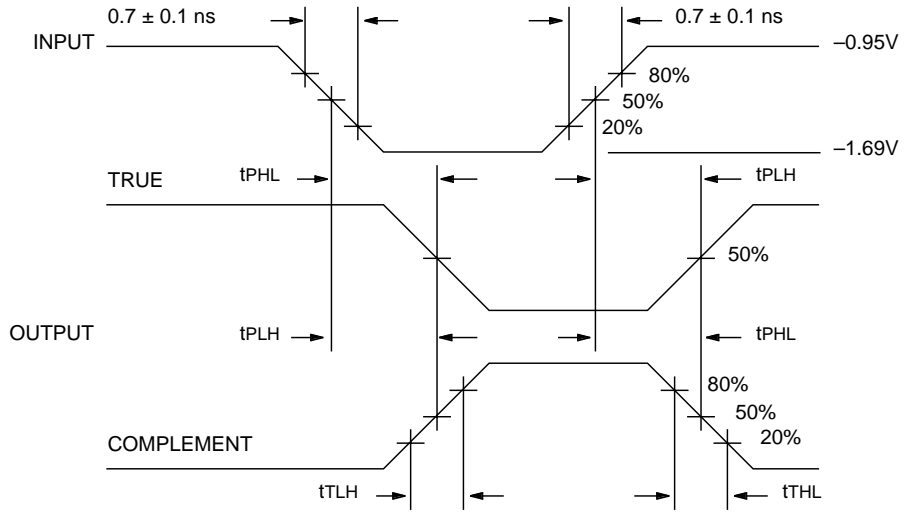
Symbol	Parameter	T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D <sub>na</sub> — D <sub>ne</sub> to O, $\bar{O}$	300	1150	300	1150	300	1150	ps	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to F	600	1650	600	1650	600	1650	ps	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

**PLCC**

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D <sub>na</sub> — D <sub>ne</sub> to O, $\bar{O}$	300	1050	300	1050	300	1050	ps	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to F	600	1550	600	1550	600	1550	ps	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

**TIMING DIAGRAM**

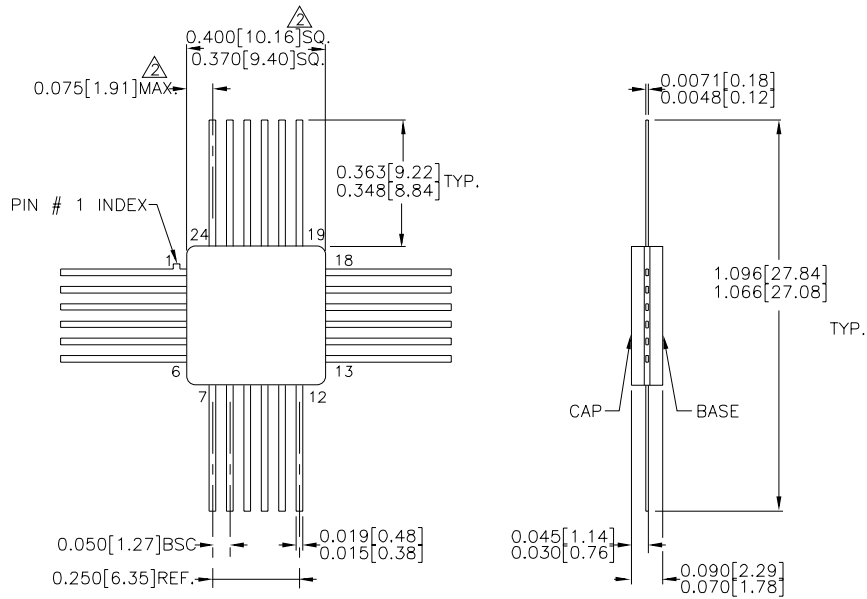


**Propagation Delay and Transition Times**

**NOTE:**

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

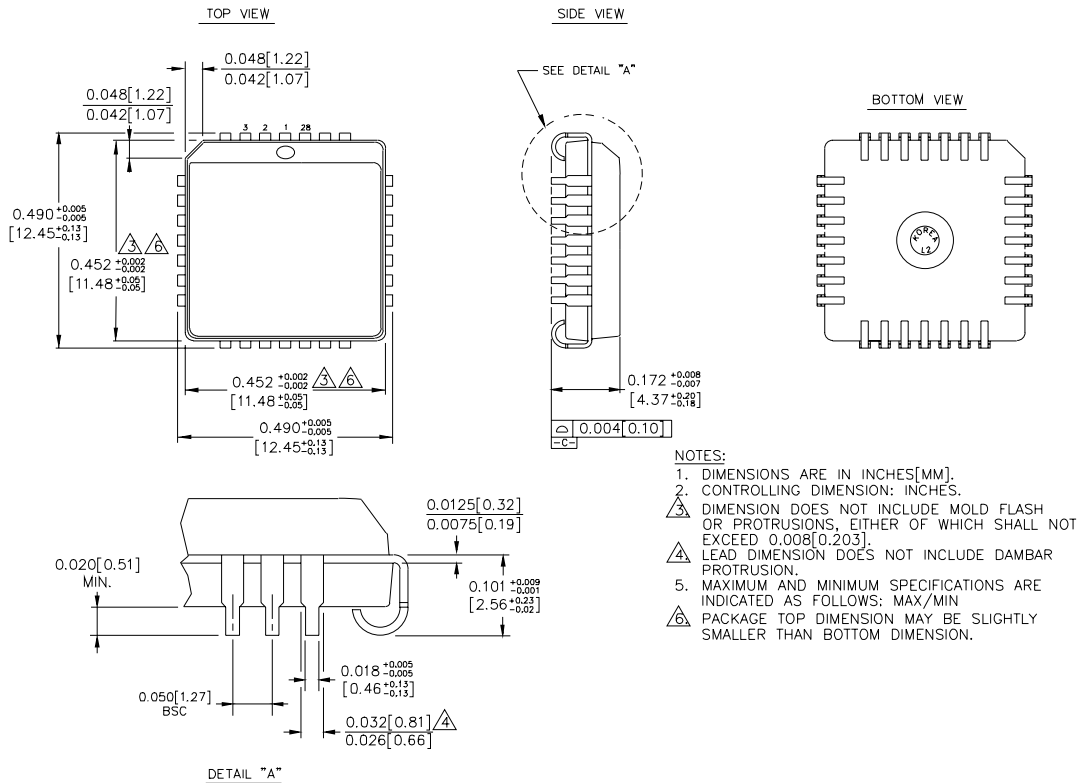
**24-PIN CERPACK (F24-1)**



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
  2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
  3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

**28-PIN PLCC (J28-1)**



Rev. 03

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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