Intel® IXP2350 Network Processor

Enables access and edge applications to 2 Gbps

Product Highlights

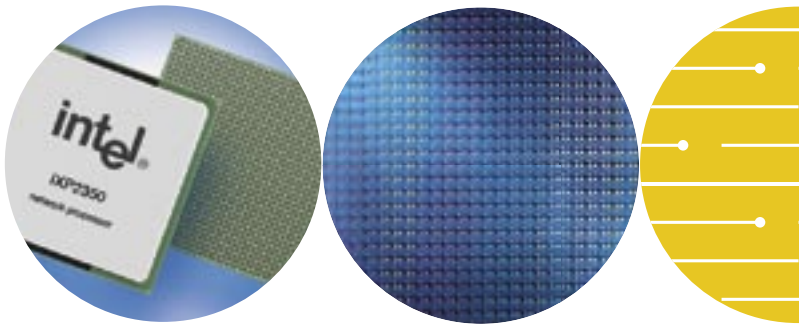
- Four fully programmable multi-threaded micro-engines with large control store memory for single chip packet forwarding and traffic management, up to 4.9 giga-operations per second
- An integrated low power 32-bit Intel XScale® core utilizes a dedicated memory controller, cache coherency and L2 push cache for high performance control plane processing
- Extensive integration of standards-based physical interconnects, high speed serial processing and cryptography acceleration features save on cost, power and board area
- Comprehensive development environment enables rapid product development and prototyping
- Application building blocks from Intel and third-party providers speed time-to-market
- Low power consumption and compact packaging reduce system cost
- Intel® Internet Exchange Architecture (Intel® IXA) Software Framework enables customers to reuse software and reduce development risk

Product Overview

Equipment designed for network access and edge applications requires great processing performance to support value-added network services at T1/E1 to 2 Gbps line rates. Network equipment vendors must rapidly add these new services and continue to minimize development time and cost. To meet these needs and extend time-in-market, network processors must combine performance with programming flexibility. In addition, by implementing standards-based interfaces, vendors can integrate components more easily and leverage software investments by reusing code. This can dramatically speed time-to-market and lower development costs.

With the addition of the Intel® IXP2350 network processor to the product line, the Intel® IXP2XXX network processors now support scalable performance from T1/E1 to OC-192/10 Gbps. This mid-range product extends Intel's fully programmable architecture to new, lower cost/performance points for access and edge applications, including broadband access devices, wireless infrastructure systems, routers and multi-service switches. The IXP2350 network processor is fully programmable, integrating key architectural features from the Intel® IXP42X and IXP2XXX product lines to support wire speed deep packet inspection, traffic management and forwarding on a single chip. Its store-and-forward architecture combines an enhanced high performance Intel XScale core, four 32-bit independent multi-threaded micro-engines, hardware-based cryptography acceleration, and a 256 HDLC channel controller to deliver up to 4.9 giga-operations per second.

www.intel.com/go/networkprocessors



The Intel® IXP2350 network processor is offered in various speed and temperature options.

The Intel® IXP2350 network processor has the processing power to run applications that previously required expensive high-speed ASICs.

To meet today's and tomorrow's demanding data-plane performance requirements, the Intel IXP2350 network processor provides a powerful, integrated control plane processor in the same chip. The high-speed core (up to 1.2 GHz) incorporates advanced I/O and memory features, such as a dedicated memory controller, cache coherency and L2 push cache, enabling customers to eliminate an external control plane processor in many applications. For instance, in a 3G base-station transport line card, heavy-duty 3G control signaling and IKE cryptography functions can be performed using the IXP2350 network processor's built-in control plane processor.

Additional hardware-assisted features in the IXP2350 network processor increase data plane performance and simplify development. In addition to local memory for microengines, the IXP2350 network processor includes built-in resources for tasks such as Asynchronous Transfer Mode (ATM) segmentation and reassembly (SAR), time stamps to support flow metering, and a multiply function for complex algorithm calculations such as Quality of Service (QoS). And, the network processor automates packet manipulation for byte alignment to improve developer productivity and streamline code flows.

Application Flexibility

The IXP2350 network processor can support up to full duplex 2 Gbps line rates (or OC-12/1 Gbps line rates with significant headroom), making it ideal for a wide variety of applications such as:

- DSL Access Multiplexers (DSLAMs)
- 2.5G and 3G wireless infrastructure Radio Access Network transport layers
- Wireless Local Area Network (WLAN) access point aggregation gateways
- WiMAX (802.16x) basestations
- Wide Area Networking (WAN) multi-service switches
- Cable Modem Termination System (CMTS) equipment
- Enterprise routers

The programmability of the IXP2350 network processor also makes it well suited for voice over IP gateways, multi-service access platforms, remote access concentrators, Virtual Private Network (VPN) gateways, and various appliances.

Apply the IXP2350 network processor in such usage models as:

- Aggregation, ATM SARing, traffic shaping, policing, forwarding and protocol conversion in either trunk cards or as intelligent line cards in DSLAMs/ mini-DSLAM equipment
- Aggregation, forwarding and protocol conversion in CMTS equipment
- ATM SARing, encryption, forwarding and protocol conversion in a basestation/radio network controller
- GTP tunneling and IPv6 forwarding in wireless infrastructure
- Aggregation, traffic shaping, policing, forwarding and protocol conversion in either WLAN switches or WiMAX basestations
- ATM SARing, traffic shaping, policing, protocol conversion and aggregation for WAN multi-service switches
- Content-aware load balancing, forwarding and policing for appliances
- Multi-gigabit aggregation with forwarding and QoS in a WLAN access point aggregation gateway
- Virtual Local Area Network (VLAN), forwarding, QoS handling in excess of 3 million packets per second in an enterprise router application

Hardware Architecture Innovations

Key to the performance capabilities of the Intel® IXP2350 network processor is Intel's unique network processing approach that allows a single-stream packet/cell-processing problem to be deconstructed into multiple, sequential tasks that can be easily linked together. The hardware design uses fast and flexible sharing of data and event signals among threads and microengines to manage data-dependent operations among multiple parallel processing stages with low latency. This combination of flexible software pipelining and fast interprocess communication enables the IXP2350 network processor to deliver rich processing capability at line rates from T1/E1 to 2 Gbps.

Intel's network processor architecture implements major innovations to ensure low latency communication among processes:

- Next Neighbor registers enable individual microengines to rapidly pass data and state information to adjacent microengines.
- Reflector Mode pathways ensure that multiple microengines can share data and global event signals using 32-bit, unidirectional buses that connect the IXP2350 network processor internal processing and memory resources.

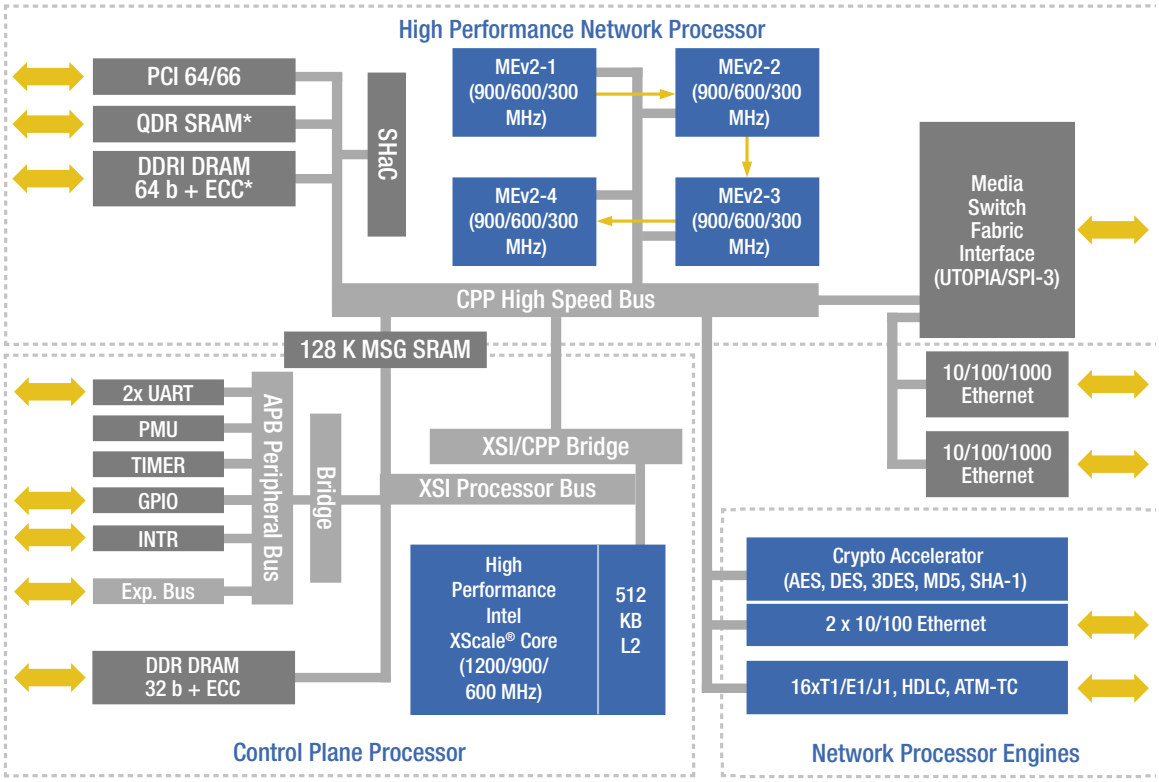


Figure 1: Intel® IXP2350 Network Processor Block Diagram
***Not available on 300 MHz MEv2 configurations**

- Ring Buffer registers provide a highly efficient mechanism for flexibly linking tasks among multiple software pipelines. Ring buffers allow developers to establish "producer-consumer" relationships among microengines, efficiently propagating results along the pipeline in FIFO order. To minimize latency associated with external memory references, register structures are complemented by 16 entries of Content Addressable Memory (CAM) associated with each microengine. Configured as a distributed cache, the CAM enables multiple threads and microengines to manipulate the same data simultaneously while maintaining data coherency.

The high performance Intel® IXP2350 network processor delivers programmability to speed the deployment of intelligent network services. Intel® IXA, Intel's network processor architecture, enables applications developed for the IXP2350 network processor to scale across other applications and to successive generations of networking products. Intel IXA includes a common set of development tools for the Intel® IXP2XXX product line, providing a comprehensive development environment that can dramatically accelerate time-to-market and extend customers' investments in software.

Development Environment

The Intel IXP2350 development environment includes the Intel® Internet Exchange Architecture software developers kit (Intel® IXA SDK) complemented by a hardware development platform with supporting software and tools. The SDK provides high-level tools, embedded operating system support, the Intel IXA Software Framework, software building blocks/libraries and reference applications that enable customers to evaluate, demonstrate, and tune performance and develop applications for the network processor to meet product requirements and minimize time-to-market.

The hardware development platform comprises an industry-standard form factor chassis, an IXP2350 baseboard, and a choice of modular media cards for maximum design flexibility. Complementary software and silicon from members of the Intel® Communications Alliance and other third-party providers are designed to work together to provide the flexibility, scalability and performance levels required to meet the demands of tomorrow's high-performance networks.

Features	Benefits
Four integrated programmable microengines (MEv2) with 8K instruction program stores running up to 900 MHz.	Flexible multi-threaded RISC processors can be programmed to deliver intelligent transmit and receive processing, with robust software development environment for rapid product development.
Integrated Intel XScale® core: • 32 Kbytes - Instruction cache • 32 Kbytes - Data cache • Up to 1,200 MHz	Embedded 32-bit RISC core for high performance processing of complex algorithms, route table maintenance and system-level management functions. Lowers system cost by eliminating external host processor.
Integrated 512 Kbytes L2 push cache	Improves CPU performance and MEv2-to-Intel XScale core and PCI-to-Intel XScale core communication.
Two unidirectional 32-bit media interfaces (Rx and Tx) programmable as SPI-3 or UTOPIA. Each path configurable for 4x8-bit, 2x16-bit, 1x32-bit or combinations of 8 & 16-bit data paths.	Supports industry standard cell and packet interfaces to media and fabric devices; simplifies design and interface to custom ASIC devices. Supports up to 127 ports using a 16-bit UTOPIA-2 MPHY mode.
Two integrated Gigabit Ethernet MACs	Lowers system cost, power and board real estate.
Two integrated 10/100 Ethernet MACs	Can be used as debugging ports or control signal ports. Lowers system cost, power and board real estate.
Integrated high speed serial controller: • 256 HDLC channel controller • ATM-TC • Up to 16xT1/E1/J1 TDM links	Performs inverse multiplexing over ATM (IMA), which provides lower system cost, power and board real estate.
Integrated cryptography accelerator	Provides up to 200 Mbps bulk encryption (DES/SHA-1) capability. Supports AES, DES and 3DES encryption algorithms as well as SHA-1 and MD5 hashing algorithms.
Two industry standard DDR DRAM interfaces: • One 64-bit + ECC DDR300 low latency channel (up to 2 GB) optimized for microengine use (not available on 300 MHz MEv2 configuration) • One 32-bit + ECC DDR300 low latency channel (up to 1 GB) optimized for the Intel XScale core	Memory subsystem supports the network processor store-and-forward processing model. Separate memory channels for Intel XScale core and microengines improves data plane and control plane performance.
I/O coherency for Intel XScale core DRAM	Improves performance through accelerated control plane/data plane communications.
One industry standard QDR SRAM interface (not available on 300 MHz MEv2 configuration)	Provides industry standard interface for memory subsystem for look-up tables and access lists, or co-processors (such as CAM/TCAM).
Asynchronous control interface supports 8 or 16-bit slow port devices via 16-bit expansion bus.	Provides control interface for connecting to microprocessor port of PHY devices and flash memory. Provides a direct connection to DSP via HPI.
Hardware support for memory access queuing	Simplifies application development and reduces system cost.
JTAG support	Improves hardware debug ability.
Intel® IXA Software Development Kit (SDK) Intel® Hardware Development Platform	Industry standard AdvancedTCA* form factor hardware reference design and state of the art development tools improves time to market via robust hardware and software development tools.
1752 ball FCBGA 42.5 mm x 42.5 mm package	Minimizes board layers, providing easier board layer routing and lower cost.

Specifications

Description	Specification
Intel® IXP2350 NPU variants	• 600/300 (600 MHz Intel XScale® core/300 MHz 4ME) • 900/600 (900 MHz Intel XScale core/600 MHz 4ME) • 900/900 (900 MHz Intel XScale core/900 MHz 4ME) • 1200/600 (1200 MHz Intel XScale core/600 MHz 4ME)
Microengine (MEv2) operating frequency	300 MHz, 600 MHz, 900 MHz
Intel XScale core operating frequency	600 MHz, 900 MHz, 1200 MHz
Microengine program control stores	8K instructions (8K x 40-bit) per microengine
Receive interface (UTOPIA, SPI-3)	• Completely independent from Tx path • 32 data signals, 2 clocks, control & parity signals • 3.3V LVTTL signaling (single edge) w/global synch clocking • Configurable for UTOPIA (1/2/3); SPI-3 (POS-PHY 2/3) • UTOPIA & SPI-3 modes enable combination of 16-bit and 8-bit channels • Up to 104 MHz operation
Transmit interface (UTOPIA, SPI-3)	• Completely independent from Rx path • 32 data signals, 2 clocks, control & parity signals • 3.3V LVTTL signaling (single edge) w/global synch clocking • Configurable for UTOPIA (1/2/3); SPI-3 (POS-PHY 2/3) • UTOPIA & SPI-3 modes enable combination of 16-bit and 8-bit channels • Up to 104 MHz operation
Gigabit Ethernet MAC with GMII/RGMII/MII/TBI interface	• Up to two • Depending on the operating modes, not all Gigabit Ethernet ports may be available
10/100 Ethernet MACs with MII/RMII interfaces	Two for debug or control signal ports
Integrated high-speed serial controller	• 256 HDLC channel controller • ATM over serial controller • Up to 16xT1/E1/J1 TDM links • ATM-TC
Integrated cryptography accelerator	• AES, DES, and 3DES encryption algorithms • SHA-1 and MD5 hashing algorithms • Cryptography will be enabled via firmware provided by Intel
Additional integrated hardware features	• Hardware hash unit (48, 64 and 128-bit) • 16 Kbytes scratchpad memory • 128 Kbytes message SRAM • Two serial UART ports for debug • Up to 16 general-purpose I/O pins • Four 32-bit timers • Interrupt controller • Watchdog • General-purpose timer • Configurable 24-bit address expansion bus controller supporting 8 or 16-bit parallel microprocessor port, 8/16-bit flash and HPI
PCI interface	64 or 32-bit PCI 2.2 compliant interface running at 66 MHz or 33 MHz
SRAM interface (QDR) One channel (not available on 300 MHz MEv2 configuration)	Supports both QDR I and QDR II. Peak bandwidth of 1.6 GBps per channel at frequency of 200 MHz (800 Mbytes/sec read, 800 Mbytes/sec write); up to 16 Mbytes per channel; parity protected.
DDR DRAM Two channels: • CPP 64-bit DDR controller for MEv2 (not available on 300 MHz MEv2 configuration) • XSI 32-bit DDR controller for Intel XScale core	 • CPP Channel: Peak bandwidth of 2.4 GBps (19.2 Gbps) per channel at frequency of 150 MHz, up to 2 Gbytes memory; ECC protected; 64-bit wide interface • XSI Channel: Peak bandwidth of 1.2 GBps (9.6 Gbps) per channel at frequency of 150 MHz, up to 1 Gbyte memory; ECC protected; 32-bit wide interface
Commercial operating temperature Extended operating temperature	• 0º to +70º C • -40º to +85º C
Power supply	• Vdd=1.2 V+/-5% (Core) • Vdd1=1.5V+/-5% (QDR) • Vdd2=2.5V+/-5% (DDR) • Vdd3=3.3V+/-5% (Media, PCI, I/O)
Power dissipation	• 6.0 Watts typical, 7.5 Watts max*** 600/300 • 9 Watts typical, 10 Watts max*** 900/600 • 11 Watts typical, 12.2 Watts max*** 900/900 • 9 Watts typical, 11 Watts max*** 1200/600 ***Can be further reduced by not using all of the I/Os
Package	1752-ball FCBGA 42.5 mm x 42.5 mm
Solder ball pitch	1 mm

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Intel® Internet Exchange Architecture (Intel® IXA)

Intel® IXA is a packet processing architecture that provides a foundation for software portability across multiple generations of network processors. Intel IXA is based on programmable microengines, Intel XScale® technology and the Intel IXA Software Framework. Additional information on Intel IXA and the Intel network processor product line is available at the addresses listed below.

Intel® Communications Alliance

With Intel development platforms, developers can design comprehensive systems combining products from Intel and third-party vendors to accelerate time-to-market and reduce development costs. For more information on third parties in the Intel® Communications Alliance who support Intel network processors and their development environment, visit: www.intel.com/go/ica

Intel Access

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For more information, visit the Intel web site at: **developer.intel.com**

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