

CD4095B, CD4096B Types

CMOS Gated J-K Master-Slave Flip-Flops

With Set-Reset Capability
High-Voltage Types (20-Volt Rating)

CD4095B Non-Inverting J and K Inputs
CD4096B Inverting and Non-Inverting J and K Inputs

The RCA-CD4095B and CD4096B are J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K inputs control transfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and \bar{Q} outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

The CD4095B and CD4096B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

MAXIMUM RATINGS, Absolute-Maximum Values:

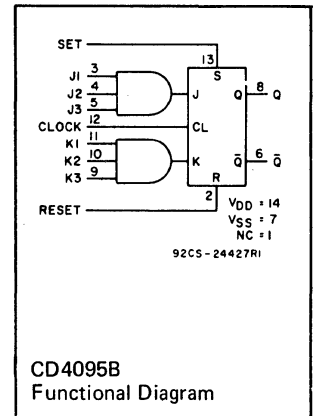
| | |
|---|--|
| DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal) | -0.5 to +20 V |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5 to $V_{DD} + 0.5$ V |
| DC INPUT CURRENT, ANY ONE INPUT | ± 10 mA |
| POWER DISSIPATION PER PACKAGE (P_D): | |
| For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E) | 500 mW |
| For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E) | Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW |
| For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F, K) | 500 mW |
| For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F, K) | Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ | 100 mW |
| OPERATING-TEMPERATURE RANGE (T_A): | |
| PACKAGE TYPES D, F, K, H | -55 to $+125^\circ\text{C}$ |
| PACKAGE TYPE E | -40 to $+85^\circ\text{C}$ |
| STORAGE TEMPERATURE RANGE (T_{stg}) | -65 to $+150^\circ\text{C}$ |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max. | $+265^\circ\text{C}$ |

Features:

- 16 MHz toggle rate (typ.) at $V_{DD} - V_{SS} = 10$ V
- Gated inputs
- 100% tested for quiescent current at 20 V
- Maximum input current of $1 \mu\text{A}$ at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin over full package-temperature range: 1 V at $V_{DD} = 5$ V, 2 V at $V_{DD} = 10$ V, 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Registers ■ Counters ■ Control circuits



CD4095B
Functional Diagram

TRUTH TABLES SYNCHRONOUS OPERATION (S=0 R=0)

| Inputs Before Positive Clock Transition | | Outputs After Positive Clock Transition | |
|---|----|---|-----------|
| J* | K* | Q | \bar{Q} |
| 0 | 0 | No Change | |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | Toggles | |

* For CD4095B For CD4096B
 $J = J_1 \cdot J_2 \cdot J_3$ $J = J_1 \cdot J_2 \cdot \bar{J}_3$
 $K = K_1 \cdot K_2 \cdot K_3$ $K = K_1 \cdot K_2 \cdot \bar{K}_3$

ASYNCHRONOUS OPERATION (J and K - DON'T CARE)

| S | R | Q | \bar{Q} |
|---|---|-----------|-----------|
| 0 | 0 | No Change | |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

0 = V_{SS} , 1 = V_{DD}

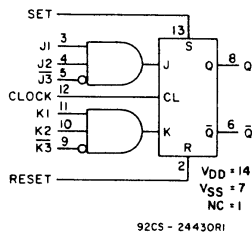


Fig. 1 - CD4096B Functional Diagram.

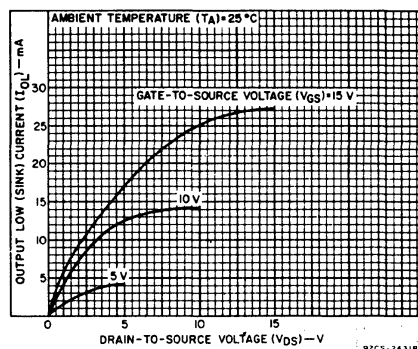


Fig. 2 - Typical output low (sink) current characteristics.

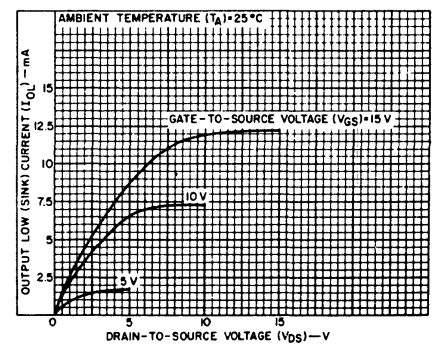


Fig. 3 - Minimum output low (sink) current characteristics.

CD4095B, CD4096B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | V_{DD} (V) | LIMITS | | UNITS |
|---|-----------------|--------|------|---------------|
| | | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) | | 3 | 18 | V |
| Data Setup Time, t_S | 5 | 400 | — | ns |
| | 10 | 160 | — | |
| | 15 | 100 | — | |
| Clock Pulse Width, t_W | 5 | 140 | — | ns |
| | 10 | 60 | — | |
| | 15 | 40 | — | |
| Clock Input Frequency, f_{CL} | 5 | — | 3.5 | MHz |
| | 10 | dc | 8 | |
| | 15 | — | 12 | |
| Clock Rise and Fall Time, t_{rCL} , t_{fCL} : | 5 | — | 15 | μs |
| | 10 | — | 5 | |
| | 15 | — | 5 | |
| Set or Reset Pulse Width, t_W | 5 | 200 | — | ns |
| | 10 | 100 | — | |
| | 15 | 50 | — | |

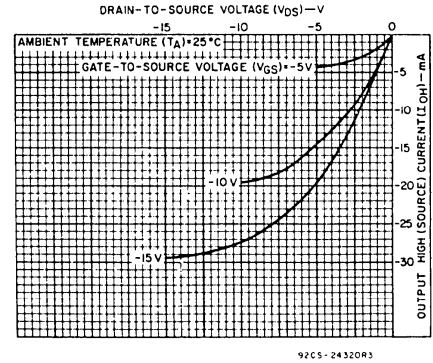


Fig.4 – Typical output high (source) current characteristics.

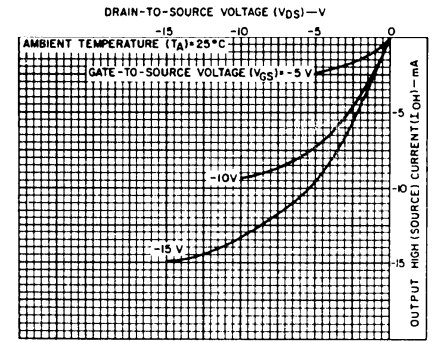


Fig.5 – Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES ($^\circ\text{C}$) | | | | | | | UNITS |
|---|--------------|-----------------|-----------------|---|-----------|---------|---------|--|---------------|-----------|---------------|
| | V_O (V) | V_{IN} (V) | V_{DD} (V) | Values at $-55, +25, +125$ Apply to D, F, K, H Packages | | | | Values at $-40, +25, +85$ Apply to E Package | | | |
| | | | | -55 | -40 | $+85$ | $+125$ | Min. | Typ. | Max. | |
| Quiescent Device Current, I_{DD} Max. | — | 0,5 | 5 | 1 | 1 | 30 | 30 | — | 0.02 | 1 | μA |
| | — | 0,10 | 10 | 2 | 2 | 60 | 60 | — | 0.02 | 2 | |
| | — | 0,15 | 15 | 4 | 4 | 120 | 120 | — | 0.02 | 4 | |
| | — | 0,20 | 20 | 20 | 20 | 600 | 600 | — | 0.04 | 20 | |
| Output Low (Sink) Current I_{OL} Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | — | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | — | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | — | |
| | 4.6 | 0,5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | — | |
| Output High (Source) Current, I_{OH} Min. | 2.5 | 0,5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | — | mA |
| | 9.5 | 0,10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | — | |
| | 13.5 | 0,15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | — | |
| | — | 0,5 | 5 | — | — | 0.05 | — | — | 0 | 0.05 | |
| Output Voltage: Low-Level, V_{OL} Max. | — | 0,10 | 10 | — | — | 0.05 | — | — | 0 | 0.05 | V |
| | — | 0,15 | 15 | — | — | 0.05 | — | — | 0 | 0.05 | |
| | — | 0,5 | 5 | — | — | 4.95 | — | — | 4.95 | 5 | |
| Output Voltage: High-Level, V_{OH} Min. | — | 0,10 | 10 | — | — | 9.95 | — | — | 9.95 | 10 | V |
| | — | 0,15 | 15 | — | — | 14.95 | — | — | 14.95 | 15 | |
| | — | 0,5 | 5 | — | — | 1.5 | — | — | 1.5 | — | |
| Input Low Voltage, V_{IL} Max. | 1, 9 | — | 10 | — | — | 3 | — | — | 3 | — | V |
| | 1.5, 13.5 | — | 15 | — | — | 4 | — | — | 4 | — | |
| | 0.5, 4.5 | — | 5 | — | — | 3.5 | — | — | 3.5 | — | |
| Input High Voltage, V_{IH} Min. | 1, 9 | — | 10 | — | — | 7 | — | — | 7 | — | V |
| | 1.5, 13.5 | — | 15 | — | — | 11 | — | — | 11 | — | |
| | — | 0,18 | 18 | ± 0.1 | ± 0.1 | ± 1 | ± 1 | — | $\pm 10^{-5}$ | ± 0.1 | |

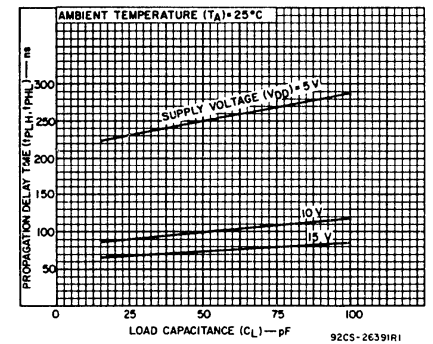


Fig.6 – Typical propagation delay time vs. load capacitance.

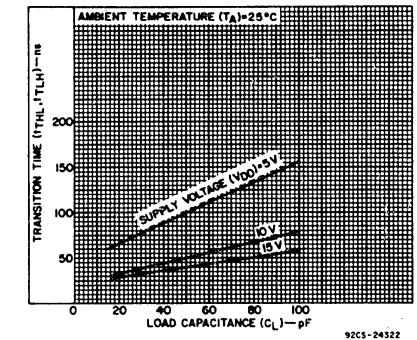


Fig.7 – Typical transition time vs. load capacitance.

CD4095B, CD4096B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ K}\Omega$

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | | UNITS | |
|---|-----------------|--------------|------|------|-------|---------------|
| | | V_{DD} (V) | MIN. | TYP. | | MAX. |
| Propagation Delay Time: t_{pHL}, t_{pLH} Clock | | 5 | — | 250 | 500 | ns |
| | | 10 | — | 100 | 200 | |
| | | 15 | — | 75 | 150 | |
| Set or Reset | | 5 | — | 150 | 300 | ns |
| | | 10 | — | 75 | 150 | |
| | | 15 | — | 50 | 100 | |
| Transition Time, t_{THL}, t_{TLH} | | 5 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| Maximum Clock Input Frequency, $(f_{CL})^*$ | | 5 | 3.5 | 7 | — | MHz |
| | | 10 | 8 | 16 | — | |
| | | 15 | 12 | 24 | — | |
| Minimum Clock Pulse Width, t_{W} | | 5 | — | 70 | 140 | ns |
| | | 10 | — | 30 | 60 | |
| | | 15 | — | 20 | 40 | |
| Clock Input Rise or Fall Time, t_{rcl}, t_{rcf} | | 5 | — | — | 15 | μs |
| | | 10 | — | — | 5 | |
| | | 15 | — | — | 5 | |
| Minimum Set or Reset Pulse Width, t_{W} | | 5 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 25 | 50 | |
| Minimum Data Setup Time, t_S | | 5 | — | 200 | 400 | ns |
| | | 10 | — | 80 | 160 | |
| | | 15 | — | 50 | 100 | |
| Input Capacitance, C_{IN} | Any Input | — | — | 5 | 7.5 | pF |

* $t_r, t_f = 5\text{ ns}$

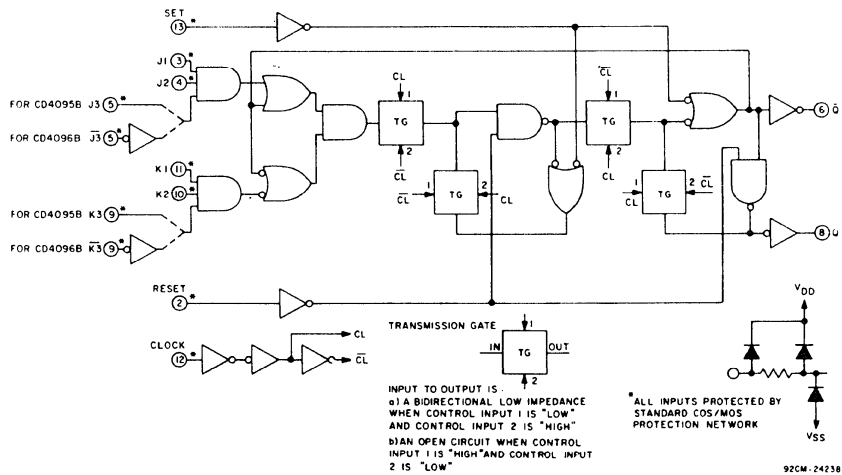


Fig.11 — CD4095B and CD4096B logic diagram.

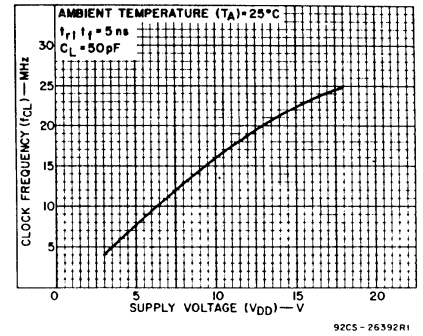


Fig.8 — Typical clock frequency vs. supply voltage (toggle mode—see Fig. 16).

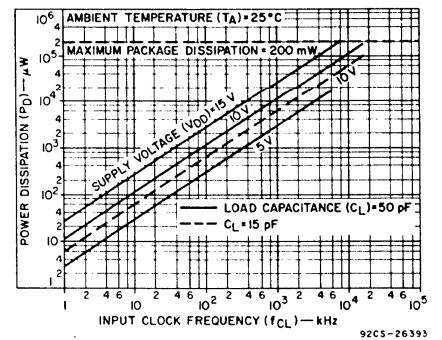


Fig. 9 — Typical power dissipation vs. input clock frequency.

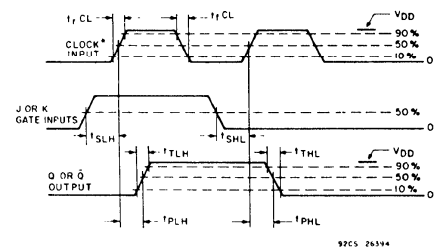


Fig.10 — Propagation delay, transition, and setup-time waveforms.

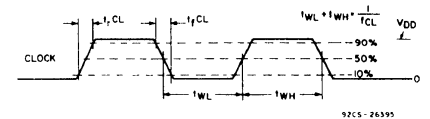


Fig.12 — Clock pulse rise and fall time waveforms.

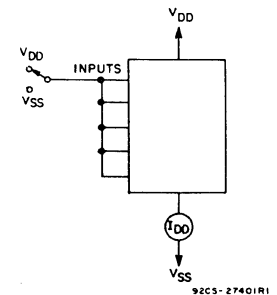


Fig.13 — Quiescent device current test circuit.

CD4095B, CD4096B Types

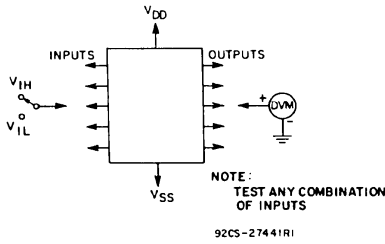


Fig. 14 - Input voltage test circuit.

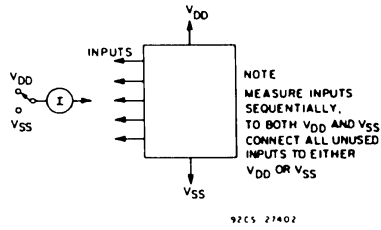


Fig. 15 - Input leakage current test circuit.

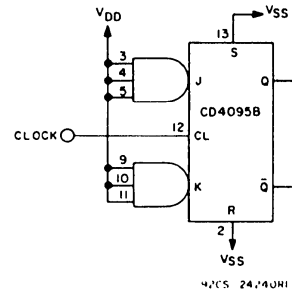


Fig. 16 - CD4095B connected in toggle mode.

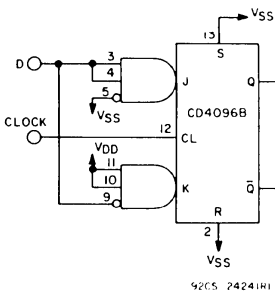
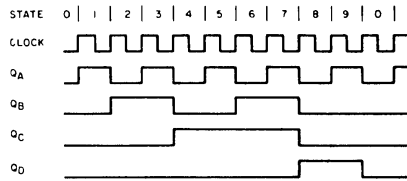
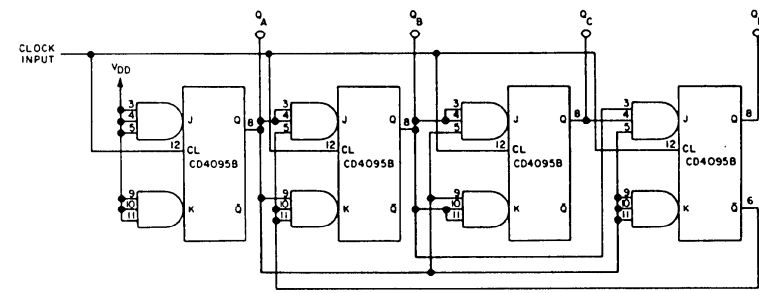


Fig. 17 - CD4096B connected as a "D" type flip-flop.



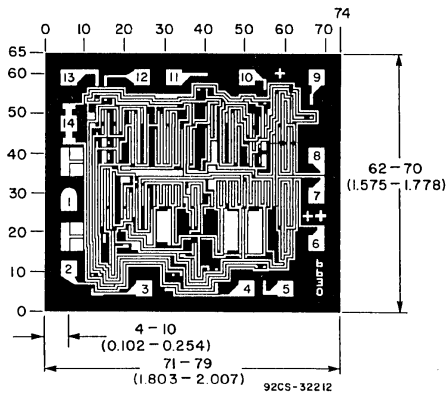
| STATE | QA | QB | QC | QD |
|-------|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 |

NOTE: PINS 2 & 13 RESET & SET, GO TO VSS ON ALL UNITS

92CM-24247RI

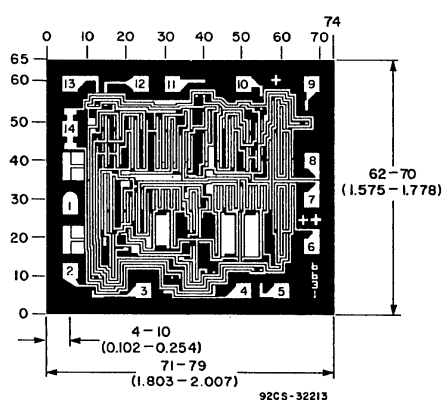
Fig. 18 - Synchronous binary divide-by-ten counter.

DIMENSIONS AND PAD LAYOUT FOR CD4095B AND CD4096B



CD4095BH

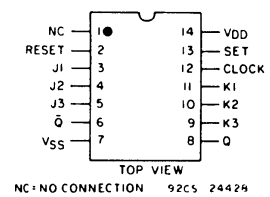
The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.



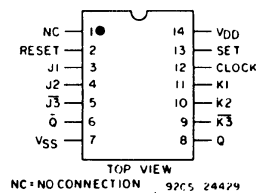
CD4096BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10-3 inch).

TERMINAL ASSIGNMENTS



CD4095B



CD4096B