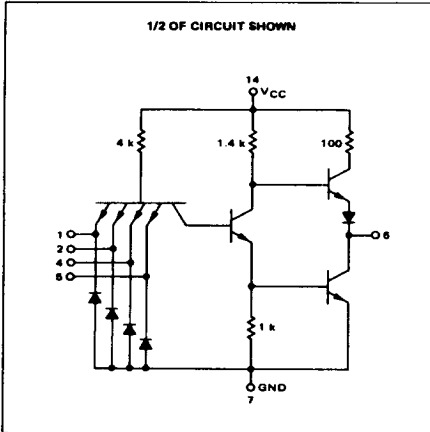


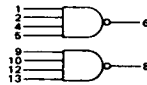
DUAL 4-INPUT "NAND" GATE

MTTL MC7400P series
MTTL MC5400L/7400L series

MC5420L*
MC7420P,L*



This device consists of two 4-input NAND gates. These gates may be cross-coupled to form a set-reset flip-flop.



Positive Logic: $6 = 1 + 2 + 4 + 5$
Negative Logic: $6 = 1 + 2 + 4 + 5$

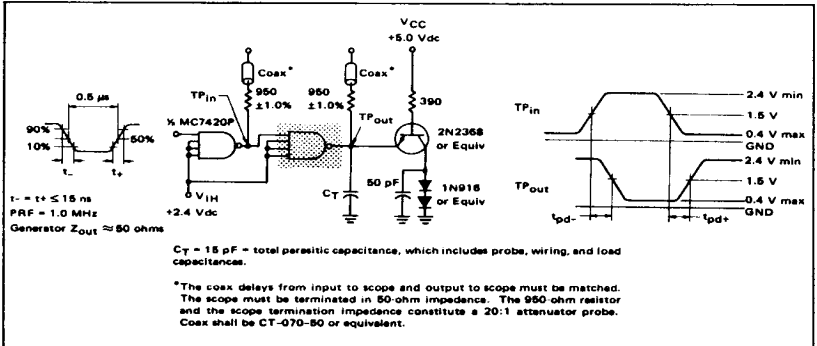
Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 20 mW typ/pkg
Propagation Delay Time = 13 ns typ

*L suffix = TO-118 ceramic package (Case 632)
P suffix = TO-118 plastic package (Case 606)
See General Information section for package outline dimensions.

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



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ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To determine testing sequences through remaining inputs.



Characteristic	Symbol	Pin Under Test	MC5420 Test Limits -55 to +125°C		MC7420 Test Limits 0 to +70°C		TEST CURRENT/VOLTAGE VALUES (All Temperatures)																	
			Min	Max	Unit	Min	Max	mA							Volts									
										I_{CC}	I_{OL}	I_{OH}	V_E	V_{F1}	V_{F2}	V_{OH1}	V_{OH2}	V_{OL1}	V_{OL2}	V_{CC1}	V_{CC2}			
										16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.5	5.5			
Input Forward Current	I_F	1	-	-1.6	mAdc	-	-1.6	mAdc	-	-	1	-	-	2.4,5	-	-	-	-	-	-	-	14	7*	
Leakage Current	I_{R1}	1	-	40	μ Adc	-	40	μ Adc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	2,4,5,7*	
	I_{R2}	1	-	1.0	mAdc	-	1.0	mAdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	2,4,5,7*	
	V_{OL}	6	-	0.4	Vdc	-	0.4	Vdc	-	-	-	-	-	-	-	1.2,4,5	-	-	-	-	-	14	7*	
V_{OH}	6	2,4	-	-	Vdc	2,4	-	Vdc	2,4	-	-	-	-	2,4,5	-	-	-	-	-	-	14	7*		
Short-Circuit Current	I_{SC}	6	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	2,4,5	-	-	1	-	-	-	14	7*		
Power Requirements (Total Device)	I_{PPH}	14	-	10.2	mAdc	-	10.2	mAdc	-	-	-	-	-	-	-	1,2,4,5,9,10,12,13	-	-	-	-	14	-	7	
Power-Supply Drain	I_{PDL}	14	-	3.6	mAdc	-	3.6	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,2,4,5,7*	
Switching Parameters	t_{pd}	1,6	-	15**	ns	-	15**	ns	-	-	2,4,5	-	-	-	-	-	-	-	-	-	14	-	7*	
t_{pl}	1,6	-	28**	ns	-	28**	ns	1	6	1	6	1	6	1	6	1	6	1	6	1	6	1	6	7*

*Ground inputs to gate not under test.

**Tested only at 25°C.

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