

## 27C256

### 256K (32K x 8) CHMOS EPROM

Intel's 27C256 is a 5V only, 262,144-bit Erasable Programmable Read Only Memory, organized as 32,768 words of 8 bits. Its standard pinouts provide for simple upgrades to 512 Kbits in the future in both DIP and SMT.

The 27C256 is ideal in embedded control applications based on advanced 16-bit CPUs. Fast 120 ns access times allow no-wait-state operation with the 12 MHz 80286. The 27C256 also excels in reprogrammable environments where the system designer must strike an optimal density/performance balance. For example, bootstrap and diagnostic routines run 1-wait-state on a 16 MHz 386™ microprocessor.

Intel offers two DIP profile options to meet your prototyping and production needs. The windowed ceramic dip (CERDIP) package provides erasability and reprogrammability for prototyping and early production. Once the design is in full production, the plastic dip (PDIP) one-time programmable part provides a lower cost alternative that is well adapted for auto insertion.

---

#### Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

#### Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

---

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

#### FOR REFERENCE ONLY



# 27C256

## 256K (32K x 8) CHMOS EPROM

- **High Speed**
  - 120 ns Access Time
- **Low Power Consumption**
  - 100  $\mu$ A Standby, 30 mA Active
- **Fast Programming**
  - Quick-Pulse Programming™ Algorithm
  - Programming Time as Fast as 4 Seconds
- **EPI Processing**
  - Maximum Latch-up Immunity
- **Simple Interfacing**
  - Two Line Control
  - CMOS and TTL Compatible
- **Versatile JEDEC-Approved Packaging**
  - Standard 28-Pin Cerdip
  - Compact 32-Lead PLCC
  - Cost Effective Plastic Dip

(See Packaging Spec., Order # 231399)

Intel's 27C256 is a 5V only, 262,144-bit Erasable Programmable Read Only Memory, organized as 32,768 words of 8 bits. Its standard pinouts provide for simple upgrades to 512 Kbits in the future in both DIP and SMT.

The 27C256 is ideal in embedded control applications based on advanced 16-bit CPUs. Fast 120 ns access times allow no-wait-state operation with the 12 MHz 80286. The 27C256 also excels in reprogrammable environments where the system designer must strike an optimal density/performance balance. For example, bootstrap and diagnostic routines run 1-wait-state on a 16 MHz 386™ microprocessor.

Intel offers two DIP profile options to meet your prototyping and production needs. The windowed ceramic dip (CERDIP) package provides erasability and reprogrammability for prototyping and early production. Once the design is in full production, the plastic dip (PDIP) one-time programmable part provides a lower cost alternative that is well adapted for auto insertion.

In addition to the JEDEC 28-pin DIP package, Intel also offers a 32-lead PLCC version of the 27C256. This one-time-programmable surface mount device is ideal where board space consumption is a major concern or where surface mount manufacturing technology is being implemented across an entire production line.

The 27C256 is equally at home in both TTL and CMOS environments. The Quick-Pulse programming™ algorithm improves speed as much as 100 times over older methods, further reducing cost for system manufacturers.

5

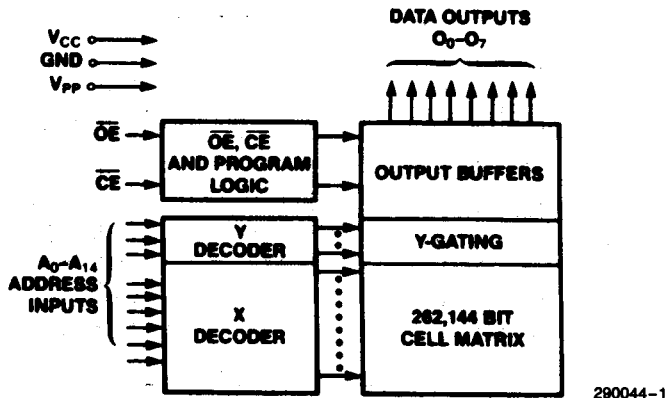
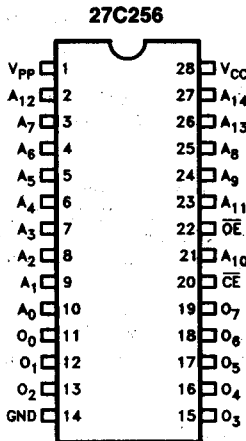


Figure 1. Block Diagram

Pin Names

A <sub>0</sub> -A <sub>15</sub>	ADDRESSES
O <sub>0</sub> -O <sub>7</sub>	OUTPUTS
OE	OUTPUT ENABLE
CE	CHIP ENABLE
PGM	PROGRAM
NC	NO CONNECT
DU	DON'T USE

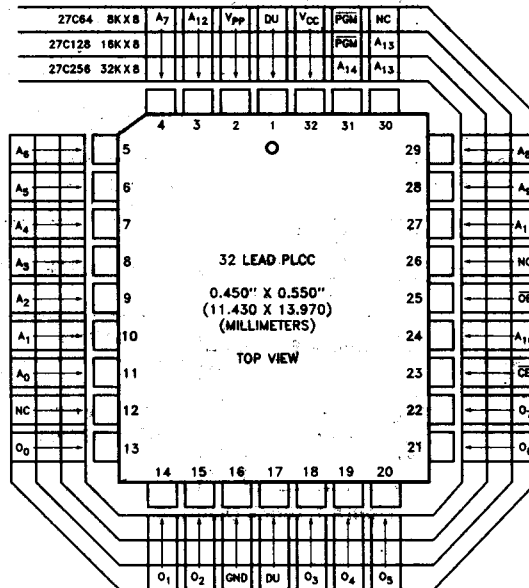
27512	27128A	2764A	2732A	2716
27C512	27C128	27C64		
A <sub>15</sub>	V <sub>PP</sub>	V <sub>PP</sub>		
A <sub>12</sub>	A <sub>12</sub>	A <sub>12</sub>		
A <sub>7</sub>	A <sub>7</sub>	A <sub>7</sub>	A <sub>7</sub>	A <sub>7</sub>
A <sub>6</sub>	A <sub>6</sub>	A <sub>6</sub>	A <sub>6</sub>	A <sub>6</sub>
A <sub>5</sub>	A <sub>5</sub>	A <sub>5</sub>	A <sub>5</sub>	A <sub>5</sub>
A <sub>4</sub>	A <sub>4</sub>	A <sub>4</sub>	A <sub>4</sub>	A <sub>4</sub>
A <sub>3</sub>	A <sub>3</sub>	A <sub>3</sub>	A <sub>3</sub>	A <sub>3</sub>
A <sub>2</sub>	A <sub>2</sub>	A <sub>2</sub>	A <sub>2</sub>	A <sub>2</sub>
A <sub>1</sub>	A <sub>1</sub>	A <sub>1</sub>	A <sub>1</sub>	A <sub>1</sub>
A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>
O <sub>0</sub>	O <sub>0</sub>	O <sub>0</sub>	O <sub>0</sub>	O <sub>0</sub>
O <sub>1</sub>	O <sub>1</sub>	O <sub>1</sub>	O <sub>1</sub>	O <sub>1</sub>
O <sub>2</sub>	O <sub>2</sub>	O <sub>2</sub>	O <sub>2</sub>	O <sub>2</sub>
GND	GND	GND	GND	GND



2716	2732A	27C64	27128A	27512
27C64	27C128	27C64	27C128	27C512
VCC	VCC	VCC	VCC	VCC
A <sub>6</sub>	A <sub>6</sub>	NC	PGM	A <sub>14</sub>
A <sub>9</sub>	A <sub>9</sub>	A <sub>6</sub>	A <sub>13</sub>	A <sub>13</sub>
V <sub>PP</sub>	A <sub>11</sub>	A <sub>6</sub>	A <sub>6</sub>	A <sub>6</sub>
OE	OE/V <sub>PP</sub>	A <sub>9</sub>	A <sub>9</sub>	A <sub>9</sub>
A <sub>10</sub>	A <sub>10</sub>	A <sub>11</sub>	A <sub>11</sub>	A <sub>11</sub>
CE	CE	OE	OE	OE/V <sub>PP</sub>
O <sub>7</sub>	O <sub>7</sub>	A <sub>10</sub>	A <sub>10</sub>	A <sub>10</sub>
O <sub>6</sub>	O <sub>6</sub>	CE	CE	CE
O <sub>5</sub>	O <sub>5</sub>	O <sub>7</sub>	O <sub>7</sub>	O <sub>7</sub>
O <sub>4</sub>	O <sub>4</sub>	O <sub>6</sub>	O <sub>6</sub>	O <sub>6</sub>
O <sub>3</sub>	O <sub>3</sub>	O <sub>5</sub>	O <sub>5</sub>	O <sub>5</sub>
		O <sub>4</sub>	O <sub>4</sub>	O <sub>4</sub>
		O <sub>3</sub>	O <sub>3</sub>	O <sub>3</sub>

290044-2

Figure 2. DIP Pin Configuration



290044-10

Figure 3. PLCC Lead Configuration

**EXTENDED TEMPERATURE (EXPRESS) EPROMs**

The Intel EXPRESS EPROM family receives additional processing to enhance product characteristics. EXPRESS processing is available for several densities allowing the appropriate memory size to match system requirements. EXPRESS EPROMs are available with 168 ± 8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This processing meets or exceeds most industry burn-in specifications. The EXPRESS product family is available in both 0°C to 70°C and -40°C to 85°C operating temperature range versions. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This allows reduction or elimination of incoming testing.

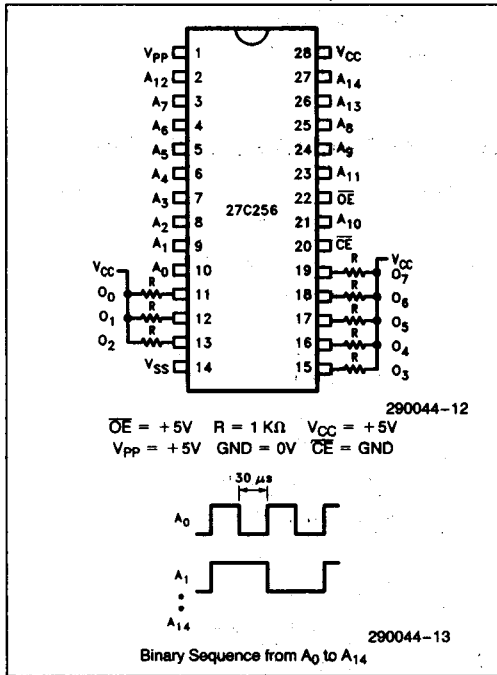
**Options**

Speed	Packaging		
	CERDIP	PLCC	PDIP
-120V10	Q, T, L	T	T
-200V10	Q, T, L	T	

**EXPRESS EPROM FAMILY**

**PRODUCT DEFINITIONS**

Type	Operating Temperature (°C)	Burn-in 125°C (hr)
Q	0°C to 70°C	168 ± 8
T	-40°C to 85°C	NONE
L	-40°C to 85°C	168 ± 8



**Burn-In Bias and Timing Diagrams**

**ABSOLUTE MAXIMUM RATINGS\***

- Operating Temperature ..... 0°C to 70°C(1)
- Temperature Under Bias ..... -10°C to 80°C
- Storage Temperature..... -65°C to 125°C
- Voltage on Any Pin (except A<sub>9</sub>, V<sub>CC</sub> and V<sub>PP</sub>)  
with Respect to GND ..... -2V to 7V(2)
- Voltage on A<sub>9</sub> with  
Respect to GND ..... -2V to 13.5V(2)
- V<sub>PP</sub> Supply Voltage  
with Respect to GND ..... -2V to 14.0V(2)
- V<sub>CC</sub> Supply Voltage with  
Respect to GND ..... -2V to 7.0V(2)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

**READ OPERATION DC CHARACTERISTICS(1) V<sub>CC</sub> = 5.0V ± 10%**

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I <sub>LI</sub>	Input Load Current	7		0.01	1.0	μA	V <sub>IN</sub> = 0V to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current				± 10	μA	V <sub>OUT</sub> = 0V to V <sub>CC</sub>
I <sub>SB</sub>	V <sub>CC</sub> Standby Current				1.0	mA	CE = V <sub>IH</sub>
					100	μA	CE = V <sub>CC</sub> ± 0.2V
I <sub>CC</sub>	V <sub>CC</sub> Operating Current	3			30	mA	CE = V <sub>IL</sub> f = 5 MHz
I <sub>PP</sub>	V <sub>PP</sub> Operating Current	3			200	μA	V <sub>PP</sub> = V <sub>CC</sub>
I <sub>OS</sub>	Output Short Circuit Current	4, 6			100	mA	
V <sub>IL</sub>	Input Low Voltage		-0.5		0.8	V	
V <sub>IH</sub>	Input High Voltage		2.0		V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage				0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage		2.4			V	I <sub>OH</sub> = -400 μA
V <sub>PP</sub>	V <sub>PP</sub> Operating Voltage	5	V <sub>CC</sub> - 0.7		V <sub>CC</sub>	V	

**NOTES:**

1. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS versions.
2. Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods < 20 ns. Maximum DC voltage on input/output pins is V<sub>CC</sub> + 0.5V which, during transitions, may overshoot to V<sub>CC</sub> + 2.0V for periods < 20 ns.
3. Maximum active power usage is the sum I<sub>PP</sub> + I<sub>CC</sub>. Maximum current value is with outputs O<sub>0</sub> to O<sub>7</sub> unloaded.

4. Output shorted for no more than one second. No more than one output shorted at a time.
5. V<sub>PP</sub> may be connected directly to V<sub>CC</sub>, or may be one diode voltage drop below V<sub>CC</sub>. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.
6. Sampled, not 100% tested.
7. Typical limits are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

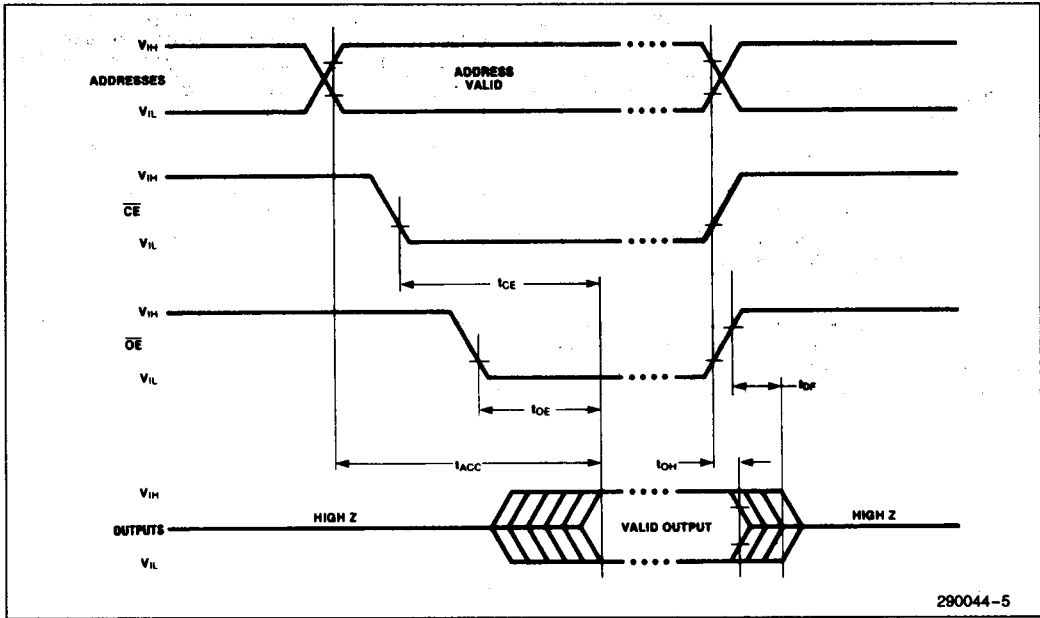
**READ OPERATION AC CHARACTERISTICS(1)**  $V_{CC} = 5.0V \pm 10\%$ 

Versions(4)		$V_{CC} \pm 10\%$	27C256-120V10 P27C256-120V10 N27C256-120V10		27C256-150V10 P27C256-150V10 N27C256-150V10		27C256-200V10 P27C256-200V10 N27C256-200V10		Unit
Symbol	Parameter	Notes	Min	Max	Min	Max	Min	Max	
$t_{ACC}$	Address to Output Delay			120		150		200	ns
$t_{CE}$	$\overline{CE}$ to Output Delay	2		120		150		200	ns
$t_{OE}$	$\overline{OE}$ to Output Delay	2		55		60		75	ns
$t_{DF}$	$\overline{OE}$ High to Output High Z	3		30		50		55	ns
$t_{OH}$	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	3	0		0		0		ns

**NOTES:**

1. See AC Input/Output Reference Waveform for timing measurements.
2.  $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
3. Sampled, not 100% tested.
4. Package Prefixes: No Prefix = CERDIP; N = PLCC; P = PDIP.

AC WAVEFORMS



290044-5

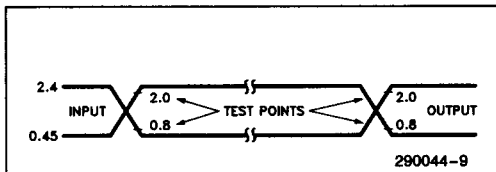
CAPACITANCE<sup>(1)</sup> T<sub>A</sub> = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Units	Conditions
C <sub>IN</sub>	Address/Control Capacitance	6	pF	V <sub>IN</sub> = 0V
C <sub>OUT</sub>	Output Capacitance	12	pF	V <sub>OUT</sub> = 0V

NOTE:

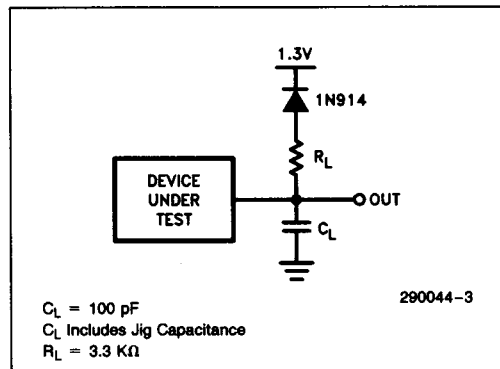
1. Sampled, not 100% tested.

AC INPUT/OUTPUT REFERENCE WAVEFORM



AC test inputs are driven at V<sub>OH</sub> (2.4 V<sub>TTL</sub>) for a logic "1" and V<sub>OL</sub> (0.45 V<sub>TTL</sub>) for a logic "0". Input timing begins at V<sub>IH</sub> (2.0 V<sub>TTL</sub>) and V<sub>IL</sub> (0.8 V<sub>TTL</sub>). Output timing ends at V<sub>IH</sub> and V<sub>IL</sub>. Input rise and fall times (10% to 90%) ≤ 10 ns.

AC TESTING LOAD CIRCUIT



C<sub>L</sub> = 100 pF  
 C<sub>L</sub> Includes Jig Capacitance  
 R<sub>L</sub> = 3.3 KΩ

## DEVICE OPERATION

The Mode Selection table lists 27C256 operating modes. Read Mode requires a single 5V power supply. All inputs, except  $V_{CC}$  and  $V_{PP}$ , and  $A_9$  during intelligent Identifier Mode, are TTL or CMOS.

Table 1. Mode Selection

Mode	Notes	$\overline{CE}$	$\overline{OE}$	$A_9$	$A_0$	$V_{PP}$	$V_{CC}$	Outputs
Read	1	$V_{IL}$	$V_{IL}$	X	X	$V_{CC}$	$V_{CC}$	$D_{OUT}$
Output Disable		$V_{IL}$	$V_{IH}$	X	X	$V_{CC}$	$V_{CC}$	High Z
Standby		$V_{IH}$	X	X	X	$V_{CC}$	$V_{CC}$	High Z
Program	2	$V_{IL}$	$V_{IH}$	X	X	$V_{PP}$	$V_{CP}$	$D_{IN}$
Program Verify		$V_{IH}$	$V_{IL}$	X	X	$V_{PP}$	$V_{CP}$	$D_{OUT}$
Program Inhibit		$V_{IH}$	$V_{IH}$	X	X	$V_{PP}$	$V_{CP}$	HIGH Z
intelligent Identifier -Manufacturer	2, 3	$V_{IL}$	$V_{IL}$	$V_{ID}$	$V_{IL}$	$V_{CC}$	$V_{CC}$	89 H
intelligent Identifier -Device	2, 3, 4	$V_{IL}$	$V_{IL}$	$V_{ID}$	$V_{IH}$	$V_{CC}$	$V_{CC}$	8D H

### NOTES:

1. X can be  $V_{IL}$  or  $V_{IH}$ .
2. See DC Programming Characteristics for  $V_{CP}$ ,  $V_{PP}$  and  $V_{ID}$  voltages.
3.  $A_1-A_8, A_{10-14} = V_{IL}$ .
4. Programming equipment may also refer to this device as the 27C256A. Older devices may have device ID = 8CH.

### Read Mode

The 27C256 has two control functions, both must be enabled to obtain data at the outputs.  $\overline{CE}$  is the power control and device select.  $\overline{OE}$  controls the output buffers to gate data to the outputs. With addresses stable, the address access time ( $t_{ACC}$ ) equals the delay from  $\overline{CE}$  to output ( $t_{CE}$ ). Outputs display valid data  $t_{OE}$  after  $\overline{OE}$ 's falling edge, assuming  $t_{ACC}$  and  $t_{CE}$  times are met.

$V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

### Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

- a) lowest possible memory power dissipation
- b) complete assurance that data bus contention will not occur

To efficiently use these two control inputs, an address decoder should enable  $\overline{CE}$ , while  $\overline{OE}$  should be connected to all memory devices and the system's READ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

### Standby Mode

Standby Mode substantially reduces  $V_{CC}$  current. When  $\overline{CE} = V_{IH}$ , the outputs are in a high impedance state, independent of  $\overline{OE}$ .



## Program Mode

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" are programmed, the data word can contain both "1's" and "0's". Ultraviolet light erasure is the only way to change "0's" to "1's".

Program Mode is entered when  $V_{PP}$  is raised to 12.75V. Data is introduced by applying an 8-bit word to the output pins. Pulsing  $\overline{CE}$  low while  $\overline{OE} = V_{IH}$  programs that data into the device.

## Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With  $V_{CC}$  at 6.25V a substantial program margin is ensured. The verify is performed with  $\overline{CE}$  at  $V_{IH}$ . Valid data is available  $t_{OE}$  after  $\overline{OE}$  falls low.

## Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data.  $\overline{CE}$ -high inhibits programming of non-targeted devices. Except for  $\overline{CE}$  and  $\overline{OE}$ , parallel EPROMs may have common inputs.

## intelligent Identifier™ Mode

The intelligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with its proper programming algorithm.

This mode is activated when a programmer forces 12V + 0.5V on  $A_9$ . With  $\overline{CE}$ ,  $\overline{OE}$ ,  $A_1$ - $A_8$ , and  $A_{10}$ - $A_{14}$  at  $V_{IL}$ ,  $A_0 = V_{IL}$  will present the manufacturer code and  $A_0 = V_{IH}$  the device code. This mode functions in the 25°C ± 5°C ambient temperature range required during programming.

## UPGRADE PATH

Future upgrade to the 512 Kbit density is easily accomplished due to the standardized pin configuration of the 27C256. A jumper between  $A_{15}$  and  $V_{CC}$

allows upgrade using the  $V_{PP}$  pin. Systems designed for 256 Kbit program memories today can be upgraded to 512 Kbit in the future with no circuit board changes.

## SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues: standby current levels ( $I_{SB}$ ), active current levels ( $I_{CC}$ ), and transient current peaks produced by falling and rising edges of  $\overline{CE}$ . Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-Line Control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1  $\mu$ F ceramic capacitor connected between its  $V_{CC}$  and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every 8 devices, a 4.7  $\mu$ F electrolytic capacitor should be placed at the array's power supply connection between  $V_{CC}$  and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

## ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain fluorescent lamps have wavelengths in the 3000Å-4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm<sup>2</sup>. Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000  $\mu$ W/cm<sup>2</sup> power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm<sup>2</sup> (1 week @ 12000  $\mu$ W/cm<sup>2</sup>).

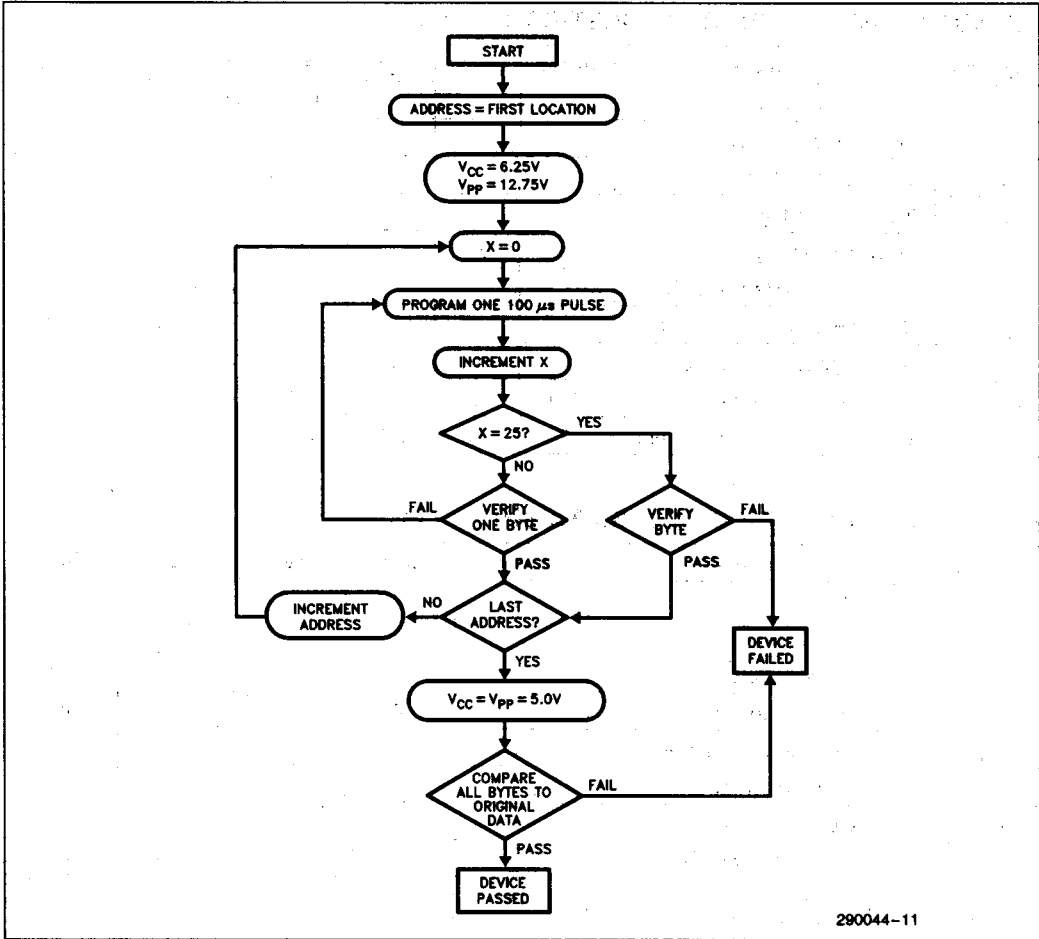


Figure 4. Quick-Pulse Programming™ Algorithm

**Quick-Pulse Programming™ Algorithm**

The Quick-Pulse Programming algorithm programs Intel's 27C256. Developed to substantially reduce programming throughput, this algorithm can program the 27C256 as fast as 4 seconds. Actual programming time depends on programmer overhead.

The Quick-Pulse programming algorithm employs a 100 μs pulse followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm terminates if 25 attempts fail to program a byte.

The entire program pulse/byte verify sequence is performed with VPP = 12.75V and VCC = 6.25V. When programming is complete, all bytes are compared to the original data with VCC = VPP = 5.0V.

**DC PROGRAMMING CHARACTERISTICS**  $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ 

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
$I_{LI}$	Input Load Current				1.0	$\mu\text{A}$	$V_{IN} = V_{IL}$ or $V_{IH}$
$I_{CP}$	$V_{CC}$ Program Current	1			30	mA	$\overline{CE} = V_{IL}$
$I_{PP}$	$V_{PP}$ Program Current	1			50	mA	$\overline{CE} = V_{IL}$
$V_{IL}$	Input Low Voltage		-0.1		0.8	V	
$V_{IH}$	Input High Voltage		2.4		6.5	V	
$V_{OL}$	Output Low Voltage (Verify)				0.45	V	$I_{OL} = 2.1$ mA
$V_{OH}$	Output High Voltage (Verify)		3.5			V	$I_{OH} = -2.5$ mA
$V_{ID}$	$A_9$ Intelligent Identifier Voltage		11.5	12.0	12.5	V	
$V_{PP}$	$V_{PP}$ Program Voltage	2, 3	12.5	12.75	13.0	V	
$V_{CP}$	$V_{CC}$ Supply Voltage (Program)	2	6.0	6.25	6.5	V	

**AC PROGRAMMING CHARACTERISTICS(4)**  $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ 

Symbol	Parameter	Notes	Min	Typ	Max	Unit
$t_{VCS}$	$V_{CP}$ Setup Time	2	2			$\mu\text{s}$
$t_{VPS}$	$V_{PP}$ Setup Time	2	2			$\mu\text{s}$
$t_{AS}$	Address Setup Time		2			$\mu\text{s}$
$t_{DS}$	Data Setup Time		2			$\mu\text{s}$
$t_{PW}$	$\overline{CE}$ Program Pulse Width		95	100	105	$\mu\text{s}$
$t_{DH}$	Data Hold Time		2			$\mu\text{s}$
$t_{OES}$	$\overline{OE}$ Setup Time		2			$\mu\text{s}$
$t_{OE}$	Data Valid from $\overline{OE}$	5			150	ns
$t_{DFP}$	$\overline{OE}$ High to Output High Z	5, 6	0		130	ns
$t_{AH}$	Address Hold Time		0			$\mu\text{s}$

**NOTES:**

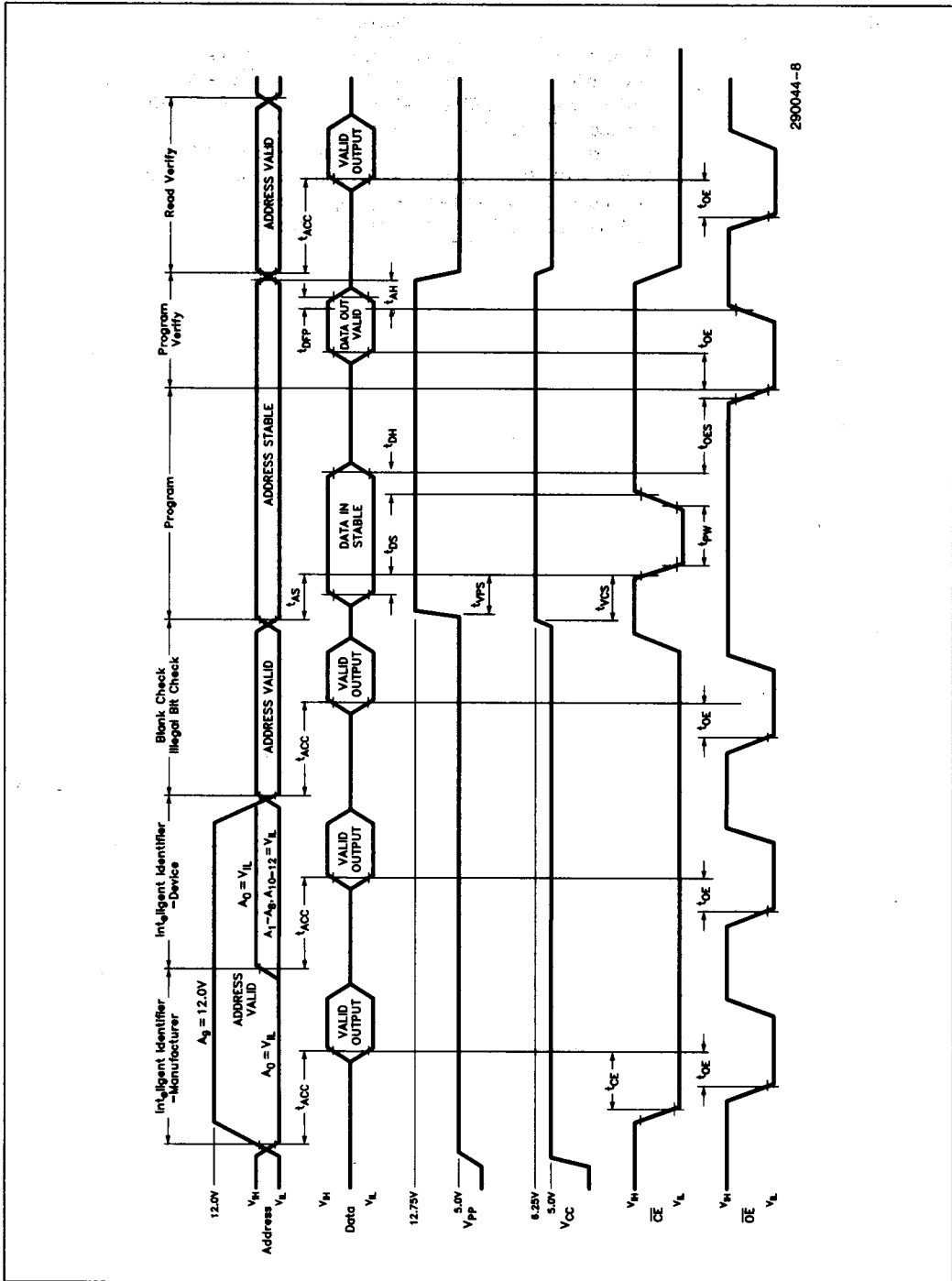
- Maximum current value is with outputs  $O_0$  to  $O_7$  unloaded.
- $V_{CP}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
- When programming, a  $0.1 \mu\text{F}$  capacitor is required across  $V_{PP}$  and GND to suppress spurious voltage transients which can damage the device.

4. See AC Input/Output Reference Waveform for timing measurements.

5.  $t_{OE}$  and  $t_{DFP}$  are device characteristics but must be accommodated by the programmer.

6. Sampled, not 100% tested.

PROGRAMMING WAVEFORMS



## REVISION HISTORY

Number	Description
010	Revised general datasheet structure, text to improve clarity Revised $I_{SB}$ Test Condition from $\overline{CE} = V_{CC}$ to $\overline{CE} = V_{CC} \pm 0.2V$ Revised $V_{OH}$ from 3.5V to 2.4V, $I_{OH}$ from -2.5 mA to -400 $\mu A$ Deleted 512K PLCC pinout references Deleted -150V10, -2, -20, -STD and -25 EXPRESS offerings Added -120V10, -200V10, PLCC and PDIP EXPRESS offerings Deleted -20, -25 and all 5% $V_{CC}$ speed bins Added PLCC and PDIP -120 speed bin packages